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REDCLIFFE

DL 901 TRANSIENT RECORDER

TECHNICAL MANUAL



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DL901

Transient Recorder

Technical Manual

PREFACE

This document is a guide to the servicing and repair of the DL901 Transient Recorder. It contains logic diagrams and descriptions, and fault diagnosis charts, and should be used in conjunction with the DL901 Operating Manual.

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1 DATA SHEET

1.1 SIGNAL INPUT

Input Range : 50mV to 50V f.s. in 1-2-5 steps.
 D.C. Offset : $\pm 1.5 \times$ voltage range — continuously variable.
 Overload : $\pm 100V$ max. $< 5\mu s$ recovery from 10 x f.s. overload.
 Impedance : $1M\Omega$ 24pF.
 Coupling : D.C.; A.C. to 2Hz; or grounded.
 Frequency Response : D.C. to 100kHz on all ranges.

1.2 ANALOGUE/DIGITAL CONVERSION

Resolution : 0.4% for f.s. input.
 Conversion Time : $5\mu s$ including sample and hold. Aperture time 40ns.

1.3 TRIGGERING

Modes : AUTO :- recording cycle initiated every 100ms, or by acceptable trigger.
 CONT :- new recording cycle initiated by every acceptable trigger.
 SINGLE :- one trigger only is accepted when the unit is armed — by front panel push-button or remote TTL pulse at rear panel connector. A lamp indication is given when the recorder is armed.
 Source : Internal from input amplifier; external input; front panel push-button; or remote TTL pulse at rear panel connector.
 Input Impedance : $1M\Omega$, 36pF.
 Coupling : D.C.; A.C. to 2Hz; pulse width $0.5\mu s$ min.
 Level : Internal, variable over signal input range. External, $\pm 5V$.
 Slope : Positive or negative.
 Pulse height (minimum) : Internal, 5% of input signal. External, 0.5V.

1.4 RECORDING CYCLE

Store Size : 1024 words, 8 bit.
 Sweep Time : 5ms to 200s for 1000 samples, in a 1-2-5 sequence.
 EXT position allows an external pulse train to define sampling rate in range 1kHz to 200kHz (1ms latency below 1kHz).
 Sweep Delay : 10 position switch, from 0 to 90% of sweep time.
 Sweep Modes : Delayed sweep, the sweep starts at the end of a trigger initiated delay of 0 to $0.9 \times$ sweep time. Pre-trigger, continuous recording commences when recorder is armed and stops after trigger initiated delay (0 to $0.9 \times$ sweep time) is complete.
 Timing Accuracy : Delay and sweep time derived from a 3.0 MHz crystal oscillator. Trigger synchronisation within 333ns.

1.5 OSCILLOSCOPE OUTPUT

The first 1000 samples can be displayed on an oscilloscope (in a Y/t mode) when not recording or when sweep time > 1 sec.

Y Output : $\pm 0.5V$ f.s.
 Ys Output : $\pm 0.5V$ f.s.
 CRO Trigger : $5\mu s$ pulse, 0V to +15V.
 Z+ : 1ms signal, 0V to +15V to brighten trace.
 Z- : 1ms signal, 0V to -15V to brighten trace.

1.6 PLOTTER OUTPUT

The analogue equivalent of the first 1000 samples is output at a slow rate to a Y/t recorder.

Y Plot : $\pm 0.5V$ f.s. for f.s. input. Active only in plot mode.

Rate : 0.2s per sample. An internal adjustment will set the rate between 20ms and 0.5s per sample.

1.7 DIGITAL OUTPUT

All 1024 samples are available via the built-in parallel buffered digital interface. This information is on the 24-way socket. Mating plug Amphenol 57-30240.

Data : 8-bit binary, parallel by bit, serial by character, TTL compatible, +ve true. Output rate continuously variable from $1.3\mu s$ to 1ms per point. Below 1ms rate a latency of up to 1024ms may occur before the data is present in the output buffer. Fast and slow rates may be mixed.

Control : Digital output initiated from front or rear panel. Data transfer controlled by 'Word Request' and 'Data Ready' signals. TTL compatible +ve true.

1.8 MECHANICAL

Power Supply : 210/260V or 105/130V, 50/60Hz, 45VA.

Size : W – 233mm (9.2in), H – 103mm (4.1in), D – 417mm (16.4in).

Weight : 5.5kg (12lbs) nett.

Operating Temperature : 0 - 55°C.

DL901 RM option : Recorder in a 19 inch rack mount case.

DL901 RM2 : Two recorders side by side in a 19 inch rack mount case.

2 INTRODUCTION

This manual contains a technical description of the DL901 Transient Recorder and data required for service and calibration procedure.

The first section comprises a general description of the instrument referring to a block diagram which illustrates the basic components of the recorder and their interconnection. A circuit description follows in which each part of the recorder is explained in detail using text and circuit diagrams to illustrate the operation and the interrelation of the individual circuits and Front Panel controls. The last section of the manual contains a set-up procedure for the recorder and a trouble shooting guide.

The DL901 Operating Manual should be used in conjunction with this manual.

3 PRINCIPLES OF OPERATION

The block diagram (Figure 3-1) illustrates the arrangement of the basic components in the DL901.

The input signal is amplified and then sampled and converted to digital form by the successive approximation analog-to-digital converter. The digital data is stored in an MOS shift register memory from which it can be output digitally. By using the digital-to-analog converter, a reconstructed analog signal (representing the original signal) can be produced to drive a display CRO or pen recorder. When not recording, the DL901 store is clocked continuously so that the stored record, via the digital-to-analog converter, can be used to drive the Y axis of a CRO: timebase trigger and Z modulation circuits complete the CRO drive requirement.

The display mode may be interrupted by a digital output (punch) or plot request or by the initiation of a new recording cycle by the arm and trigger circuits. The analog-to-digital converter, operating at a word rate defined by the Sweep time control, then digitises the preamplified input signal into eight-bit binary coded numbers. The eight-bit numbers are fed into a 1024 x 8 bit recirculating store comprising eight MOS shift registers. When recording, new data is fed in and old data is shifted out until the store is full. Then the new record is held in the memory and is recirculated continuously. On readout, digital words are successively placed in the output buffer register to drive both the digital-to-analog converter and the digital output lines via the appropriate plug-in digital interface.

The word rate of the analog-to-digital converter is controlled by the timebase generator. A 3.3MHz crystal controlled oscillator drives a chain of $\div 2$, $\div 5$, $\div 10$ counters. The SWEEP TIME control selects a particular output from the divider to define the converter word rate. Auxiliary outputs from the timebase control the display, plot and auto trigger rates. Sweep delays from the front panel DELAY lever switch are set into the delay counter and counted down through zero. The counter underflow signals the end of the delay period to the control logic.

A 10-bit binary address counter (AC) is used to identify each word in the store. Reset at the start of a recording, it is incremented at each memory cycle until, on overflow, it indicates that the store is full. A decoder for AC = 1000 indicates when word 1000 has been accessed so that the display Z modulation or Y Plot signals can be terminated.

The 10-bit binary N counter is needed because of the dynamic nature of the MOS memory shift registers. These shift registers have to be clocked continually at not less than 1kHz :- below this rate data might be lost. Thus, when access rates less than 1kHz are required, the store is clocked continuously in a recirculating mode and data is written in or read out as the correct word position is reached; hence the one millisecond latency referred to in the External Advance and Digital Output modes. In the Plot mode and while recording sweeps of two seconds or longer the store is clocked at a 1MHz data rate and data is extracted or inserted asynchronously. The Digital Output and External Advance modes interpose the maximum one millisecond static period between each recirculation; the store is recirculated back to, and pauses on, the correct word position ready to synchronise to the external control without latency if possible. The N counter is used to mark the word position which is to be accessed. It is incremented when access is required e.g. by the External Advance pulse train or Digital Word Request. By comparing AC and N counters the AC = N signal will indicate when the correct word position has been reached in the recirculation, and then either (a) data may be strobed out or (b) the recirculation path may be broken to insert a new data word.

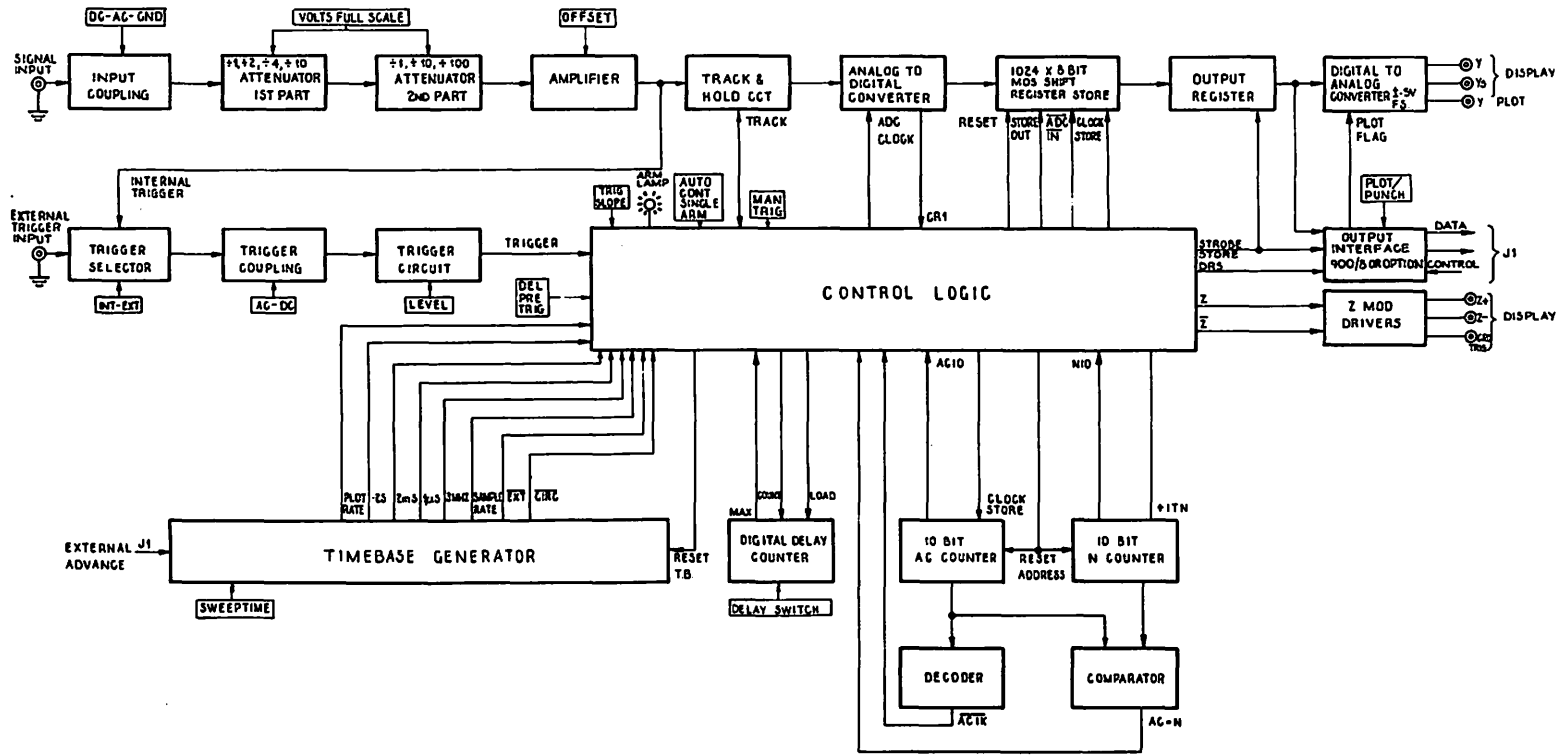


Figure 3-1 Block Diagram

4 CIRCUIT DESCRIPTION

4.1 GENERAL

This section of the manual comprises a detailed explanation of the circuits in the DL901 Transient Recorder. The instrument comprises a Front Panel on which the manual controls are situated, a single printed circuit card containing the active circuits, a plug-in interface card and a rear panel mounted power unit. 74N series TTL logic is used throughout with conventional symbols and positive true notation. In the text un-named logic elements are referred to by their position and output pin number, e.g. gate J7/6 refers to output pin 6 of the gate positioned at column J row 7 of the positioning matrix used on the printed circuit card.

The main Transient Recorder circuits are shown by Figures 6-13 to 6-18. These drawings are divided into sections A-F, 1-4 to enable the tracing of signals, e.g. the outgoing LINK signal (figure 6-13, Sheet 1) is marked 2E3 which can be found on Sheet 2 (Figure 6-14) in section E3. The layout of the main printed circuit board is shown in Figures 6-17 and 6-18.

Removing the top cover panel allows access to the Front Panel, power unit and component side of the main circuit card. Removing the lower cover panel provides access to the underside of the main circuit card including numerous Test Points (TP) for signal monitoring, attenuator trimmer capacitors, preamplifier gain adjustment, trigger level zero adjustment, digital-to-analog (D/A) converter linearity controls and the plug in interface card. Standard or optional interface cards are inserted into a 64-way edge connector so that the components on the interface card face downwards — closest to the low cover panel.


On replacement, cover panels should be positioned so that the cooling slots are positioned above the rear mounted power unit.

4.2 FRONT PANEL

4.2.1 General

The Front Panel contains the manual controls that define the DL901 operating parameters. The individual controls are described below and are illustrated schematically on the drawings of the circuits to which they are connected.

4.2.2 Controls

VOLTS FULL SCALE	This six-section switch forms an integral part of the attenuator which precedes the preamplifier. Attenuation factors of 1 to 1000 can be inserted in the signal path to reduce the signal to the 50mV fullscale input requirement of the fixed gain (100) amplifier.
INPUT COUPLING	Provides either D.C or A.C. coupling via a front panel-mounted 0,1 μ F capacitor. The  position disconnects the signal and grounds the amplifier input.
OFFSET	The - 15V (Clockwise) to +15V output of this potentiometer is used to shift the input signal within the dynamic range of the instrument. It is applied within the preamplifier and results in an offset range of $\pm 1,5x$ the volts full scale setting.
TRIGGER MODE	Three signals AUTO, CONT and ARM SW are generated. AUTO or CONT are grounded to indicate automatically initiated triggering or continuous triggering. Both signals at +5V select single triggering and ARM SW is grounded when the switch lever is depressed to arm the DL901.
ARM LIGHT	This is a light emitting diode which is lit when the recorder is armed to accept a trigger. The light is extinguished after the trigger has occurred.
TRIGGER SOURCE/ SLOPE	This selects the preamplifier output for internal triggering (INT) or an externally applied signal (EXT) to trigger the recorder. A D.C. level -VE TRIG is at +5V for -ve slope triggering or 0V for +ve slope triggering; edge selection occurs within the control logic.
MAN TRIG	This push button produces a trigger via a wired OR with the TTL digital trigger facility. Operable regardless of trigger source.

TRIGGER COUPLING	This provides either A.C. or D.C. coupling for the selected trigger source. A.C. coupling is via a front panel-mounted 0,1 μ F capacitor.
TRIGGER LEVEL	The +15V (Clockwise) to -15V output of this potentiometer provides the reference level for the trigger circuit comparator.
RECORD MODE	This selects delayed sweep or pre-trigger recording by grounding its PRE output or switching it to +5V.
DELAY	Defines the recording sweep delays in increments of 100 samples. The amount of delay is indicated by four signals $\overline{D1}$, $\overline{D2}$, $\overline{D4}$ and $\overline{D8}$ in -ve true 1-2-4-8 BCD code.
SWEPTIME	The recording sweep sample rate is defined by this control via a set of five D.C. signals SA, SB, SC, SX and SY which are at 0V or +5V to select the appropriate timebase output.
PUNCH/PLOT	This switch controls the manual initiation of the DL901 output modes. Operating the switch grounds the appropriate control signal ($\overline{PUNCH SW}$ or $\overline{PLOT SW}$) and readout starts within one millisecond.
POWER	A two-position toggle switch which interrupts the mains supply to the power unit (down for on). Power on is indicated by the adjacent light emitting diode which is powered from the +5V stabilised supply.

4.2.3 Dis-assembly

Remove A.C. power from the recorder.

Remove the top and bottom cover panels — note that on reassembly the cooling slots position above and below the rear mounted power unit.

From above, pull off the panel wiring from the printed circuit board 'disconnect' pins, unplug the blue/brown power leads, remove the two knurled screws (6BA), the two knurled nuts (R24) and the attenuator screen (see Figure 4-1). From below the recorder, remove the remaining panel wiring from the printed circuit board 'disconnect' pins.

NOTE

On later models, only the Input Socket ground and Trigger source are connected via the 'disconnect' pins. The remainder of the panel wiring is connected via two multi-way connectors, accessible from the top of the recorder.

The attenuator switch is mounted on the main printed circuit board (PCB) and remains in position when the Front Panel is removed. Using a 4BA Allen key, remove the knob from the VOLTS FULL SCALE switch and then remove the retaining nut.

The front panel can be withdrawn sufficiently to allow the signal input lead to be removed from the attenuator switch. The Front Panel can now be completely removed.

The rotary controls, pushbutton and power switch can be removed after undoing their retaining nuts. The other controls are fixed to a sub-panel and can be removed after the rotary controls, pushbutton and power switch have been removed. The lettered top panel can then be lifted off to reveal the fixings for the other components.

Re-assembly is achieved by reversing the disassembly procedure.

Refer to Figure 4-1 for details of Front Panel wiring colour codes on early units. Later units have the colour codes silk-screened against the appropriate 'disconnect' pins on the main PCB. When replacing 'disconnect' sockets onto the pins, ensure that positive location is achieved.

4.3 INPUT AMPLIFIER & TRIGGER CIRCUIT

4.3.1 Amplifier

The DL901 preamplifier comprises an attenuator and fixed gain amplifier. According to the selected VOLTS FULL SCALE setting, the input signal is attenuated by a factor between 1 (50mV) and 1000 (50V) as detailed on the circuit diagram. The signal is buffered by voltage follower IC2 and amplified by a factor of 100 in the non-inverting operational amplifier IC3. VR4 is used to adjust the amplifier gain to suit the fullscale range of the analog-to-digital converter. The inverting input of IC3 accommodates the OFFSET control by providing a D.C. offset of +1,5 to -1,5 times the range of the amplifier. The amplifier output is 0V to -5V approx. for a fullscale input and this output is level-shifted to +2,5V to -2,5V by R114 and R117 for use as an internal trigger signal.

4.3.2 Trigger Circuit

The trigger circuit input consists of a high impedance source follower FET TR4 with VR2 adjusted on test to remove any gate/source offset voltage. The trigger signal is derived either from the preamplifier as described above or from an external source when it is attenuated by a factor of 2 to match the +2,5V to -2,5V dynamic range of the trigger comparator IC1, a $\mu 710C$ with approximately 300mV hysteresis, and trigger threshold controlled by the front panel potentiometer. The correct slope is selected via the D.C. level - VE TRIG which causes E6/6 to invert the $\mu 710C$ output when negative going signals are to trigger the recorder. When positive slope triggering is selected -VE TRIG is low and E6/6 does not invert. E6/8 acts as an OR gate for the analog trigger, the rear panel digital trigger and the MANUAL TRIGGER pushbutton.

4.4 TRACK/HOLD CIRCUIT AND ANALOG-TO-DIGITAL CONVERTER

4.4.1 Track/Hold Circuit

The signal from the preamplifier is digitised at regular intervals at a rate controlled by the Sweeptime control. The analog-to-digital converter takes 2,5 microseconds to complete a digitisation and during this time the signal input to the converter must be held at one value for accurate digitisation. The track/hold circuit comprising FET TR7, IC4 and capacitor C71 does this. In between digitisations, drive transistor TR6 is turned on which keeps FET TR7 on so that the circuit tracks the signal with C71 being kept at signal potential. When a digitisation is to occur TR6 is turned off which turns off FET TR7 to isolate C71 from the preamplifier. The sampled signal is then held steady at the track/hold output for the duration of the analog-to-digital conversion cycle. The approximate 150mV offset apparent between tracked and untracked signal at IC4 pin 6 is a normal feature of this circuit configuration (see Figure 6-3).

4.4.2 Analog-to-Digital Converter

The analog-to-digital converter operates on the successive approximation principle whereby a series of binary weighted reference currents are summed until the current produced exactly equals the current produced by the sampled signal. The converter comprises the reference current network in the form of an integrated circuit IC5, discriminator IC6, the conversion registers IC's F8, F9, F10, F11 and control gates H9, H10 — shown on Figure 6-13. The associated control logic is shown on Figure 6-14 and comprises IC's E7, F7 and parts of IC's D5, D7, F5, J7.

A conversion is initiated when the timebase output sets SAMPLE (SWEEP initiates only the first conversion in a record) which in turn sets SYNC causing TRACK to go low whence the track/hold circuit maintains its output in a steady state. Flip flop $\div 2$ allows the track/hold transition time to settle and then CONVERT is set which gates the 3 MHz timebase output to generate ADC CLOCK. The sequence is illustrated by timing diagram Figure 4-2.

The negative transition of TRACK resets the conversion register via gates E8/3, 8, 11. This switches in the first, most significant current whence DISC at E8/6 will go high or low to indicate whether this current is less than or greater than that generated by the signal. Initially ADC CLOCK pulses ripple right through gates H10 and H9 and each pulse first switches the high order register bit according to DISC and then sets the next low order register bit to switch in the next lowest current. This also prevents ADC CLOCK pulses switching the already-used higher order bits which now contain the partial result of the on-going conversion. Finally the least significant bit CR1 is set and another discrimination is made whereby CR1 will remain set or will be reset by the next ADC CLOCK pulse. This latter terminates the conversion by clocking CR1 to reset the CONVERT flip-flop which resets SYNC which in turn resets SAMPLE. The result of the conversion now resides in the conversion register ready for storage in memory whilst the track/hold circuit switches back to the tracking mode.

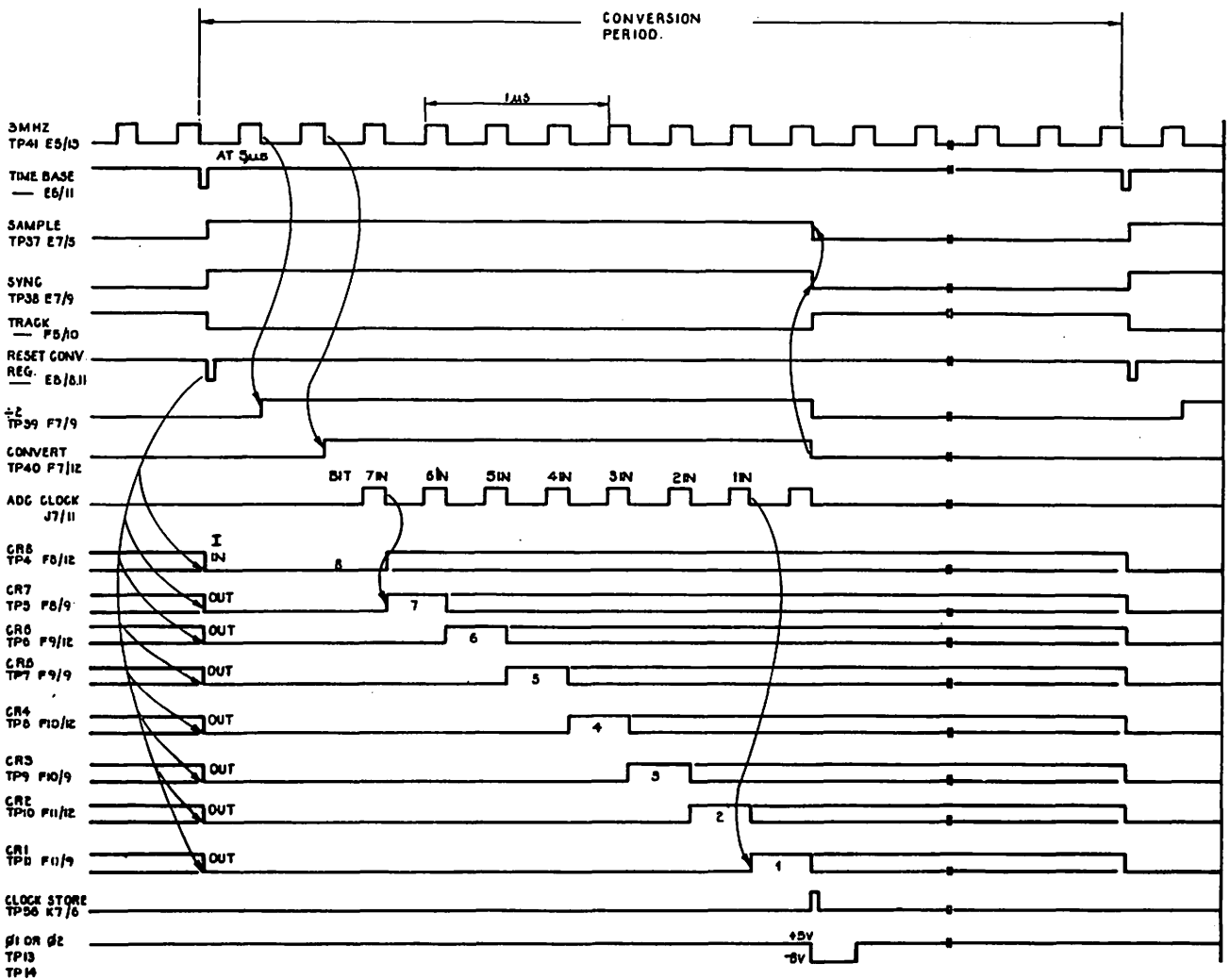


Figure 4-2 Timing Diagram — Analog-to-Digital Conversion

4.5 MOS MEMORY & Y DIGITAL-TO-ANALOG CONVERTER

4.5.1 MOS Memory

The DL901 memory comprises eight 1024-bit MOS dynamic shift registers — one for each bit of the eight-bit analog-to-digital converter. Each of the 1024 eight-bit conversions is presented to the store and clocked into it by one of the two clock pulses $\emptyset 1$ or $\emptyset 2$. The data input to the memory is via two quad two-input multiplexer IC's H8 and H11. Each input is connected to a bit of the analog-to-digital converter conversion register and the multiplexer outputs are fed into the shift registers. The shift register outputs are terminated by a second pair of multiplexers K8 and K11. These serve both as an MOS/TTL interface and also permit gating of external data into the memory — this is reserved for use on special systems, all production units have these inputs grounded. The outputs from the second set of multiplexers are fed back round to the other inputs of the first set of multiplexers to form a recirculation path for data in the shift registers. The memory input multiplexers are switched by $\overline{\text{ADC IN}}$ which, when low, gates the analog-to-digital converter words through to the shift registers. When high, $\overline{\text{ADC IN}}$ causes the memory output to be gated through to its input so that it can be recirculated for readout, display, plot, etc.

The 250 nanosecond high level clock pulses $\emptyset 1$ and $\emptyset 2$ switching from +5V to -8V are generated by a monolithic dual clock driver IC7. The CLOCK STORE signal initiates each memory cycle via IC's K6 and J7 which function as a demultiplexer producing $\emptyset 1$ and $\emptyset 2$ pulses alternately. Each pulse reads and writes one bit of data into each shift register — the negative transition shifts data through the register one place putting new data on the output whilst the positive transition writes new data into the register.

The parallel data from the memory is in negative true, binary code and is set into the output buffer register IC's K9, K10 by STROBE STORE. The output buffer register drives both the digital output interface and the Y display digital-to-analog converter.

The STORE OUT and ENABLE BUFFER signals are used to ensure that only coherent data is displayed during recording sweeps, both being high for data to be read out.

4.5.2 Y Digital-to-Analog Converter

The Y digital-to-analog converter has its eight-bit digital input driven by the memory output buffer register. The digital data switches a set of eight binary weighted currents, via diode switches D26-D49, into a summing junction to produce a current proportional to the data. The three most significant currents are adjustable by potentiometers VR5-VR7 whilst a single potentiometer VR8 controls the weight of the three least significant currents. The digital-to-analog converter current output is amplified by the discrete amplifier comprising TR9 and TR10 which is buffered by emitter follower TR8 to produce a +0.5V to -0.5V fullscale output at the Y and Ys rear panel sockets. The Ys display output has a two-microsecond RC time constant to effect smoothing. The Y output is also switched by a reed relay to the Y Plot output. In the plot mode PLOT FLAG goes high to energise the relay coil and close its contacts — at the end of the plot mode PLOT FLAG returns low and the relay contacts open to isolate the Y Plot output from the digital-to-analog converter.

4.6 OUTPUT INTERFACE (See Figure 6-16)

4.6.1 General

This interface is contained on a plug-in circuit card mounted in a connector on the underside of the main circuit card. (Note that when replacing this card, or any optional interface, that the components face the lower cover panel.) The standard interface card contains a general purpose TTL logic level interface by which an external digital device can access the DL901 memory to read out the stored record. The eight binary data lines are buffered and all the J1 rear panel signals are routed via the interface card which also contains the plot mode initiating logic.

The interface card position is also used for the various 900 series optional interfaces, e.g. 900/ASCL, 900/TTY, etc. These cards replace the standard card and duplicate common circuits in addition to providing the special circuits required by each option. These optional interfaces are documented separately.

4.6.2 Punch Mode

The DL901 must be in the single trigger mode and in the quiescent display state (CYCLE J1/20 = 0, PLOT FLAG J1/15 = 0) for the interface to operate. Other trigger modes will inhibit the functioning of the interface and selection of them during output will terminate the readout process. An armed condition will be cancelled when output starts. To enable the initiation of output, DIGITAL OUTPUT ENABLE (J1/19) must be grounded. This signal is used as a 'device present' signal and may be activated either by the device when it is ready (e.g. power on), or, more simply, by a link to 0V (J1/12) in the interface cable. This signal is intended to prevent accidental initiation of the interface logic and consequent "lock-up" when a device is not present.

Once the DIGITAL OUTPUT ENABLE is 0 then digital readout may be initiated by either

- (a) momentarily operating the PUNCH/PLOT lever on the Front Panel,
- or (b) applying a 1 to 0 transition to DIGITAL OUTPUT REQUEST (J1/24).

The output sequence starts within 1,024 milliseconds; this is indicated by an 0 to 1 transition of DIGITAL OUTPUT FLAG (J1/18). DIGITAL OUTPUT REQUEST can now be returned to 1 if desired. DIGITAL OUTPUT FLAG remains at 1 for the whole of the readout. The first word is automatically placed on the output lines within 1,3 microseconds and an 0 to 1 transition by DATA READY (J1/17) indicates valid data. This 0/1 transition may be used to strobe data at the receiving device. To read out further words the WORD REQUEST (J1/23) is used; a 0/1 transition causes DATA READY to go to 0 within 0,1 microseconds, indicating that WORD REQUEST was received. In an interlocked, handshaking interface the DATA READY 1/0 transition is used to return WORD REQUEST to 0. Alternatively, WORD REQUEST may simply be a positive pulse greater than 0,1 microseconds wide. Providing WORD REQUEST is applied at greater than 1kHz, DATA READY will occur within 1,3 microseconds; thus the readout rate may be controlled at any speed between 1,3 microseconds and 1 millisecond per word. When more than 1 millisecond elapses between successive WORD REQUEST pulses, new data will not be readout for up to 1,024 milliseconds after the request; further requests occurring during this period are ignored. If, at the end of the 1,024 milliseconds latency period, WORD REQUEST signals are applied within 1 millisecond of one another, the 'fast' mode will be automatically restored.

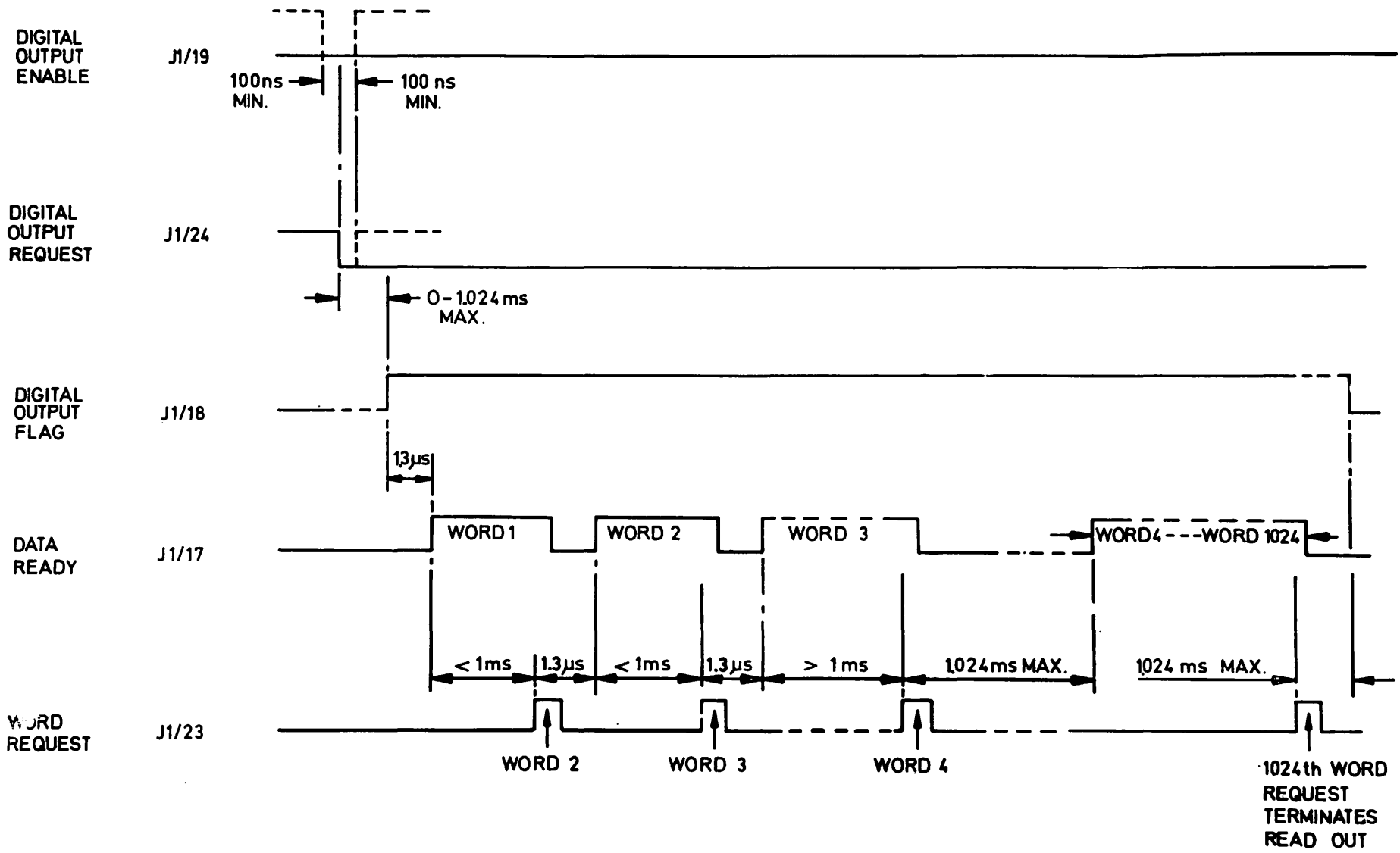
The readout continues until all 1024 words have been output, whereupon the next WORD REQUEST terminates the Punch mode and DIGITAL OUTPUT FLAG makes a 1/0 transition to indicate this. Timing diagram Figure 4-3 illustrates the interface timing sequence.

Referring to Figure 6-16, the eight data bits from memory are buffered through inverter pairs prior to connection to J1 and data is present in all readout modes, i.e. Punch, Plot and display modes. The Front Panel PUNCH switch or DIGITAL OUTPUT REQUEST sets REQ when DIGITAL OUTPUT ENABLE is low. Meanwhile the DL901 memory is cycling in the display mode and when the last word is accessed AC10 clocks REQ to set PUNCH. The PUNCH flip flop signals to the main control logic and the readout sequence starts. The positive edge of STROBE STORE sets data into the memory buffer register whilst its negative edge sets DRS to put DATA READY high. The front edge of WORD REQUEST resets DRS via gates H3/10, 13 and control logic responds to DRS reset by fetching the next word from memory and setting DRS again. After the last word has been output main control logic resets PUNCH and REQ to terminate the readout and the DL901 returns to the display mode. PUNCH and PLOT flip-flops are interlocked to prevent simultaneous selection. The PUNCH mode is described further in subsection 4.8.10.

4.6.3 Plot Mode

This mode is similar to a slow display mode. The DL901 memory is recirculated continuously and successive words are taken out and converted to analog form; the digital record is reconstructed into its analog equivalent at a speed suitable for a Y/t recorder. The Plot mode is initiated by operating the Front Panel PLOT switch. The display mode will be terminated when AC10 goes low at the end of the memory cycle and PLOT is set. Main control logic clocks the memory at the display rate of 1MHz but STROBE STORE occurs at the selected Plot Rate (see subsection 4.8.9), and hence data is taken from the memory at a slow rate. During this process PLOT FLAG is high causing the Y Plot output to be connected to the digital-to-analog converter. After word 1000 has been output PLOT FLAG goes low to isolate the Y Plot output and control logic clocks the memory through to the last word when RPP resets PLOT and the DL901 returns to the display mode. The Plot mode is described further in subsection 4.8.9.

The standard plot rate is 200 milliseconds per word. Alternative rates from 20 milliseconds per word to 5 seconds per word are available. See the Operating Manual for details of how to change the plot rate.



(NOT TO SCALE)

Figure 4-3 Timing Diagram — Digital Output Mode

4.6.4 DL901 Transient Recorder J1 Connections

J1 – 24 Way Amphenol connector – Mating plug 57-30240

All signals are TTL/DTL compatible. Logic 0 = 0V to +0.8V.

Logic 1 = +2.5V to +5.0V. Risetimes \geq 100ns. Pulse widths \leq 100ns.

<u>Pin</u>	<u>Signal</u>	<u>Use</u>
1	—	Spare
2	DIGITAL ARM	1/0 transition arms 901
3	DIGITAL TRIGGER	1/0 transition triggers 901 when trigger slope switch set to - 0/1 transition triggers 901 when trigger slope switch set to + To use this facility select External trigger mode, D.C. coupling and set trigger level fully anti-clockwise. Most significant bit 2^7 .
4	BINARY DATA BIT 8	
5	BINARY DATA BIT 7	
6	BINARY DATA BIT 6	
7	BINARY DATA BIT 5	
8	BINARY DATA BIT 4	
9	BINARY DATA BIT 3	
10	BINARY DATA BIT 2	
11	BINARY DATA BIT 1	Least significant bit 2^0 .
12	0V	Instrument ground
13	—	Spare
14	—	Spare
15	PLOT FLAG	1 when 901 is in Plot mode — otherwise 0.
16	—	Spare
17	DATA READY	1 indicates valid data on B1-B8 lines during Digital Output.
18	DIGITAL OUTPUT FLAG	1 indicates Digital Output mode in progress.
19	DIGITAL OUTPUT ENABLE	Apply 0 to enable initiation of Digital Output sequence.
20	CYCLE	1 indicates recording in progress.
21	—	Spare
22	EXTERNAL ADVANCE	+4V pulse (no risetime limit) takes sample, advances memory one point. Rates 200kHz to 1kHz infinitely variable. Rates < 1kHz may incur 1,024ms latency before recorder will obey next command.
23	WORD REQUEST	0/1 transition requests new data in Digital Output mode (Punch). Rate infinitely variable from 1,3 μ s/word to 1ms/word. Rates < 1kHz may incur 1,024ms before data is ready. No risetime limitation.
24	DIGITAL OUTPUT REQUEST	1/0 transition initiates Digital Output mode after 1,024ms maximum delay. — No risetime limitation.

4.7 TIMEBASE, DELAY GENERATOR & ADDRESS LOGIC

4.7.1 General

The crystal-controlled timebase logic provides pulse trains, at preselected rates, to define the DL901 sampling rates, delay periods, memory recirculations speed and plot rates. Refer to Figure 6-14.

4.7.2 Timebase

A 3MHz crystal-controlled oscillator provides a basic 3MHz clock, at Test Point 41, which is used to control the analog-to-digital converter. The 3MHz is divided further to provide a 1 microsecond period used to control the memory clocking rate in display, plot, 2-200 second recording sweeps and recirculation modes. A chain of $\div 5/\div 10$ decade counters (IC's B1, 2, 3, C1, 2, 3) produces five basic timebase outputs of 5 μ s, 50 μ s, 500 μ s, 5ms and 50ms. These counters plus the output from two further decades (IC B4) provide a variety of plot rates from 20ms to 0.5s.

A 2ms signal is generated whose positive-going edge (at 1ms) controls the minimum clocking rate for the MOS shift register memory. Similarly the positive-going edge (at 0.1s) of the 0.2s output is used to generate the auto-trigger rate. A three-bit digital code, SA, SB, SC generated by the SWEEP TIME switch is used to select one of the five basic time-base outputs via multiplexer IC A2. Further subdivision of the selected rate is controlled by IC's A3, A4 under control of a two-bit code SX, SY also generated by the SWEEP TIME Switch. This second divider operates at $\div 1$ when $SX=SY=1$, $\div 2$ when $SX=1$ $SY=0$ and $\div 4$ when $SX=SY=0$. The \bar{Q} output of IC A3/13 thus provides the desired sampling rate ($SWEEP\ TIME \div 1000$) which via IC E6 controls the analog-to-digital converter word rate.

The SA, SB, SC, code from the SWEEP TIME Switch is decoded by gates A1/6,8 to indicate when external control of the sample rate is selected — the external source is routed through multiplexer IC A2 and the EXT/\bar{EXT} levels indicate the requirement to control logic and also ensure that IC A3 is in the $\div 1$ mode. Decoding by gate A1/12 produces a 0 for \bar{CIRC} indicating that a sweep time requiring continual memory recirculation has been selected. During sweeps of 2-200 seconds the memory is continually recirculated at a fixed $1\mu s$ rate and samples are input at the appropriate place in the memory.

4.7.3 Delay Generator

The delay is controlled by a single decade lever switch generating a negative true 8-4-2-1. BCD code — $\bar{D}8, \bar{D}4, \bar{D}2, \bar{D}1$ are the code designations. The inverted code is set into the synchronous decade counter B6 by the \bar{Q} output of the ARM bistable. SAMPLE or SYNC provide the count input via IC's C6, D6 connected as a $\div 100$ circuit — hence the 100 sample increments for the delay facility. The $\div 100$ output counts B6 down through zero to underflow whence the DELAY bistable is clocked by the synchronous counter MAX/MIN output 1/0 transition.

In the delayed recording mode, the B6 MAX/MIN output clocks the SWEEP flip-flop set, thus acting as a trigger-initiated delay between trigger and recording sweep.

In the PreTrigger recording mode B6 MAX/MIN output resets SWEEP flip-flop to terminate recording — i.e. the end of PreTrigger recording is delayed.

4.7.4 Address Logic (Figure 6-15)

IC's L7, M7 and N7 form a 10-bit binary counter used to indicate the store addresses. It is incremented by the negative transition of the \bar{Q} output of the CLOCK STORE monostable. Initialisation to zero is by the RESET ADDRESS signal and the A.C. outputs are decoded to indicate word 1000 ($\bar{AC}1\bar{K}$ low) for the display and plot modes. The 1/0 transition of AC10 is used to detect when the last word of store has been clocked and gates H7, K5 produce AC10P for use by the control logic.

The 10-bit binary N counter comprising IC's L5, M5 and N5, is used to track data in the memory when it has to be recirculated in between record samples or readout strobes; the N counter holds the data word address whilst the AC counter is incremented as each word is shifted through the memory. A comparator comprising gates L6, M6, N6, and diodes D1-D10 compares AC and N and indicates equality by putting $\bar{AC}=\bar{N}\bar{C}$ low. N is incremented by the negative transition of +1TN when the store is accessed e.g. indirectly by WORD REQUEST in the Digital Output mode; then the comparator is used to detect when the desired address is reached.

Alternatively, if N is left at a value then the comparator will indicate each complete store recirculation. In the readout modes N counter overflow via N10 indicates that all stored data has been output. The further use and control of $AC=N$ is discussed in subsection 4.8.5.

4.8 CONTROL LOGIC (Figures 6-14, 6-15)

4.8.1 General

The control logic circuits are positioned on the right-hand side (viewed from front) of the main circuit card and are responsible for initialisation, trigger synchronisation, delay time and sample rate generation, analog-to-digital converter and memory control and display, plot and digital output mode operation.

4.8.2 Display

When not recording or outputting (Punch/Plot) the DL901 is in its display mode. The store is clocked at 1MHz and the CRO TRIG and Z signals are generated in synchronisation with the start of the record readout. This process is shown on Figure 4-4.

Referring to Figure 6-15, DIS=1 at gate J3/4 selects the 1 μ s timebase output at J5/8 to generate clock store pulses via mono K7. In the display mode- or when a two-second or slower record sweep is in progress — the Z flip-flop J input is high when AC10 is low. Thus, 1 μ s clocks Z set to produce high level Z mod signals and the CRO TRIG via the mono comprising gates P2/6, 8. The display used in conjunction with the continuous monitoring feature (pre-trigger recording with sweep times > 1 second) is triggered differently as explained in subsection 4.8.8.

In all displays — gates N2/6 and M2/8 produce STROBE STORE pulses to set the store data into the output buffer register to drive the Y axis digital-to-analog converter. After word 1000 has been displayed $\overline{AC1K}$ is low and 1 μ s clocks Z reset preventing the last 24 words of memory from being strobed out. The display process is repeated until it is interrupted either by a recording sweep or a Plot/Punch request.

4.8.3 Arm & Trigger

Arming the DL901 for a recording sweep is controlled by the ARM flip-flop shown in Figure 6-14. The recorder can only be armed when it is in the display mode; in SINGLE trigger mode the ARM switch or a DIGITAL ARM pulse sets the ARM flip-flop via gate D7/6. When recording starts DIS goes low to prevent further arm signals during recording.

When CONT or AUTO triggering is selected ARM is set by the first AC10P after each recording sweep — this ensures at least one display cycle between recordings. Once the DL901 is armed it is triggered by using the TRIGGER to reset ARM and the resultant TRIG P or change in ARM and \overline{ARM} levels are used to initiate subsequent logic. The trigger circuit output is inverted or not inverted by exclusive OR gate E6/6 depending on the trigger slope (+/-) switch setting — thus the desired slope of the trigger signal may be selected to reset ARM. Alternatively a remote DIGITAL TRIGGER can reset ARM — the trigger slope control is effective. A third means of triggering the recorder is operation of the front panel MAN TRIG pushbutton which is a wired OR with DIGITAL TRIGGER facility. In the AUTO trigger mode the Timebase .2S output resets ARM — which can still be reset by regular triggers when the DL901 is armed.

In the DEL'D SWEEP mode the recorder is armed to accept a trigger to start recording, whereas in the PRE TRIG sweep mode the recorder starts recording when armed and a trigger initiates the end of recording. These modes are described in the following subsections; the DEL'D SWEEP mode is also used to explain the detailed operation of the External Advance and store recirculation functions.

4.8.4 Delayed Sweep Recording (DEL'D SWEEP)

The occurrence of a trigger resets ARM to produce TRIG P the initialising pulse which resets the DL901 logic from the display mode to the recording mode via the reset signals \overline{RX} , RESET ADDRESS and RESET TB. Figure 6-14 shows \overline{RX} , at gate E5/4. The 0V to +5V RC combination at gate A 7/8 is used to provide a 'power on' reset whilst the R,C, diode combination on pin 9 of gate A7/8 applies a reset when the DEL'D SWEEP/PRE TRIG mode switch is switched from DEL to PRE TRIG during the CONT trigger mode. This prevents logic lock-ups due to misoperation.

Referring to Figure 4-5 the delayed sweep mode starts with a pre-sweep delay and follows with the recording sweep. Consider now that the recorder is set in DEL'D SWEEP mode, delay =3 and sweep time = 10ms; the recorder was armed and a trigger has occurred. TRIG P initiates the DL901 logic and simultaneously sets the DELAY flip-flop via gate E4/6. During the arm phase prior to the trigger, ARM =1 has forced a permanent load condition on the Delay Counter formed by IC's D6, C6 and B6 thus resetting the $\div 100$ stage and setting B6 to 3. Triggering puts ARM =0 removing the counter load condition.

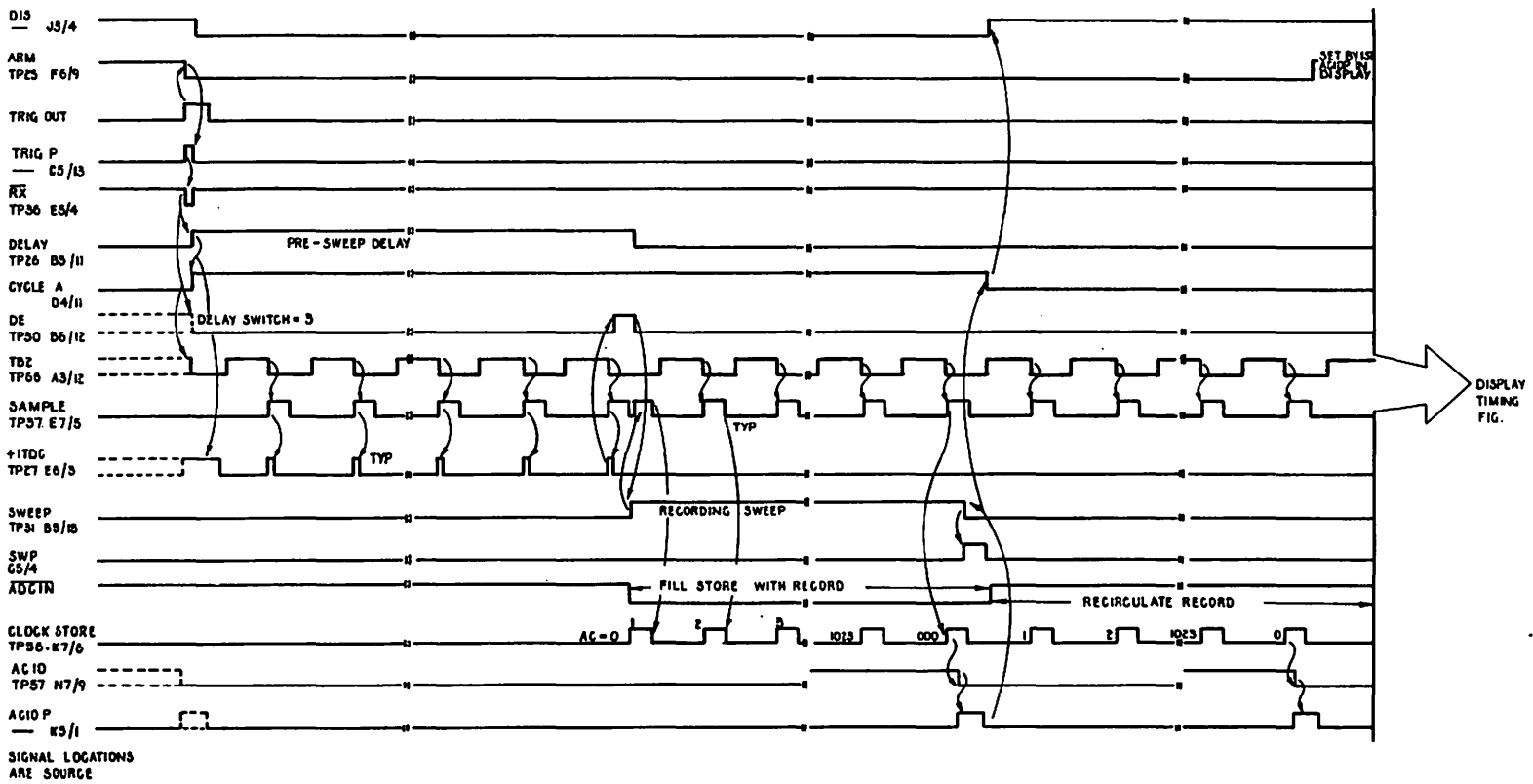


Figure 4-5 Timing Diagram — Delayed Sweep

The I/O transition of $\overline{\text{DELAY}}$ is used to provide the first count pulse via gate E6/1 — this allows zero delays to be executed in the same way as non-zero delays. The SAMPLE flip-flop E7 is now being clocked by the timebase output A3/13 and the SYNC 0/1 transition via gate F3/8 increments the Delay Counter. The timebase is running at $10\mu\text{s}$, being divided by 100 via counters C6,D6 thus causing B6 — originally set to 3 — to be decremented at a 1ms rate until after 3ms, B6 underflows and its MAX/MIN output 1/0 transition resets the DELAY flip-flop which sets the SWEEP flip-flop. SWEEP via gates D4/3/6 puts $\overline{\text{ADCIN}}$ low to gate the analog-to-digital register content into the store; gate F3/6 is used when the store is recirculated between sample insertions. SAMPLE causes the TRACK/HOLD/ADC CLOCK process to commence as shown in Figure 4-2.

The STORE OUT flip-flop was reset by $\overline{\text{RX}}$ and remains low until the memory has been clocked 1024 times — AC10P sets STORE OUT. This facility is only of use in sweep speeds where the store is displayed whilst recording — it produces a coherent display of new data filling the empty store. Figure 6-15 shows gate J5/3 producing pulses to CLOCK STORE mono K7 — SAM the logical “AND” of SAMPLE and SWEEP flip-flops is gated by STATIC which is high since RECIRC and CIRC are low at gate E3/3.

Now the store, AC and N counter (via gate H5/8) are being clocked at the $10\mu\text{s}$ timebase rate. This continues until 1024 samples have filled the store and AC10P resets SWEEP through gate H3/12. $\overline{\text{ADCIN}}$ returns high so that the stored record may be recirculated in the store — gate D4/3 provides a trailing edge delay to ensure $\overline{\text{ADCIN}}$ remains low until the last sample is stored. SWEEP going low causes CYCLEA to go low and at gate J3/4 DIS goes high selecting the $1\mu\text{s}$ pulse train to clock the store in the display mode. The store recirculates in the display mode at 1MHz and after one recirculation AC10P re-arms the recorder if CONT triggering is selected — the display continues until the next trigger.

4.8.5 Recirculating Sweeps

For sweep times greater than 1 second the store is not clocked at the sample rate; the dynamic MOS shift registers can lose data at shift rates below 1kHz. Therefore, with sweep times between 2 and 200 seconds the store is clocked at a 1MHz rate and words from the analog-to-digital converter are inserted at the appropriate times in the store recirculation. During these sweep speeds the display mode is operative showing the store filling with new data. The SWEEP TIME switch outputs SA, SB, SC are decoded by gate A1/12 to produce $\overline{\text{CIRC}}=0$ when sweep times 2-200 sec are selected. Via gate E3/3 $\overline{\text{CIRC}}$ low puts $\overline{\text{STATIC}}$ high. This puts the J input of Z flip-flop high causing the production of the display Z, CRO TRIG and STROBE STORE signals. CIRC = 1 via gate H7/6 selects the $1\mu\text{s}$ signal to clock the store.

The sample rates are not integral multiples of the 1,024ms recirculation time and therefore data is inserted into the store in an asynchronous manner shown in Figure 4-6.

The analog-to-digital converter and N counter are pulsed at the sample rate but $\overline{\text{ADCIN}}$ is controlled by gate F3/3 which only puts $\overline{\text{ADCIN}}$ low when AC = N occurs in this CIRC mode, i.e. by comparing N with AC, the correct place in the store recirculation may be found at which time $\overline{\text{ADCIN}}$ is put to 0, so that the analog-to-digital converter register content is clocked into the store on the current store cycle. Gate M4/3 allows SAM (SAMPLE.SWEEP) to set TS flip-flop which causes $1\mu\text{s}$ to clock AACN thus allowing NOR gate J3/10 to invert $\overline{\text{AC=NC}}$ to produce AC=N. When the correct point in the store recirculation is reached AC = N goes high and the next $1\mu\text{s}$ will reset TS and AACN after first allowing AC = N to be used as described above. The process continues until the store is completely filled when AC = N and AC10P coincide. Both AC and N counters are at overflow — then the SWEEP flip-flop is reset via gates F3/6 and H3/12.

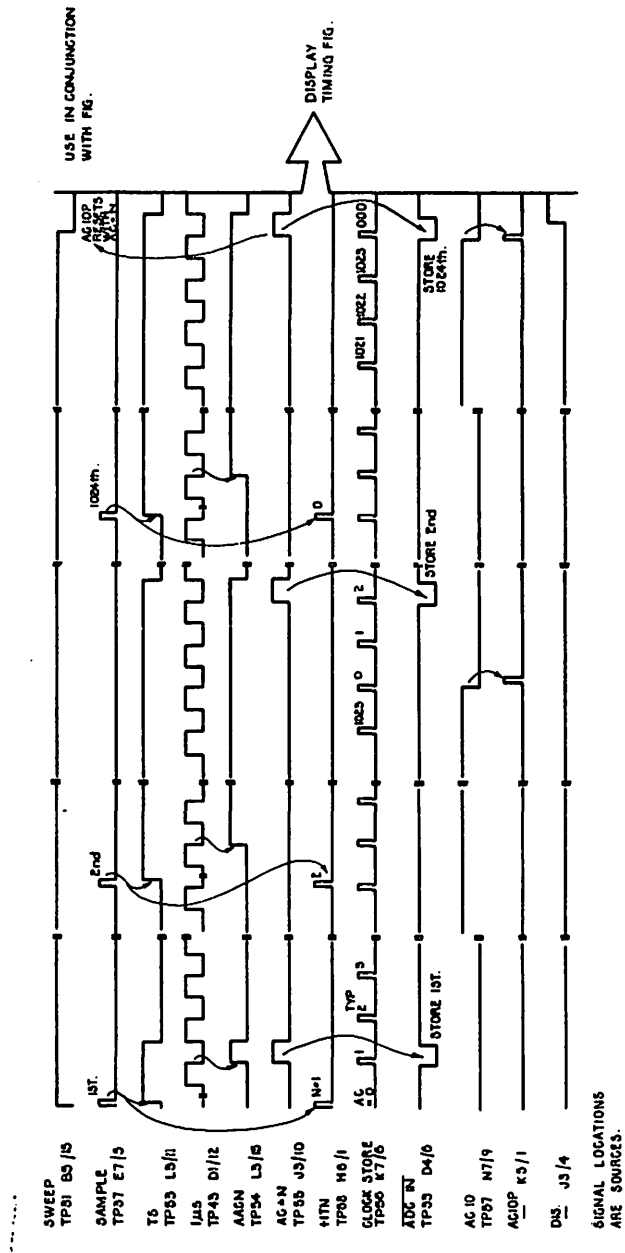


Figure 4-6 Timing Diagram – Recirculation (2-200s Sweeps)

4.8.6 External Advance

The SWEEP TIME control EXT position allows the record sampling rate to be controlled by an external pulse train EXT ADV connected to rear panel socket J1/22. At sample frequencies from 200kHz to 1kHz, the store is clocked at the advance rate. Below 1kHz sample frequencies the store has to be protected against data loss by enforced recirculation. At the end of an enforced recirculation the recorder pauses for 1ms during which time it can immediately respond to an external advance pulse. If no pulses occur within the 1ms then a further recirculation will be enforced. The process of enforced recirculation and pausing may continue indefinitely.

The input signal is sampled and converted at the time of application of the external pulse; the first such pulse occurring during a recirculation causes sampling and digitisation; all further external pulses are ignored and the digitised sample is stored at the end of the recirculation. Each sweep requires the acceptance of 1024 pulses for its completion. The digital delay facility is also controlled by the external advance pulse train. Gates A1/6,8, decode the SWEEP TIME switch SA, SB, SC outputs to put EXT low and EXT high when the EXT position is selected. The External Advance input is buffered via TR5 and passed through the multiplexer and the TB1, TB2 dividers which are both in the ÷1 mode. Thus, the external pulses clock SAMPLE to count delays, initiate conversions and store cycles. Each CLOCK STORE produces a RESET TB via gate K4/11 thus the timebase is reset so that it can be used to detect static periods greater than 1ms; Figure 4-7 illustrates the sequence.

So long as the advance rate is 1kHz or more the recording sweep functions in the same manner as the internally-timed sweeps of 1 second or less. When the rate falls below 1kHz the 2ms 0/1 transition sets TS through gate L4/8 to enforce a store recirculation; RECIRC goes high to gate 1µs at J5/8 to clock the store and AACN is set to allow AC=N to indicate recirculation complete. In the absence of external pulses AC=N going high will cause TS and AACN to be reset.

An external pulse during recirculation will set SAMPLE which will not reset whilst RECIRC is low at gate F5/13 — this prevents N counter incrementing during a recirculation. After the recirculation is complete RECIRC goes high to reset SAMPLE which increments N and clocks the store to write in the latest digitised sample — ADC IN goes low when RECIRC is high. STATIC is high whenever RECIRC is low and effectively switches the logic between the 1-second and 2-second modes. When low, STATIC also causes the display logic to function as previously described.

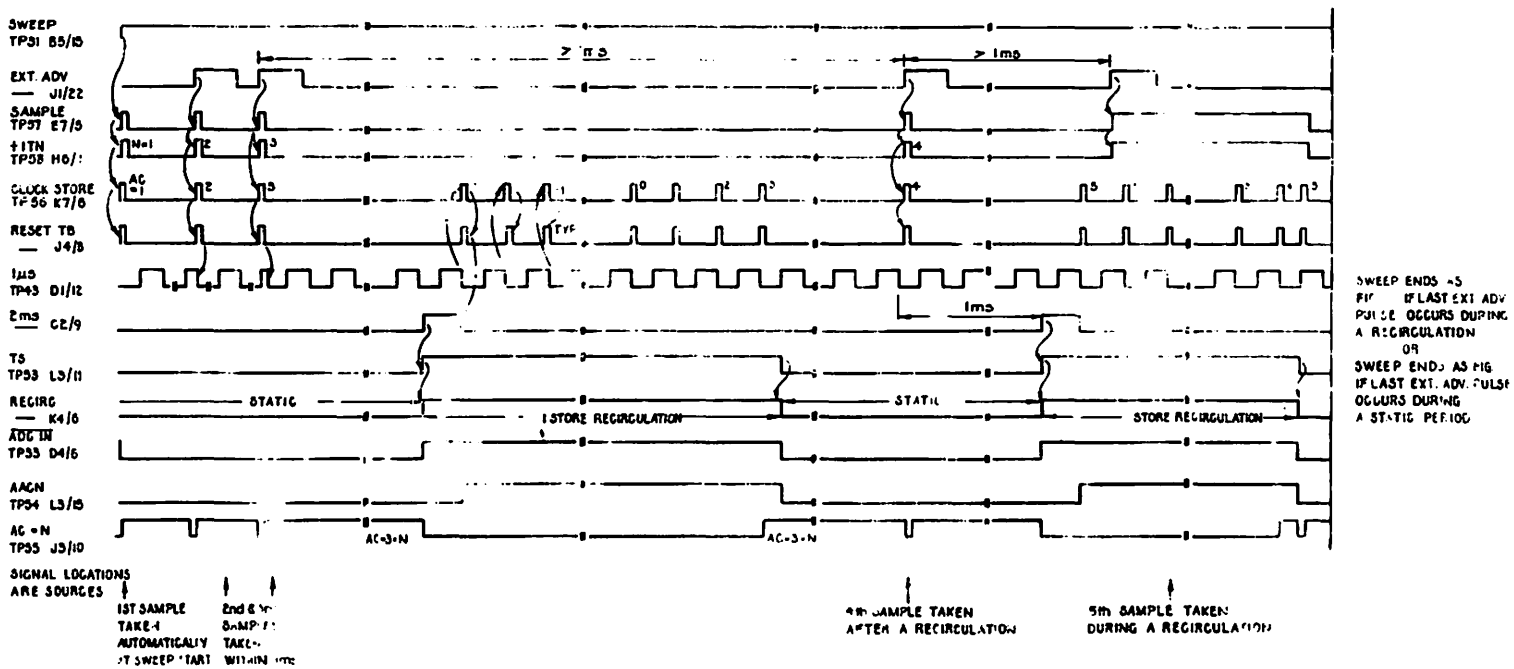


Figure 4-7 Timing Diagram — External Advance

4.8.7 Pre-Trigger Recording (PRE TRIG)

This mode enables the recording of data that occurs before the trigger. Figure 4-8 shows that recording at the preset Sweeptime rate commences when the DL901 is armed. The occurrence of a trigger initiates the delay logic which counts out the preset delay before terminating the recording sweep. Figure 6-14 shows ARM via gate E4/6 holding DELAY and SWEEP flip-flop set and forcing the Delay Counter in a load state. Thus, data is recorded as described previously at the preset sample rate — except that when the store is full the process continues with new data replacing old data.

The occurrence of a trigger resets ARM, TRIG P is not used and this removes the preset from the DELAY, SWEEP and Delay Counter flip-flops. Now each time a sample is taken it is counted via gates F4/6 or F4/12 until the required delay has been executed.

Then the counter B6 max/min output clocks the DELAY flip-flop reset which in turn resets SWEEP. The SWEEP 1/0 transition produces SWP, a pulse to reset the AC and N counters so that they are correct relative to the stored record. The DL901 will now be in the display mode. Note that whilst the pre-trigger mode can operate in the AUTO or CONT trigger modes, it is more normally used with SINGLE trigger due to its unique nature.

The generation and control of the 2-200 second recirculating sweeptimes and the External Advance facility in the Pre-Trigger mode are as described for Delayed Sweep recording.

4.8.8 Pre-Trigger Recording — Continuously Updating Display

When sweeptimes greater than 1 second are used in conjunction with Pre-Trigger recording a continuously updating CRO display can be obtained by not triggering the DL901. The CRO display waveform moves from right to left showing the introduction of new data and the loss of the oldest data. This display is achieved by a different process to that normally used in display. When SWEEP and PRE TRIG are 1, gate M2/3 prevents the Z flip-flop from being set and allows $\overline{AC=NC}$ 1/0 transition at gate N2/8 to produce CRO TRIG pulses.

STROBE STORE is produced each $1\mu s$ and now the CRO TRIG coincides with the newest sample in the store. The display shows a full 1024 samples without any Z blanking only in this unique configuration.

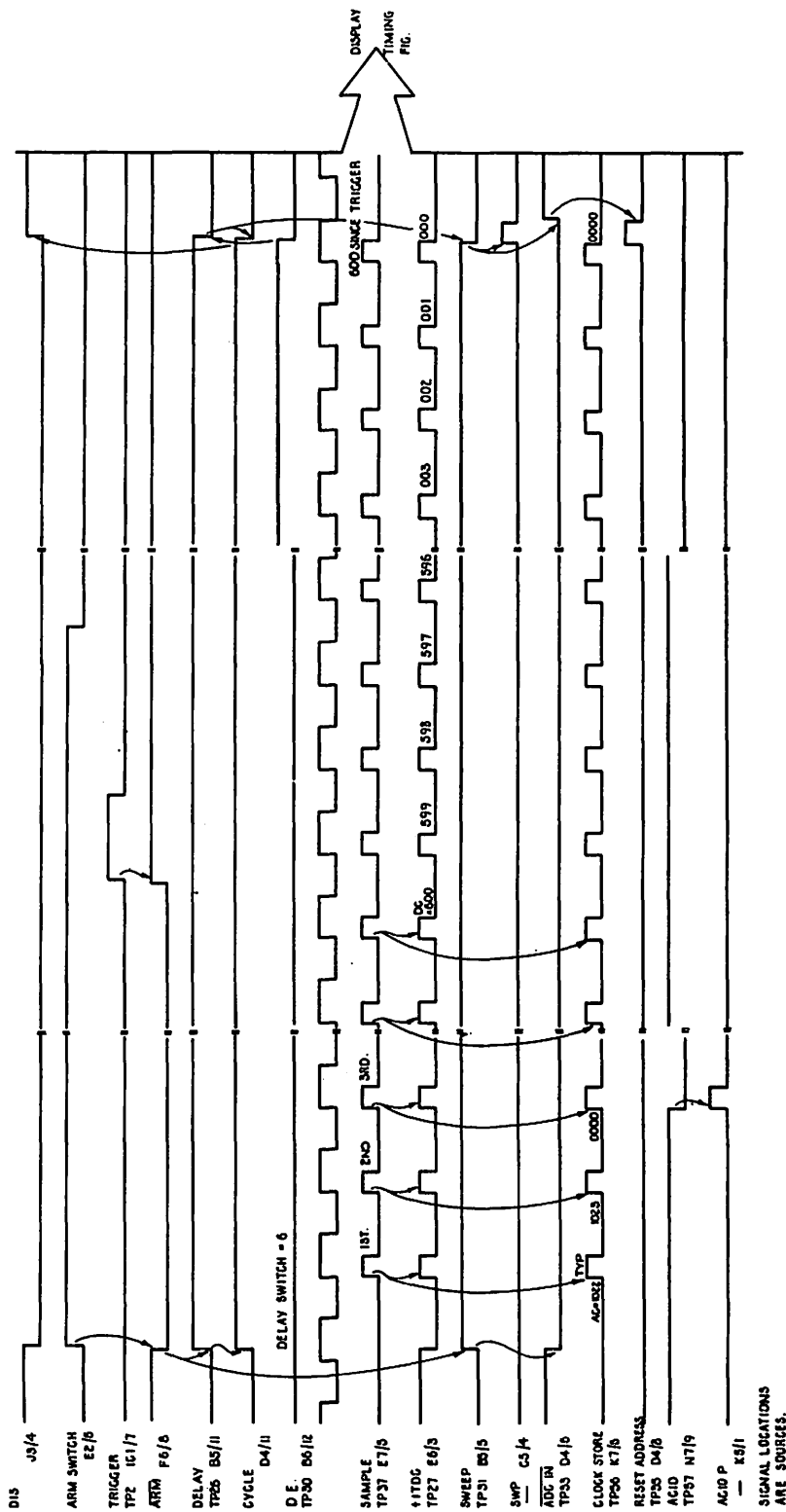


Figure 4-8 Timing Diagram – Pre-trigger Sweep (Sweep < 2s)

4.8.9 Plot Mode

In the Plot mode the store and AC counter are clocked at the 1MHz rate whilst the N counter, clocked at Plot Rate, is used to track data in the store and produce pulses to gate the data words into the output buffer register to drive a Y/t plotter via the digital-to-analog converter.

Figure 4-9 illustrates Plot mode timing. Operation of the PLOT switch sets PLOT on the interface card — see subsection 4.6.3.

PLOT puts OUTPUT high at gate P4/8 and the subsequent $\overline{\text{OUTPUT}}$ pulse sets Z. On the interface card Z puts PLOT FLAG high which energizes the Y Plot relay to connect the rear panel Y Plot socket to the Y digital-to-analog converter. The N counter is incremented by $\overline{\text{OUTPUT}}$ and the subsequent timebase plot rate pulses via gate M4/6. TS flip-flop is set when N is incremented and hence AACN enables AC=N to indicate correct words for output. Gate N2/12 produces STROBE STORE when AC=N goes high-N4/13 is high in the Plot mode. After 1000 words have been plotted $\overline{\text{AC1K}}$ low causes Z to be reset which puts PLOT FLAG low de-energising the PLOT relay to isolate the Y Plot output. The last 24 words of store are accessed at the plot rate then the N counter overflows setting NC10S which prevents further $\overline{\text{PR1}}$ pulses producing +1TN. The next $\overline{\text{PR1}}$ produces RPP at gate J4/12 which resets the PLOT flip-flop on the interface card and returns the recorder to the display mode and DIS resets NC10S.

Note that via gate J3/13 recording in progress (CYCLE = 1) or non-selection of SINGLE trigger mode also produces RPP. This can be a convenient way of stopping the PLOT mode early — by selecting CONT trigger — even though it rearms the recorder. An armed condition is cancelled when the Plot mode starts — gate E5/1 inhibits the effect of the subsequent TRIG P.

4.8.10 Punch Mode (Digital Output)

Subsection 4.6.2 describes the operational details of this mode, it allows a remote device to access digital data in the DL901 store at an externally-controlled rate. Various general purpose and specific interfaces exist — this explanation assumes the use of the standard TTL interface although the DL901 output logic functioning is constant for all interfaces.

New data is requested by the WORD REQUEST and its presence is indicated by DATA READY. To suit the widest possible range of peripherals the readout speeds are defined by the peripheral via the WORD REQUEST with only the minimum store clocking rate imposing a limitation. The store is controlled similarly to the External Advance recoding mode; it is clocked at the WORD REQUEST rate for rates between $1.3\mu\text{s}/\text{word}$ and $1\text{ms}/\text{word}$. Below 1ms word the store is automatically recirculated once for each 1ms period during which no WORD REQUEST occurs. A WORD REQUEST occurring during a recirculation is obeyed at the end of the recirculation.

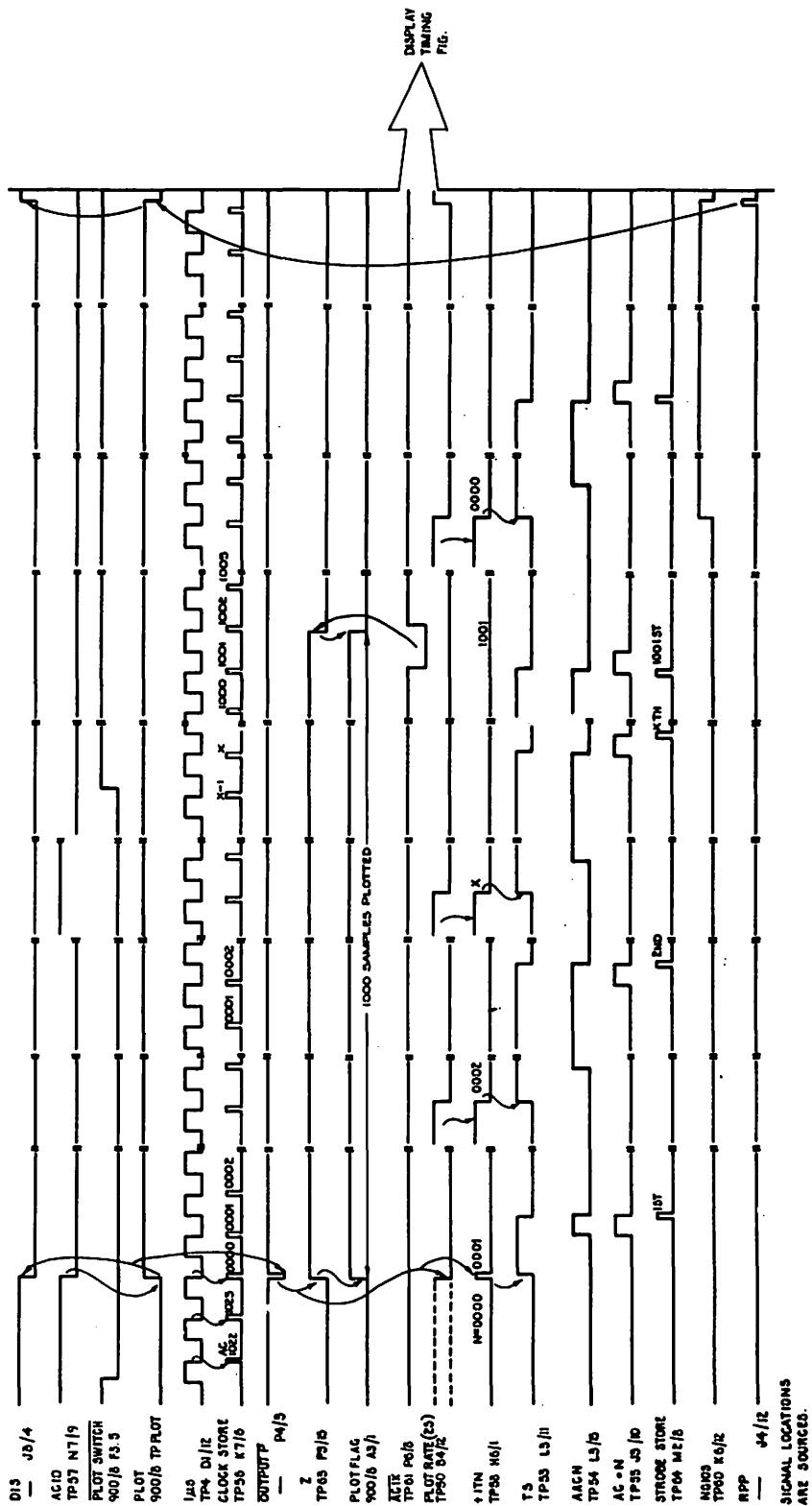
After OUTPUT REQUEST has set PUNCH on the interface card (See subsection 4.6.2) OUTPUT goes high at gate P4/8. Figure 4-10 shows the timing for this mode. The first word from store is output automatically, the remainder requires use of the WORD REQUEST. The PUNCH RATE flip-flop controls access of new data by sensing when DRS is reset by WORD REQUEST. Initially when PUNCH is set DRS is low and this causes gate H6/10 to set PUNCH RATE which resets to produce the +1TN pulse and CLOCK STORE to clock out word 1. The AC=N gate J3/10 is active since TS and AACN are reset which with L4/12 high holds K3/8 low, AC=N immediately goes high as AC and N counters both are 0001 and STROBE STORE is generated by gate N2/12, DATA READY is set and since being reset by the last CLOCK STORE the timebase counts toward the 1ms maximum static time for the store.

If WORD REQUEST occurs within 1ms DRS is reset and PUNCH RATE sets and resets to increment N and clock the store for word 2. Assuming WORD REQUEST does not occur within 1ms then the 0/1 transition of 2ms sets TS through gate L4/8 to cause an enforced recirculation of the store. AACN is set and $\overline{\text{RECIRC}}$ is low selecting $1\mu\text{s}$ to trigger CLOCK STORE and $\overline{\text{RECIRC}}$ prevents PUNCH RATE resetting if a WORD REQUEST occurs.

After the recirculation, PUNCH RATE resets to generate +1TN and CLOCK STORE to output the next word. The output sequence continues until the last word has been output and the N counter overflows to set NC10S. The last WORD REQUEST produces a PUNCH RATE which via gate H5/6 generates RPP to reset PUNCH and terminate the readout — the DL901 returns to the display mode.

NOTE

Optional interfaces plug into the interface card connector in place of P.C. 900/8 — interface connections being made via the J1 plug. These optional interfaces are documented separately.



900/8 INTERFACE CARD MUST BE FITTED

Figure 4-9 Timing Diagram - Plot Mode

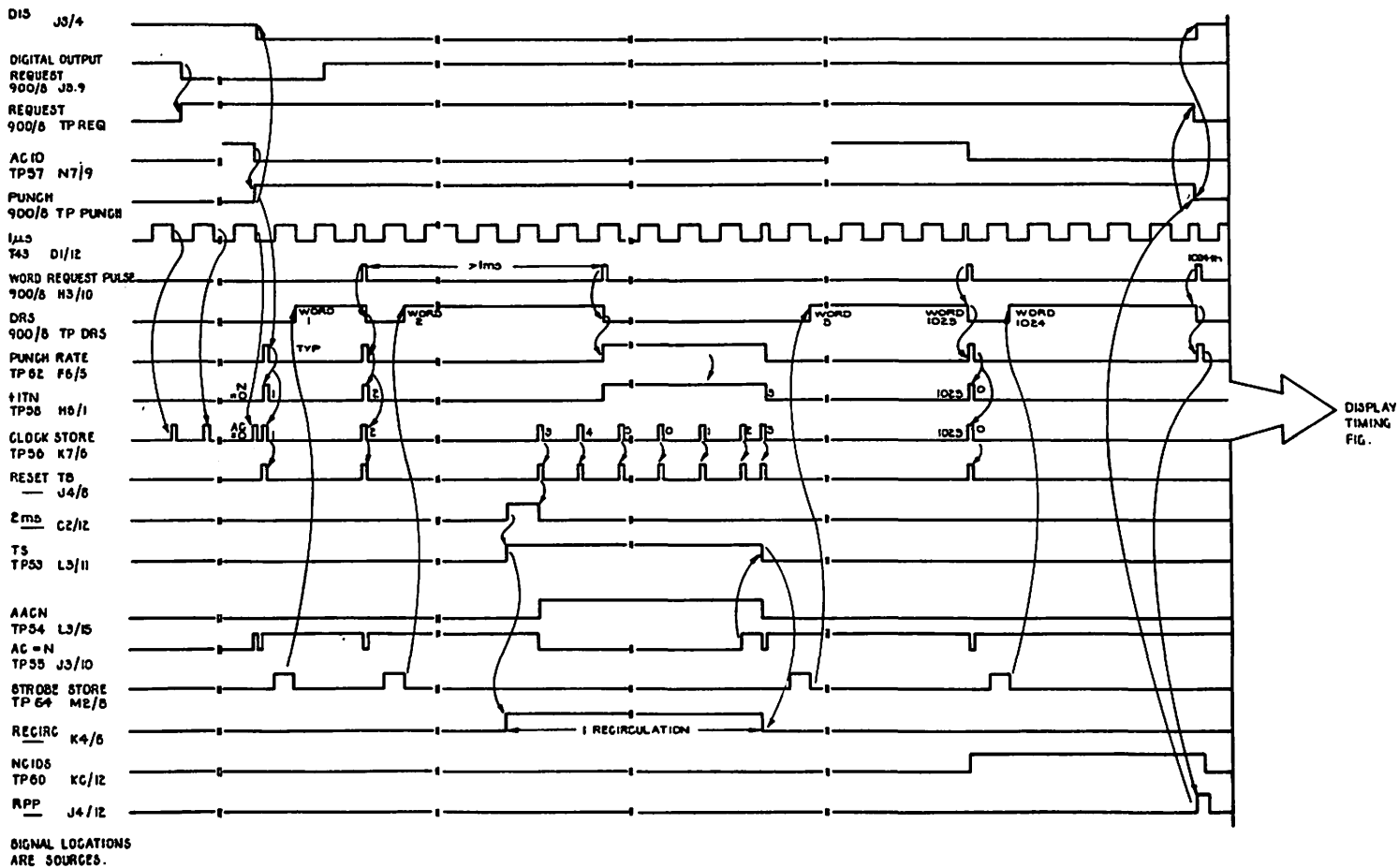


Figure 4-10 Timing Diagram — Punch Mode

4.9 POWER SUPPLY

4.9.1 General

The power supply is of conventional series stabiliser design incorporating I.C. regulator amplifiers mounted on a printed circuit card 901/PS.

This card is wired into the power supply assembly

4.9.2 Supply Lines

The supply is fused at the A.C. power input by either a 1A 230V fuse or a 2A 115V fuse accessible at the recorder rear panel. Units are factory wired for 230V or 115V operation although the power transformer tapping can be changed in service by reference to Figure 6-15.

Three stabilised D.C. supplies are generated to power the DL901 circuits; they are +15V at 0,1A, +5V at 2,5A, and -15V at 0,25A. Each supply is protected against short-circuit or overload by a current limiting feature in the regulator which reduces the output voltage when an excessive current is taken.

Each supply can be pre-set by a potentiometer on the printed circuit card which also provides test points for monitoring the supplies (see section 5.2). Note that when the power supply is unplugged its supplies are isolated from each other — their grounds are commoned at the main circuit card.

4.9.3 Removal of Unit

The power supply can be removed as a unit from the instrument case after unplugging the output plug from the main circuit card and disconnecting the mains power connectors' coupling the power input lead, 'power on' switch and power unit. These connectors are accessed by removing top & bottom cover panels. Now remove the two Philips-head screws securing the lower part of the heat sink to the case — remove the four slot-head screws securing the top cross rail member to the case sides. The power supply can now be withdrawn with the cross rail attached.

5 SET UP & CALIBRATION PROCEDURE

5.1 GENERAL

This section describes the correct procedure for setting up the DL901 circuits. Recorders normally retain their calibration for a long period and re-adjustment procedure is usually required only in the case of replacement of a failed component.

Consult the DL901 Operating Manual Section 4 for details of the Plot Rate adjustment.

Before making any adjustments the recorder should be allowed to attain its normal operating temperature.

Equipment required for adjustment is as follows:

Square wave/ramp generator with fast risetime $\leq 10\text{ns}$.

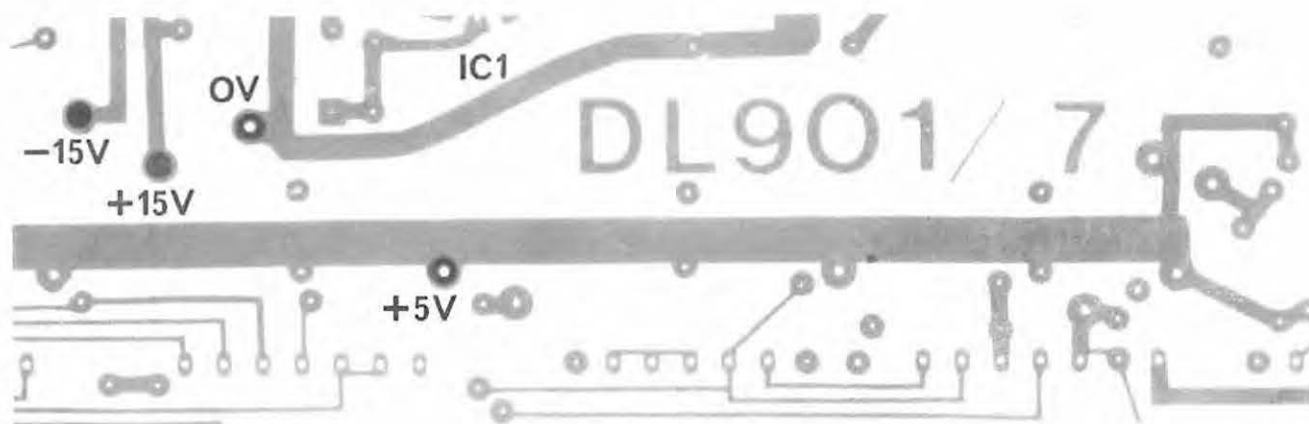
Sinewave generator with variable output.

Two-channel, 40 MHz oscilloscope.

Voltmeter.

5.2 POWER SUPPLY

Measure each of the three stabilised supplies at the indicated points on the under side of the main circuit board, with the *interface card in position*. Adjust each potentiometer on the power supply so that the supply voltage is within $\pm 50\text{mV}$ of its nominal value.



Underside of Main Board

Figure 5-1 Power Supply Test Points

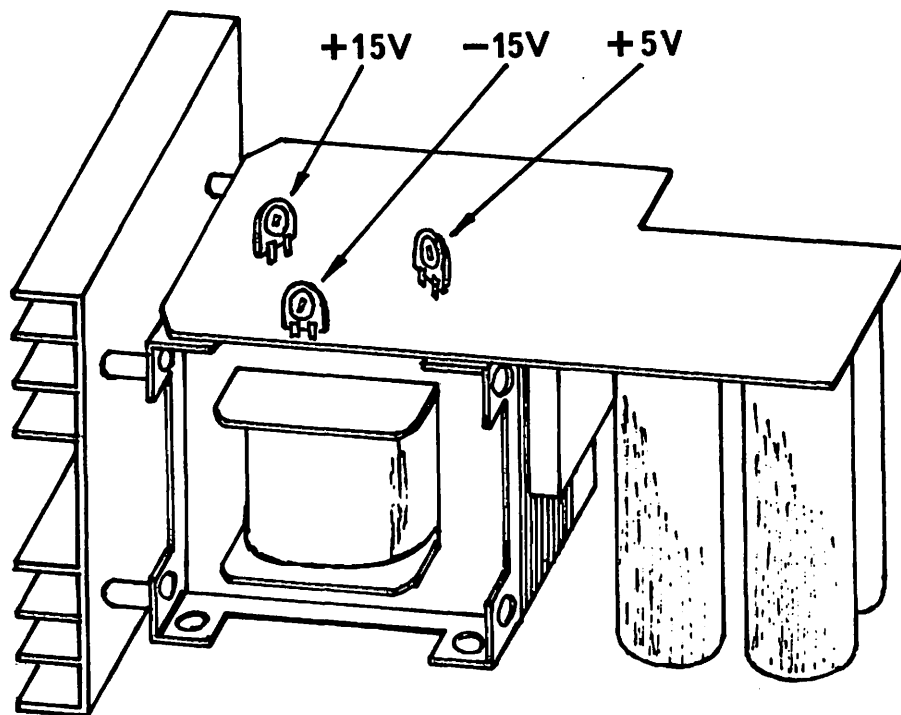


Figure 5-2 Location of Power Supply Potentiometers

5.3 INPUT AMPLIFIER

There are two methods of calibrating and adjusting the attenuator sections. In each case it is not essential that the overall gain of the recorder is exact.

METHOD 1

Connect square wave generator (set to 1kHz) to recorder input, and the oscilloscope probe to TP1 with its ground lead connected to 0V.

Set VOLTS FULLSCALE switch to 0,1V

Input offset control central.

Set generator output, such that the observed waveform at TP1 has an amplitude of less than the equivalent full scale of 5V P/P, say 4V P/P, *note* all signals at TP1 are offset negative by approximately 2,5 volts.

Now the following procedure must be followed in sequence.

- (a) Adjust CV6 for an optimum square wave output, without over or under shoot (refer to Figure 5-3).
- (b) Set VOLT'S FULLSCALE switch to 0,2V.
Adjust square wave generator to suit display (4V P/P)
Adjust CV5 for optimum square wave
- (c) Set VOLTS FULLSCALE switch to 0,5V
Adjust square wave generator to suit display
Adjust CV4 for optimum square wave
- (d) Set VOLTS FULLSCALE switch to 1V
Adjust square wave generator to suit display
Adjust CV8 for optimum square wave
- (e) Set VOLTS FULLSCALE switch to 10V
Adjust square wave generator to suit display
Adjust CV7 for optimum square wave
- (f) Check all positions of the VOLTS FULLSCALE switch to ensure that over- and undershoots are not present.

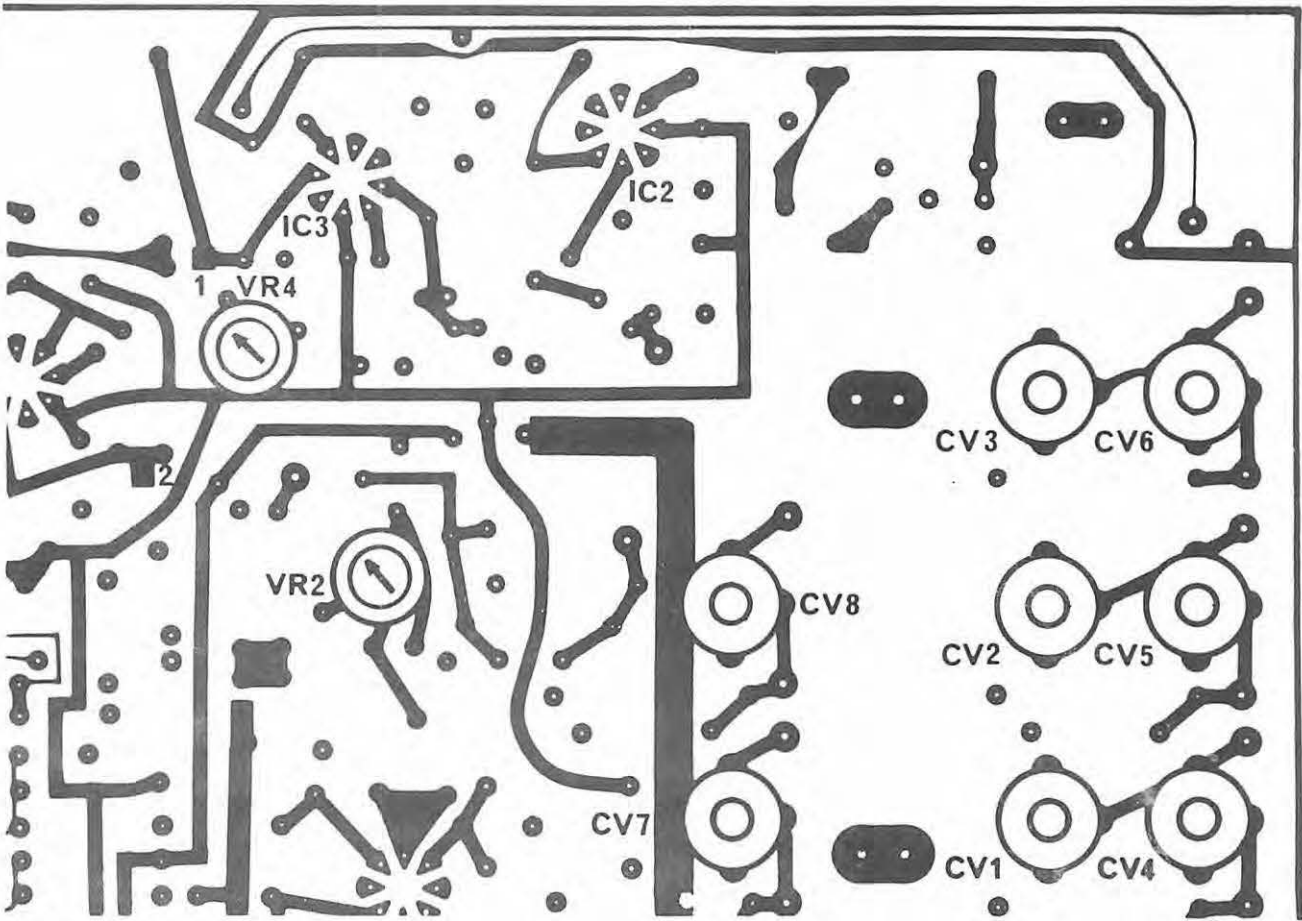


Figure 5-3 Input amplifier-location of adjustments.

METHOD 2

This method involves the DL901 recorder, connected to a display oscilloscope in the normal manner, see the Operating Manual, Section 4.1. First, determine the fullscale limits of the recorder output, on the display oscilloscope.

Set VOLTS FULLSCALE switch to 0,1 inject a 1kHz signal from the square wave generator adjusting the generator amplitude and the recorder offset control, to centre an almost fullscale signal. Use 5ms sweep time, delayed sweep with continuous triggering.

Then follow (a) to (f) as for Method 1 adjusting the trimmer capacitors for optimum squarewave on the display oscilloscope.

5.3.1 Input Capacitance Equalisation

The network shown in Figure 5-3 is required for this adjustment:—

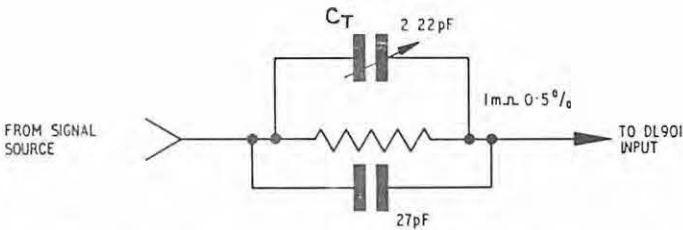


Figure 5-4 Input Capacitance Equalisation Network

The network is best mounted in a screened box, fitted with BNC input and output connectors, a small hole is required for access to the Trimmer. The input capacitance may now be equalised between input ranges as follows:—

Connect Square wave generator set to 1kHz to Recorder via the network, the input amplifier output can be observed by one of the two methods previously outlined.

- (a) Set Volts full scale switch to 0,05V. Adjust generator output to suit display, adjust C_T of network Figure 5-4 for optimum square wave.
- (b) Set volts full scale switch to 0,1V adjust generator output to suit display, adjust CV3 for optimum square wave.
- (c) Set volts full scale switch to 0,2V adjust generator output to suit display, adjust CV2 for optimum square wave.
- (d) Set volts full scale switch to 0,5V adjust generator output to suit display, adjust CV1 for optimum square wave.

5.4 PREAMPLIFIER GAIN ADJUSTMENT

The overall gain of the DL901 recorder is set by potentiometer VR4. Feed a 400 Hz sine wave, amplitude precisely 1V P/P into the recorder input, select VOLTS FULLSCALE = 1 volt, delayed sweep, sweep time 5ms. Adjust the trigger controls to obtain a waveform of two whole cycles, adjust the input offset control such that the positive peaks of the displayed record are just clipping. Whether the gain is too high or too low will be indicated by the negative peaks being clipped or not; by successively moving the input offset control and adjusting VR4 a position for both controls will be found where the positive and negative peaks are on the point of clipping, this is the correct setting.

5.5 TRIGGER OFFSET

In the event of FET TR4 being replaced, an adjustment for gate source voltage is required. Potentiometer VR2 is provided for this purpose. Select EXT TRIG + with trigger coupling to D.C. Do not inject any signal into the EXT TRIG socket.

Locate junction C34, R62, VR2 wiper, adjust VR2 for zero volts at this junction with an oscilloscope, or sensitive voltmeter.

5.6 DIGITAL-TO-ANALOG CONVERTER

Acceptable linearity can be obtained without specialized equipment if the following procedure is carried out. This procedure is only necessary if any of the following components have been changed:

- R167 to R180 inclusive
- D26 to D49 inclusive
- VR5 to VR8 inclusive

Record one sweep of a 5ms ramp waveform, with a time base speed of 5ms, adjust the input amplitude, and trigger controls to obtain a display as Figure 5-5.

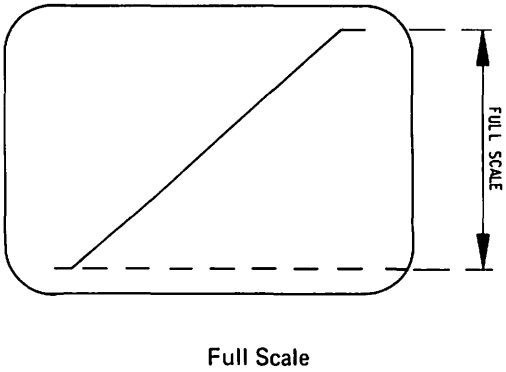


Figure 5-5 Adjusting linearity of D/A Converter

The adjustment of VR5 to VR8 must be made in the following sequence:

VR8, VR7, VR6, and VR5 last.

Each potentiometer should be adjusted in turn to obtain a smooth line, with the minimum of discontinuity.

Adjustment of VR8 produces the effect shown in Figure 5-6

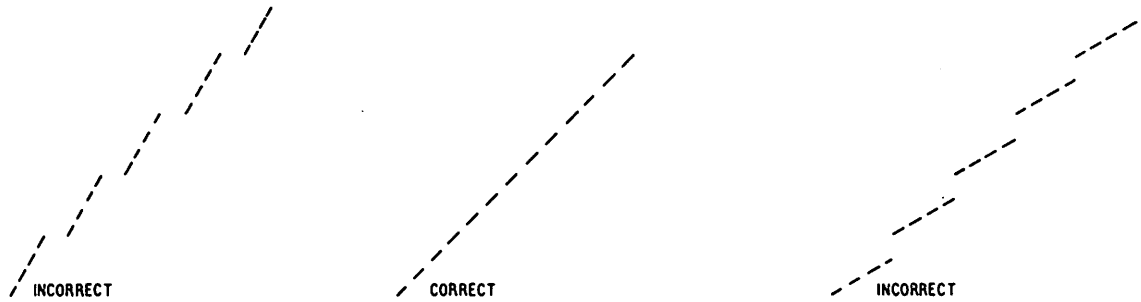


Figure 5-6 Enlarged Portion of the Display

Adjustment of potentiometers VR5, 6, 7 affect different parts of the displayed waveform. The circles indicate these areas, see Figure 5-7.

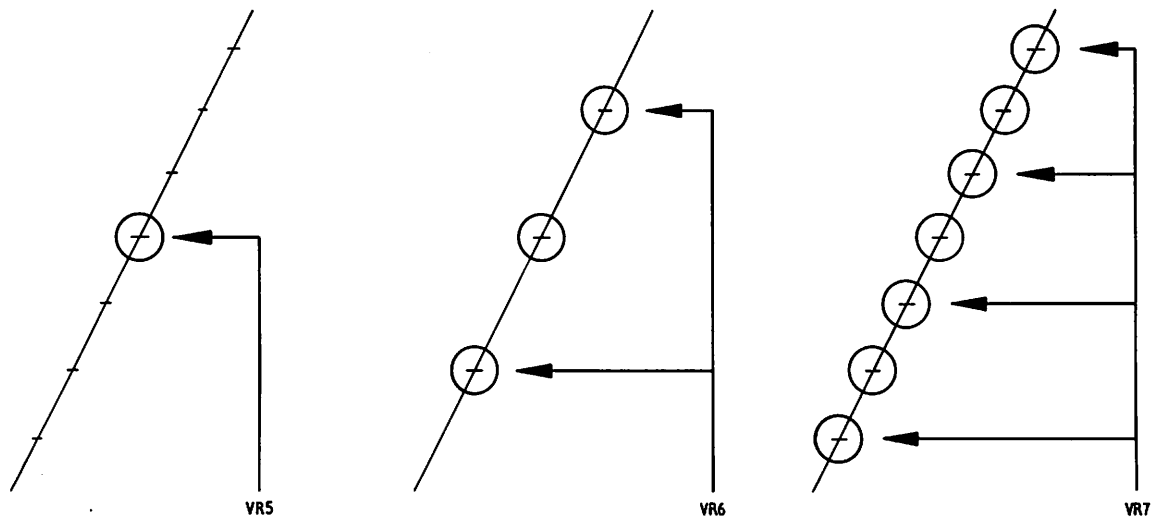


Figure 5-7 Display Effect due to Potentiometer Adjustment

When adjusting these potentiometers the areas denoted by the arrows, are the most important.

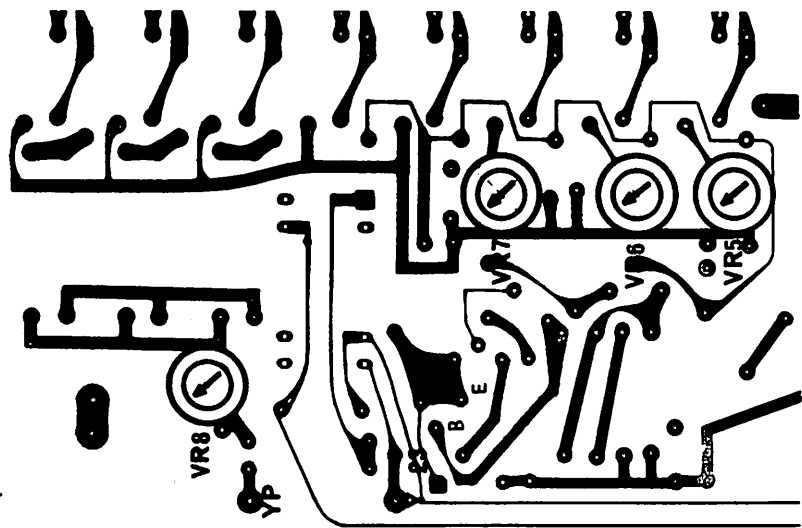


Figure 5-8 D/A Converter-Location of Potentiometers

6 SERVICE GUIDE

6.1 INTRODUCTION

The purpose of this Service Guide is to provide a logical sequence of tests which will trace and isolate faults in the recorder. The Service Guide is intended for use by personnel with general experience in instrument practice and who are conversant with digital logic techniques. Whilst the following checks are intended to locate most fault conditions they are not foolproof; they will, however, provide a good insight into the functioning of the instrument and help to locate many faults. Inexperienced operators are recommended to refer to the Manufacturer or their local Agency for Service support.

The circuit descriptions contained in the first part of the Technical Manual should be used in conjunction with the Service Guide. Logic packages are referred to by their position in the letter/number matrix used on the printed circuit board; e.g. A7/10 refers to pin 10 of the package in column A row 7. Major waveforms in the instrument (see subsection 7.1) can be monitored at Test Points noted in the text as TP. Other components are referred to by their circuit designation.

6.2 INITIAL CHECK

When a fault condition is suspected, first checkout the A.C. power supply & fuse for correct voltage and continuity. Then proceed to the peripheral equipment-preamplifiers, transducers, trigger sources, monitor oscilloscope, etc. If the Recorder still does not function make sure that it is being operated correctly by referring to Section 6 of the Operating Manual.

Now with the DL901 in its Display Mode (unarmed, single trigger) work through the next three general purpose checks of power unit, crystal oscillator/timebase and switch status. Faults in any of these items can cause unpredictable malfunction of the instrument. Check back through non-functional circuits and replace components as necessary.

6.3 POWER SUPPLY CHECK

Measure the following voltages at the Test Points shown on Figure 5-1. With an oscilloscope check each supply for negligible ripple.

+15V $\pm 0,05V$
+ 5V $\pm 0,05V$
-15V $\pm 0,05V$

The power unit circuit diagram is located on Figure 6-15

6.4 CRYSTAL OSCILLATOR/TIMEBASE CHECK

Monitor TP41 on an oscilloscope. Logic level signal should have a period of 333ns and a mark/space ratio of 4:1.

Monitor TP43 on an oscilloscope. Logic level signal should have a period of 1 μ s and a mark/space ratio of 2:1.

Monitor TP66 and compare the Timebase Output against Timing Diagram in Figure 6-1 for each position of the Sweep-time Control. The Timebase circuits are shown on Figure 6-14.

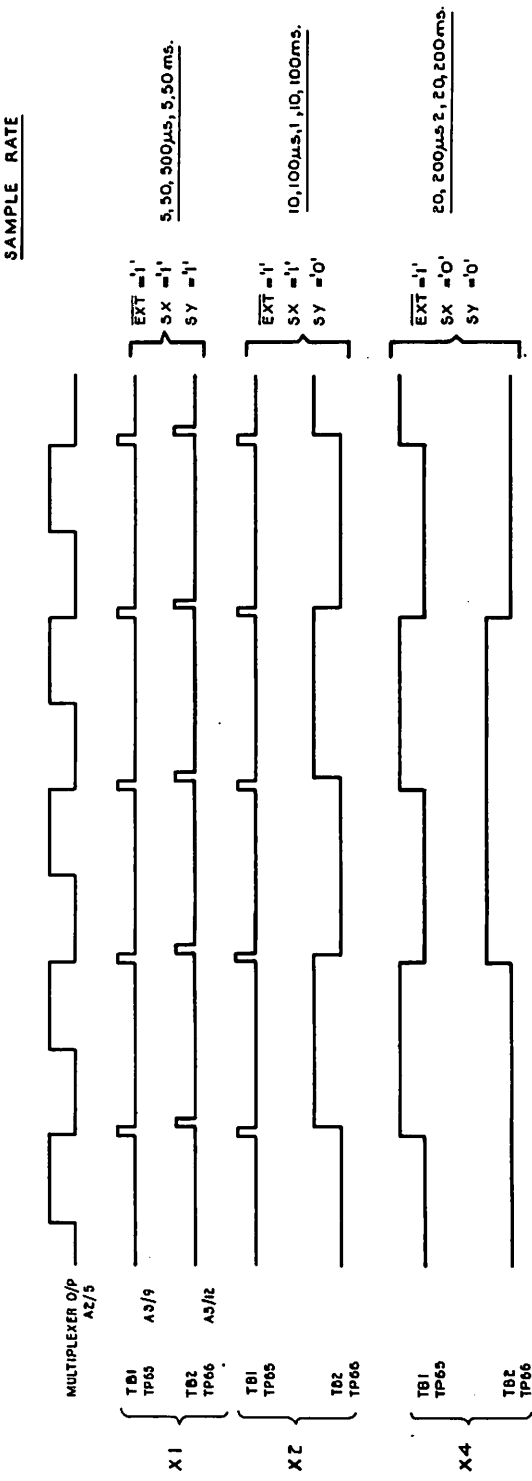


Figure 6-1 Timebase Generator Sequence

6.5 SWITCH STATUS CHECK

Using an oscilloscope or voltmeter check the voltage levels produced by the Front Panel switches as indicated below.

Switch	Signal	Wire Colour	Destination	Switch Position	Voltage
TRIGGER SLOPE	-VE TRIG	GN/BK	I.C. E6/4	INT+/EXT+	0V
TRIGGER SLOPE	-VE TRIG	GN/BK	I.C. E6/4	INT-/EXT-	+5V
MAN TRIG	DIGITAL TRIGGER	YL/BK	I.C. E6/10	Released	+5V
MAN TRIG	DIGITAL TRIGGER	YL/BK	I.C. E6/10	Depressed	0V
TRIGGER MODE	$\overline{\text{AUTO}}$	SL/WH	I.C. B7/1/12/13	AUTO	0V
TRIGGER MODE	$\overline{\text{AUTO}}$	SL/WH	I.C. B7/1/12/13	CONT/SINGLE	+5V
TRIGGER MODE	$\overline{\text{CONT}}$	VL/WH	I.C. B7/2	AUTO/SINGLE	+5V
TRIGGER MODE	$\overline{\text{CONT}}$	VL/WH	I.C. B7/2	CONT	0V
TRIGGER MODE	$\overline{\text{ARM SW}}$	YL	I.C. E2/2/4/5	AUTO/CONT/SINGLE Depressed	+5V 0V
SWEEP MODE	PRE	ORG	I.C's E3/9/10, E4/3 D5/3, C4/13, F4/1/5, M2/1	DEL'D SWEEP	0V
SWEEP MODE	PRE	ORG	I.C's E3/9/10, E4/3 D5/3, C4/13, F4/1/5, M2/1	PRE TRIG	+5V
PUNCH/PLOT	$\overline{\text{PLOT SW}}$	BK	Interface Pin AK	Released/Raised	+5V
PUNCH/PLOT	$\overline{\text{PLOT SW}}$	BK	Interface Pin AK	Depressed	0V
PUNCH/PLOT	$\overline{\text{PUNCH SW}}$	BN	Interface Pin AL	Released/Depressed Raised	+5V 0V

The digital delay lever switch produces an 8-4-2-1 negative true B C D code which can be checked against the table below.

Signal, Destination & Wire Colour Position	$\overline{\text{D8}}$ I.C. A6/3 BN/WH	$\overline{\text{D4}}$ I.C. A6/1 ORG/WH	$\overline{\text{D2}}$ I.C. A6/5 YL/WH	$\overline{\text{D1}}$ I.C. A6/9 GN/WH
0	+5V	+5V	+5V	+5V
1	+5V	+5V	+5V	0V
2	+5V	+5V	0V	+5V
3	+5V	+5V	0V	0V
4	+5V	0V	+5V	+5V
5	+5V	0V	+5V	0V
6	+5V	0V	0V	+5V
7	+5V	0V	0V	0V
8	0V	+5V	+5V	+5V
9	0V	+5V	+5V	0V

The sweeptime switch produces a five-bit code which can be checked against the table below:

Signal Destination & Wire Colour Position	SA I.C. A1/11, A2/11 BL	SB I.C. A1/10, A2/10 VL	SC I.C. A1/9, A2/9 SL	SX I.C. A4/10 WH	SY I.C. A4/5 BK/WH
5ms	+5V	0V	0V	+5V	+5V
10ms	+5V	0V	0V	+5V	0V
20ms	+5V	0V	0V	0V	0V
50ms	0V	+5V	0V	+5V	+5V
0,1s	0V	+5V	0V	+5V	0V
0,2s	0V	+5V	0V	0V	0V
0,5s	+5V	+5V	0V	+5V	+5V
1s	+5V	+5V	0V	+5V	0V
2s	0V	0V	+5V	0V	0V
5s	+5V	0V	+5V	+5V	+5V
10s	+5V	0V	+5V	+5V	0V
20s	+5V	0V	+5V	0V	0V
50s	0V	+5V	+5V	+5V	+5V
100s	0V	+5V	+5V	+5V	0V
200s	0V	+5V	+5V	0V	0V
EXT	+5V	+5V	+5V	+5V	+5V

6.6 SIGNAL PATH CHECKS

6.6.1 Introduction

If checks in subsections 6.3, 6.4, 6.5 have not isolated the fault it is now necessary to decide if the fault is in the signal path or the control circuits of the instrument.

The signal path comprises the preamplifier, track and hold, analog-to-digital converter, store and digital-to-analog converter; faults in these circuits generally affect the amplitude of the displayed record. Broken up sinewaves, glitches at regular intervals, D.C. only recorded are characteristic of signal path faults.

This section contains a series of checks to verify the correct functioning of the signal path.

If a display on the monitor oscilloscope (even of a distorted signal) is unobtainable first check out against subsection 6.6.9. Then proceed to subsection 6.7 for the control circuit checks.

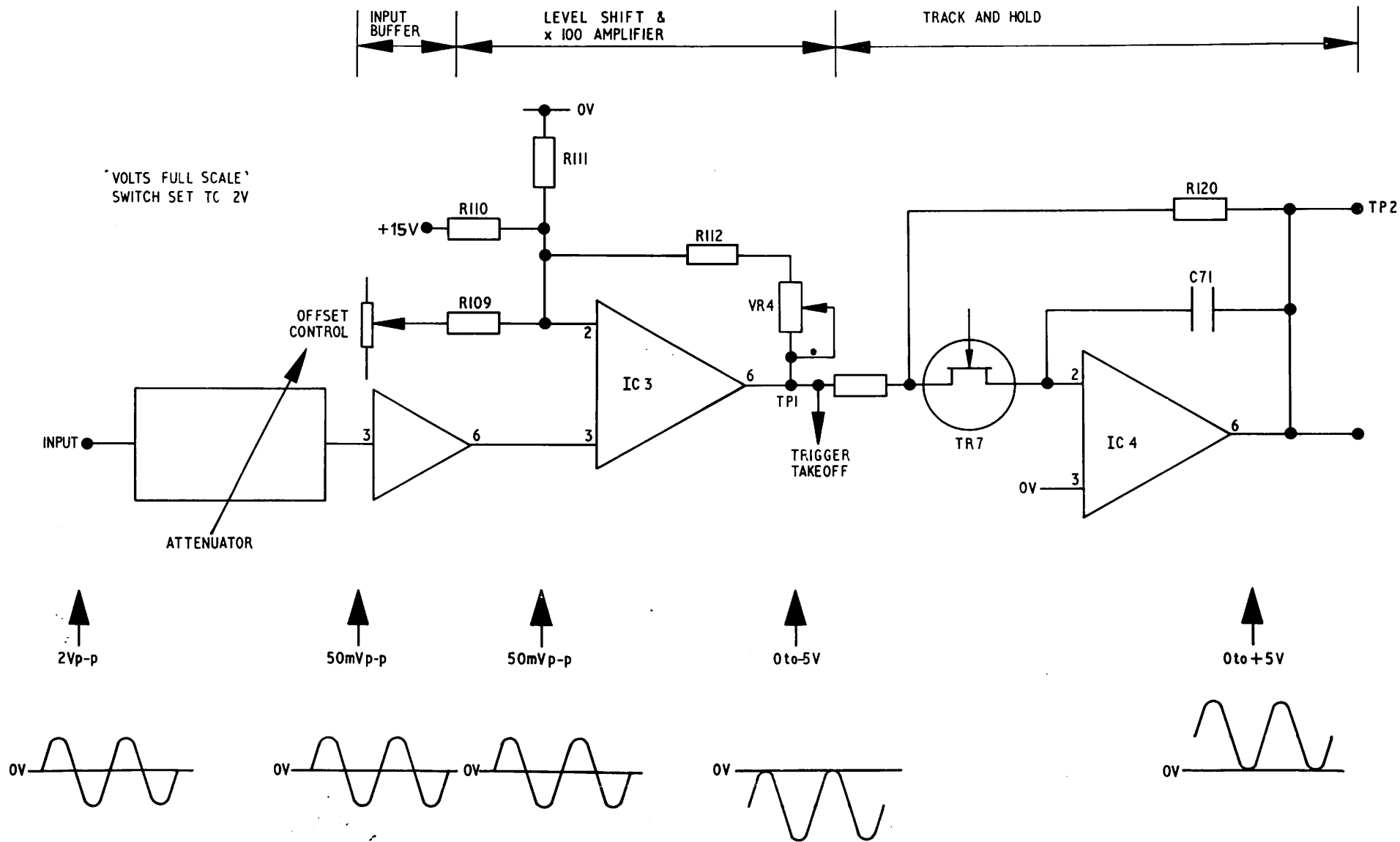
6.6.2. Pre-amplifier/Track Hold Check

Figure 6-2 shows the amplitude and level shift changes that occur in the input amplifier and track and hold circuits to a full scale input signal with the VOLTS FULL SCALE switch set accordingly.

The input to the unity gain buffer IC2 is 50mV p/p, for full scale output from the track and hold circuit.

Amplifier IC3 provides a signal gain of X100 together with a fixed negative offset of 2.5V (this is produced by R110) and a variable offset produced by R109 and the front panel OFFSET control.

Figure 6-2 Analog Signal Path



6.6.3 Check Offset Range

- With INPUT COUPLING switch, selecting GND, locate RED /BLK wire and measure $\pm 0,5V$ while rotating OFFSET potentiometer VR3, between minimum and maximum rotation.
- As above, measure +6 volt down to -12V, at TP1.
- As above, with OFFSET control at mid-range measure at TP1. $2.5V \pm 0,25V$.

6.6.4 Check Amplifier Gain

The measured A.C. gain of 1kHz sinewave from input of IC2 (Pin 3) to TP1 is adjustable by VR4 from 98 to 104.

6.6.5 Bandwidth Check

The measured bandwidth of IC2 and IC3 to the -3dB point (0,707) is not less than 100kHz and not greater than 120kHz.

6.6.6 Check Track and Hold

IC4 performs the track and hold function, in conjunction with TR7 — an FET switch. When the gate of TR7 is low (0V) (TRACK CONDITION) TR7 becomes a low resistance and IC4 then behaves as an inverter with unity gain. When the gate of TR7 is HIGH (+7V), TR7 is turned off (HOLD CONDITION) and C71 remains charged to the previous input potential.

Figure 6-3 is the waveform from TP2 which shows the offset that occurs with a full-scale input signal during the sweep time.

Input frequency 200Hz

901 Sweep time 5ms, delayed sweep.

Oscilloscope trigger from the DL901 signal source, timebase 1ms/div.

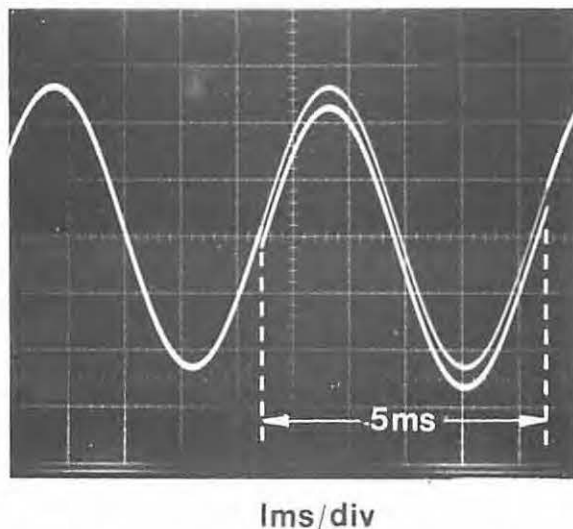


Figure 6-3 Track and Hold Waveform

6.6.7 Analog-to-Digital Converter Check

A pulse from the TIMEBASE via E6/11 sets SAMPLE (TP37) on its rising edge, provided that CYCLEA is HIGH. The rising edge of SAMPLE sets SYNC (TP38), this removes the reset from $\div 2$ (TP39), $\div 2$ is consequently set by the next available 3MHz clock pulse, this allows the following 3MHz clock pulse to set CONVERT (TP40) F7/12.

See Timing Diagram Figure 4-2.

CONVERT being set allows 3MHz (TP41) to be gated via J7/11 to form ADC CLOCK. Initially ADC CLOCK ripples through AND gates H10 and H9 to clock CR7 (TP5) set, and to set CR8 (TP4) if DISC is high (DISC high indicates that the input signal is negative). Should the DISC be high then the action of setting CR8 removes the most significant current and the setting of CR7 introduces the next lower significant current to the summing network of IC5.

The process continues in a similar fashion, i.e. the next ADC CLOCK pulse sets CR6, and CR7 is now reset or remains set depending upon the action of the discriminator. The seventh ADC CLOCK pulse sets CR1 and may reset CR2 and the eighth ADC CLOCK pulse resets CR1 if required and also allows CONVERT (TP40) to be reset thus ending the conversion period, and allowing SYNC (TP38) to be reset via D7/8, see subsection 4.4.2. SYNC subsequently resets SAMPLE (TP37) via F5/4 and D5/8.

It is possible by removing LINK SS, which connects CR1 to CONVERT K input, to isolate ADC faults to the conversion register or the conversion register control logic. The removal of this link allows the general logic to operate at a rate determined by the Time Base, except that SAMPLE, SYNC, $\div 2$, and CONVERT do not complete a correct conversion sequence, due to the fact that the CONVERT K input F7/3 is FLOATING, and assumes a "1" potential, and, therefore, is set and reset by consecutive 3MHz clock pulses thus producing a single ADC CLOCK pulse. If the aforementioned sequence does not happen then the fault lies within the ADC Control logic and possibly not with the Conversion Register.

If the control logic toggles as described, then a conversion register malfunction is certain.

Figure 6-4 shows the waveform at IC5 pin 3 when the analog-to-digital converter is operating correctly. The lower trace is a repeat of the TP2 waveform.

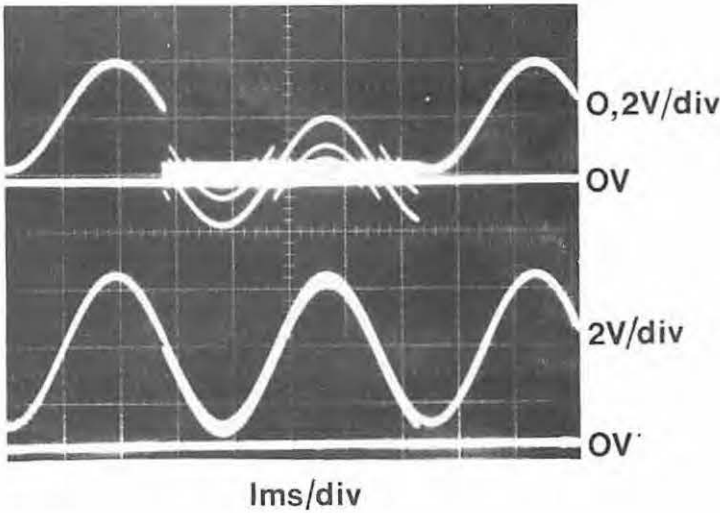


Figure 6-4 Discriminator Input

6.6.8 Store Check

Record one cycle of a fullscale sinewave input signal of 200Hz frequency using the Delayed Sweep mode with a Sweeptime of 5ms.

Use CRO TRIG to trigger a dual-trace oscilloscope and monitor Y DISPLAY on one trace — with a timebase speed of 0,1ms/div.a smooth trace should be observed. Repeat the test with a signal frequency of 1Hz, and a Sweeptime of 1s. In both cases the displayed record should be free from non-linearities and glitches — other than those caused by signal noise and digital-to-analog converter switching transients. Presuming that the preamplifier, track/hold and analog-to-digital converter have been checked and found correct,any non-linearity in the displayed record will be caused by a store or digital-to-analog converter fault.

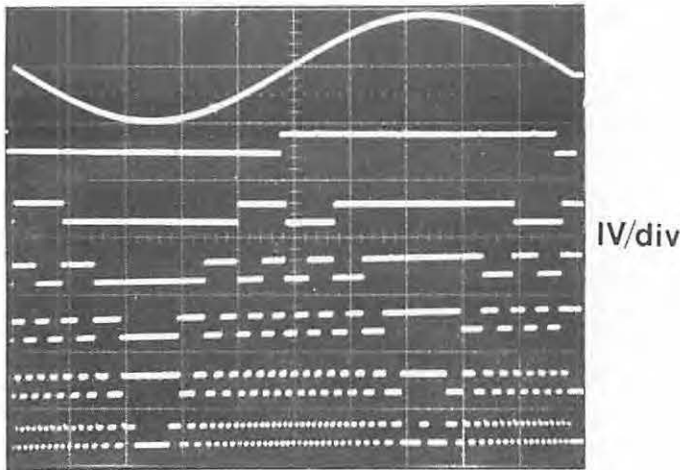
If both tests are successful then the store and digital-to-analog converter are functioning correctly — non linearities in records taken at Sweeptime greater than 1s would be due to a control malfunction. If the 5ms record is satisfactory and the 1s record is incorrect then a faulty shift register is indicated. A digital-to-analog converter fault would be observed regardless of Sweeptime. Errors in the 5ms record could be due to either store or digital-to-analog converter.

Using the second trace of the oscilloscope monitor pin 5 of each shift register IC's MM1—MM8. IC MM8 is the most significant bit store and should show four transitions when compared to the Y DISPLAY signal. The number of transitions doubles for each less significant bit.

By comparing Y DISPLAY with individual shift register outputs, errors can be quickly related. See Figure 6-5 for Y DISPLAY V MS 6 BITS.

If a shift register is suspected, first check the store input/recirculate multiplexers IC's H8, H11 by comparing their input/output waveforms during the 5ms recording sweep:trigger the oscilloscope from TP31 0/1 transition (SWEEP).

If more than one shift register is suspect check first that the -9V supply to each register is correct and also that the Clock Driver is functional:— the antiphase clock pulses switch between +5V and -8V; being at -8V for not less than 130ns.



- Top trace — Y display. Record of 200 Hz signal
- 2nd trace — MS bit at TP15 — bit 8
- 3rd trace — 2nd MS bit at TP16 — bit 7
- 4th trace — 3rd MS bit at TP17 — bit 6
- 5th trace — 4th MS bit at TP18 — bit 5
- 6th trace — 5th MS bit at TP19 — bit 4
- 7th trace — 6th MS bit at TP20 — bit 3

Figure 6-5 Multiple Exposure of Store Waveforms

When replacing a shift register remember that it is a high impedance MOS device and care must be taken to avoid static charge damage. Always use a grounded soldering iron and short out the device leads when handling.

Having checked that the shift registers are functional next check the output multiplexers IC's K8, K11 — compare their inputs and outputs to Y DISPLAY in order to locate the suspect gate. Finally repeat this procedure to verify correct operation of the data output register formed by IC's K9, K10. Any non-linearities in the displayed trace must be due to a faulty digital-to-analog converter if this check is functioning correctly.

6.6.9 Digital-to-Analog Converter Check

If a digital-to-analog converter fault is suspected of causing relatively minor non-linearities then first check out the current weighting adjustments detailed in subsection 5.6. This adjustment must also be checked if any digital-to-analog converter components are changed.

By recording a D.C. input signal set exactly to midscale the following voltages should be measured at the components listed:

TR9 collector	+13,5V
TR10 collector	+7V
TR9 emitter to TR10 emitter	600mV
TR9 base to TR10 base	0V
TR8 emitter (TP23)	0V \pm 50mV

Failure of any of these components or their associated resistors etc. will generally result in a D.C. Y DISPLAY output with no A.C. component.

Non-linearities due to faulty switching diodes may be readily traced by simply comparing waveform voltage levels between different switches.

6.7 CONTROL CIRCUIT CHECKS

6.7.1 Introduction

Having checked the DL901 through all the previous procedures without isolating the fault it is safe to assume that a fault exists in the control circuits. Typical control faults are — instrument starts recording sweep but will not terminate it, trigger not accepted, no display available, digital readout just locks up. . . . Due to the large number of possible logic faults . . . it is not feasible to formalise a fault tracing procedure for each malfunction.

Instead a breakdown of the control chain is provided for each mode of operation — display, arm, trigger, record, readout. Each mode is detailed to guide the Operator through only the relevant logic circuits — at each step possible fault sources are noted. The procedures are not infallible so the relevant procedure should be repeated if the validity of its result is in doubt. The flowcharts should be used in conjunction with the Technical Descriptions and Timing Diagrams in the first part of this Manual.

Many of the control sequences have to be repeated several times to enable oscilloscope monitoring of the various signals. The fault being traced may not allow repetitive sequences to be initiated especially when it prevents a sequence from terminating correctly. So it is often necessary to reset the recorder logic between triggers, plot switch operations, etc. A reset is easily applied to the control logic by momentarily grounding pin 10 of IC A7 — thereafter the relevant control switch can be operated to initiate the sequence being monitored.

Before proceeding with the control logic checks first check the trigger circuit.

6.7.2 Trigger Circuit Check

Measure $\pm 15V$ at R64, whilst rotating the TRIGGER LEVEL control between its limits.

Measure $\pm 3V$ at the junction of R64, R65 whilst rotating the TRIGGER LEVEL control between its limits.

Select INT trigger source, D.C. coupling, midscale INPUT OFFSET and Input grounded — measure $\pm 0,25V$ at R60/ R61 junction.

Select EXT trigger source. Check that TR4 source is approximately +0,5V to +1,5V. Adjust VR2 until 0V is measured at junction of C34, R62.

Now rotate TRIGGER LEVEL control between limits and check for 1/0, 0/1 transitions at TP24. 0 is typically -0,5V, 1 is typically +3,5V.

6.7.3 Pre-Trigger Recording

The slow and fast recording sweep checks use delayed sweep recording mode. The logic used in this mode is also utilised in the pre-trigger mode. Some circuits are, however, unique to the pre-trigger mode and should be checked for correct operation when the pre-trigger mode does not function.

I.C.	Function
F4/6	Generates +1TDC for sweeptimes ≤ 1 second.
F4/12	Generates +1TDC for sweeptimes > 1 second.
C4/11, E4/6 (part)	Hold DELAY, SWEEP preset during pre-trigger recording (until ARM reset).
C5/4, D5/6 (part)	Reset AC at end of Pre-Trigger recording to synchronise AC with record in store.
M2/3	Causes "continually updating" type display in pre-trigger sweeptimes > 1 second.

CONDITIONS:-

DL901 IN SINGLE TRIGGER MODE,
UNARMED - SHOULD BE DISPLAYING
STORED RECORD ON MONITOR CRO.

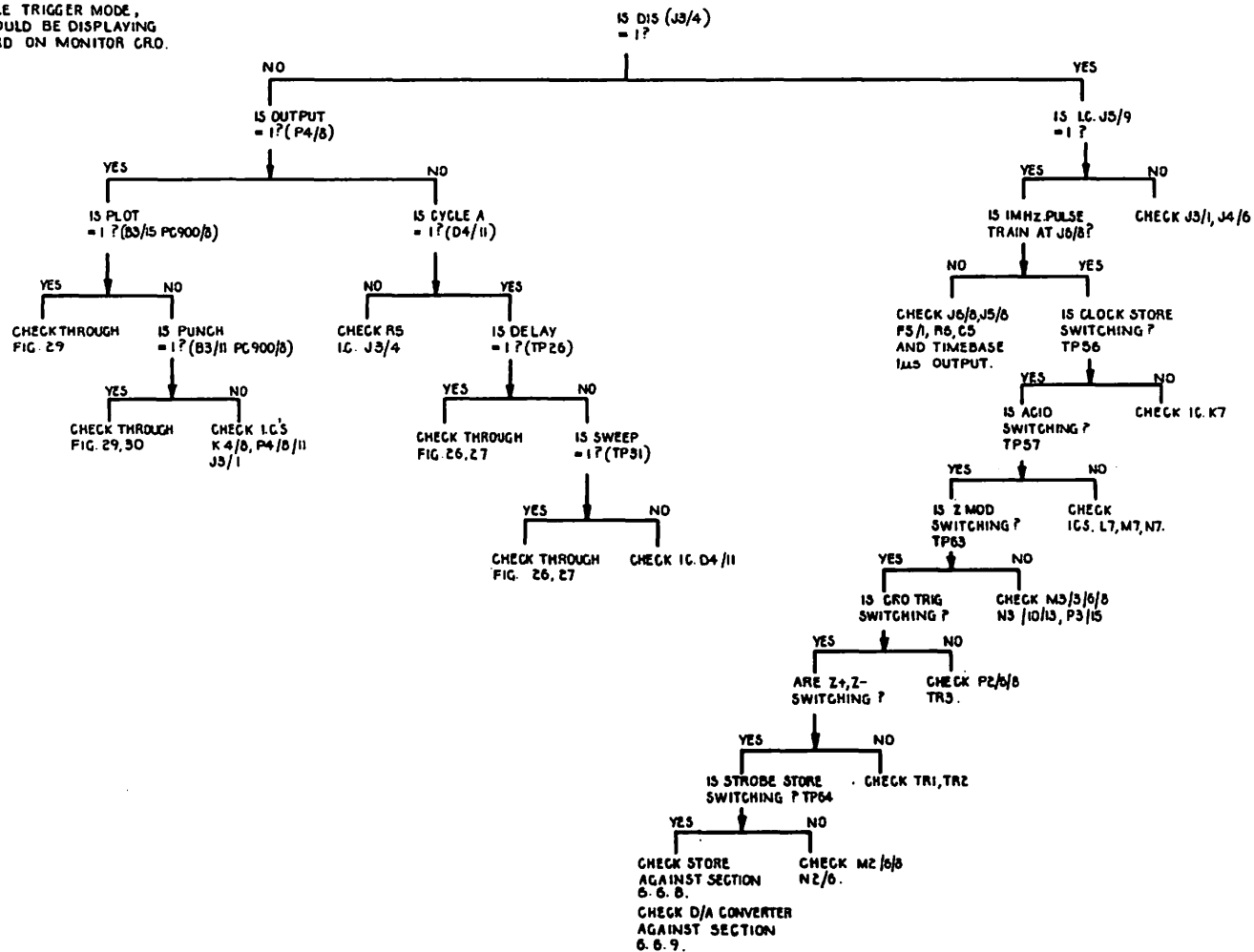
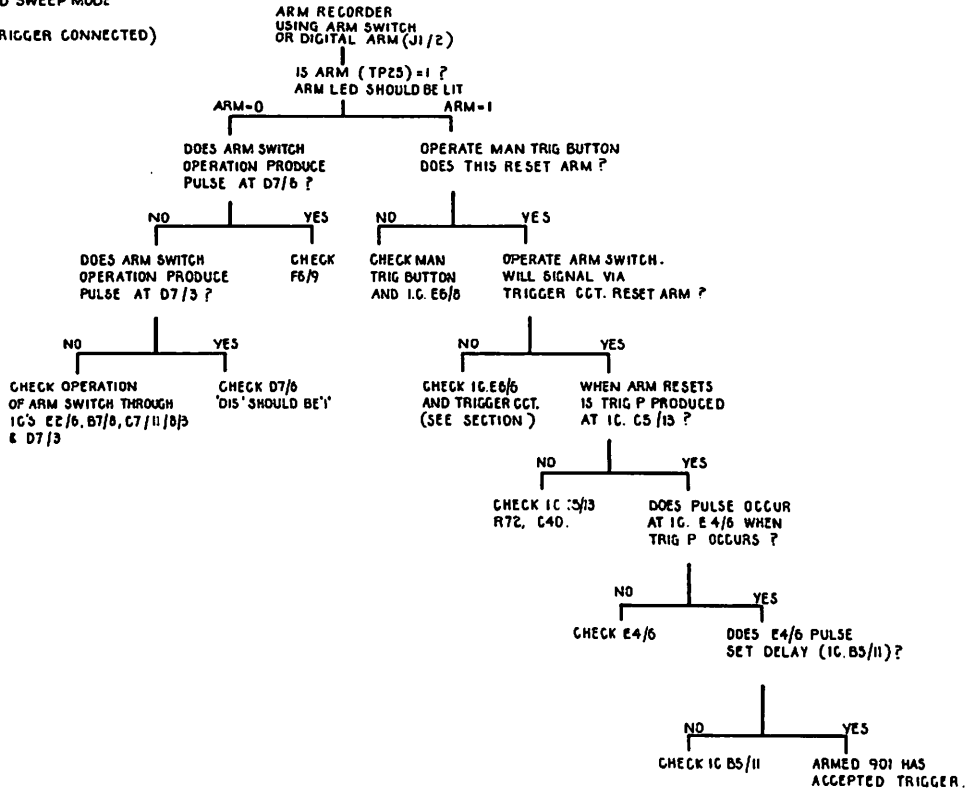


Figure 6-6 Display Mode Check

CONDITIONS : DL901 IN DELAYED SWEEP MODE
SINGLE TRIGGER
EXT. TRIG (NO TRIGGER CONNECTED)



NOTE :
DIGITAL ARM ACTS VIA I.C. E2/6
SKT J1/2 IS LINKED THROUGH
INTERFACE CARD TO I.C. E2/1

Figure 6-7 Recorder does not Arm/Trigger

CONDITIONS :- DL901 IN DELAYED SWEEP RECORD MODE.
ARMED & TRIGGERED, WITH SWEEPTIME ≤ 1 SEC.

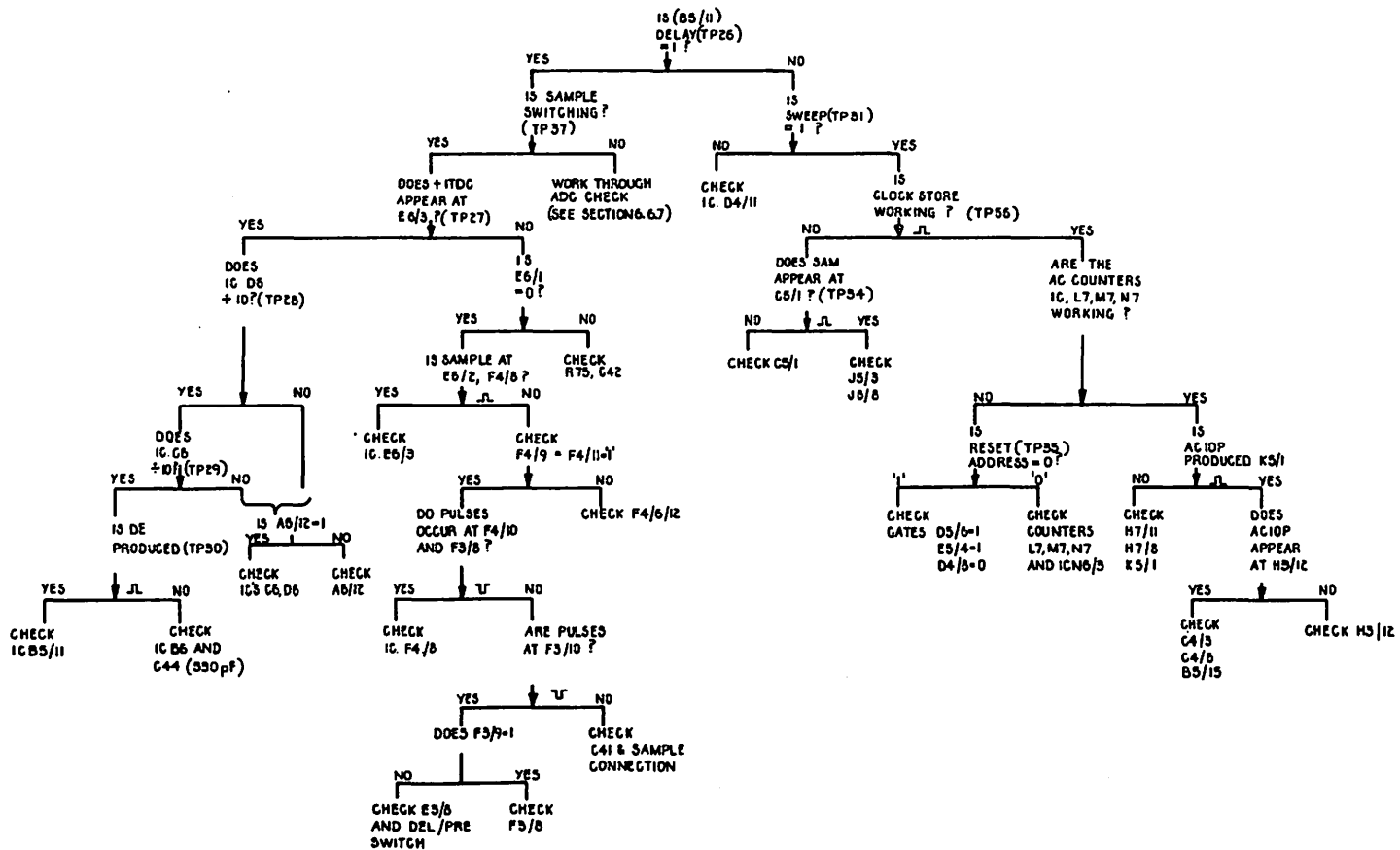


Figure 6-8 Recording with Sweeptime ≤ 1 Second

CONDITIONS:-
DL901 IN DELAYED SWEEP RECORD MODE.
ARMED AND TRIGGERED, WITH SWEEPTIME > 1 SEC.
RECORDER CHECKED & MADE OPERATIONAL
IN RECORDING WITH SWEEPTIME ≤ 1 SEC* BEFORE
USING THIS CHECK.

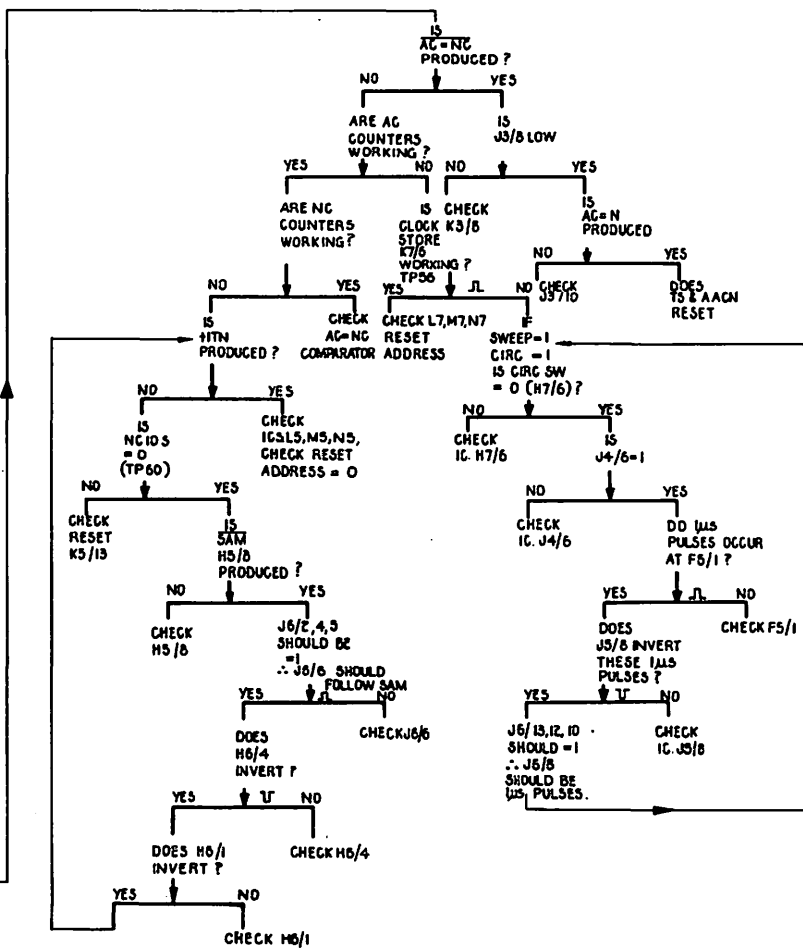
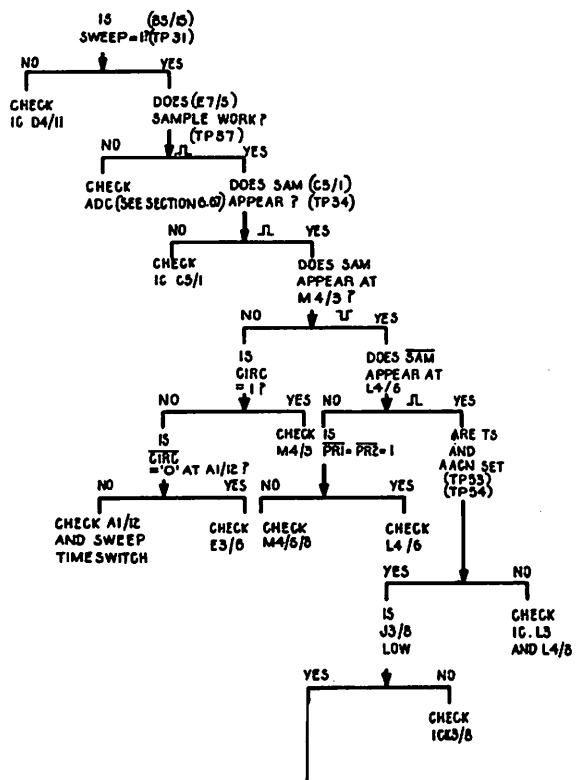


Figure 6-9 Recording with Sweeptime > 1 Second

CONDITIONS :-

DL 901 UNARMED IN SINGLE TRIGGER
MODE DISPLAYING RECORD
ON MONITOR CRO.

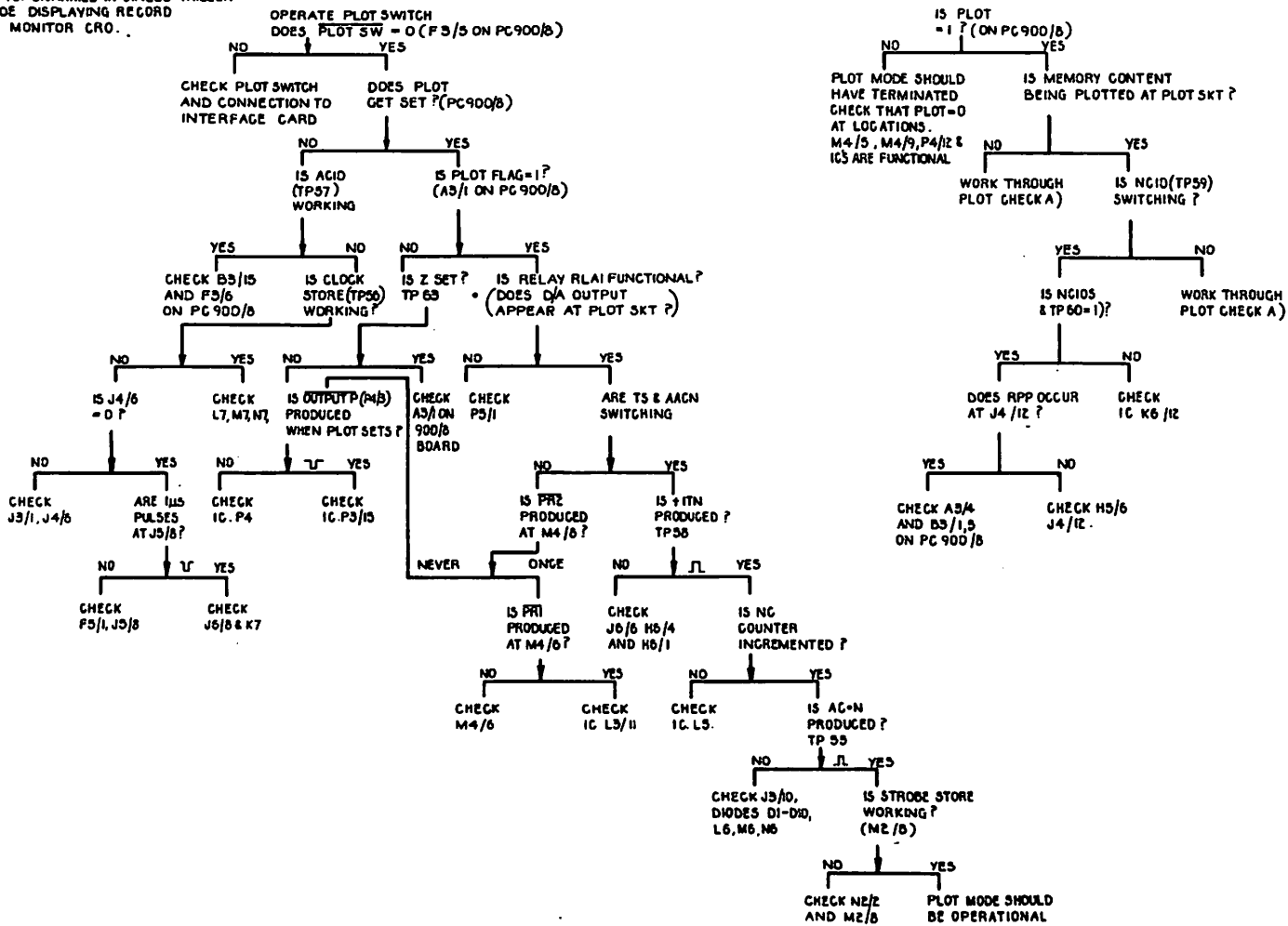
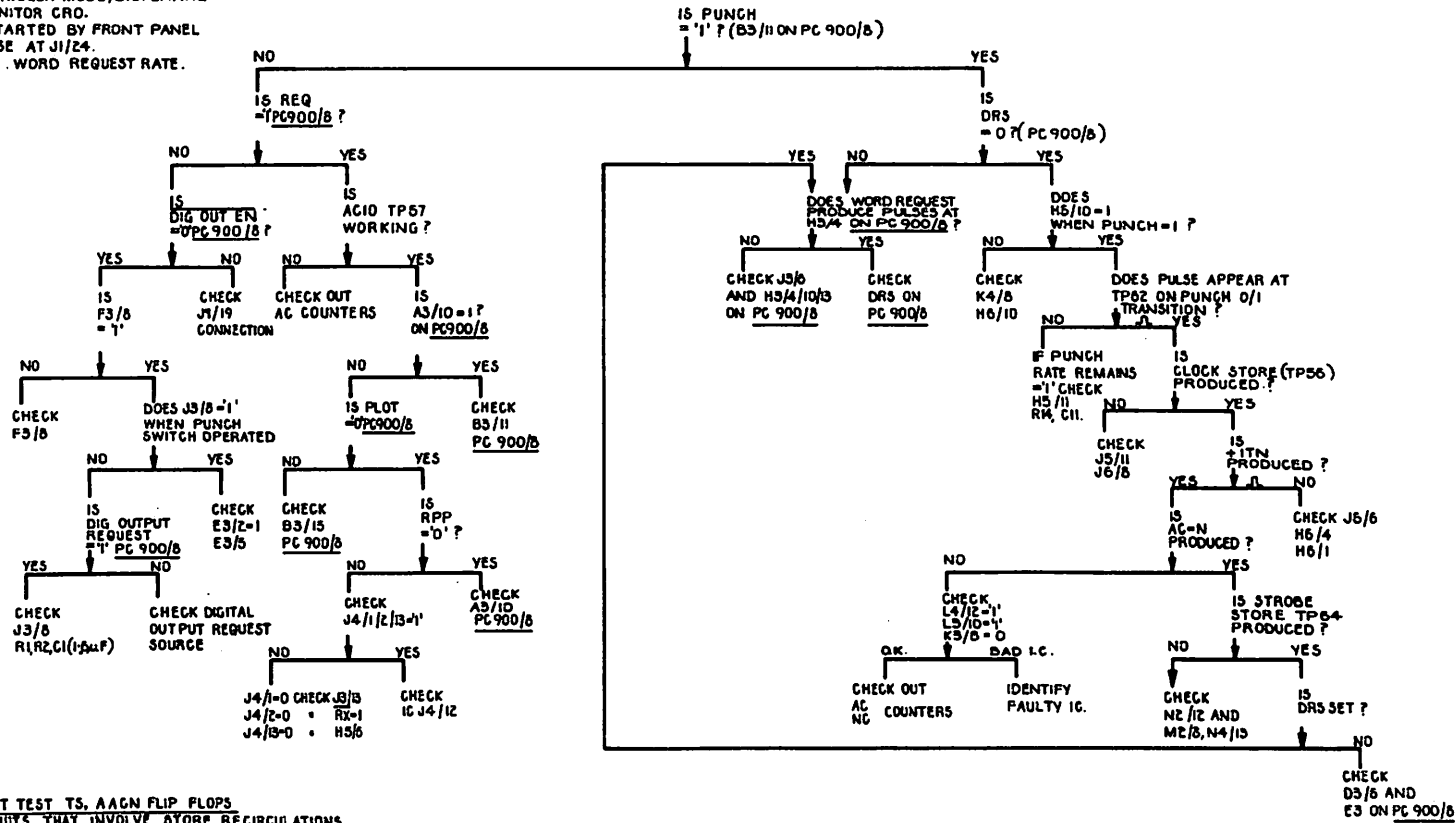


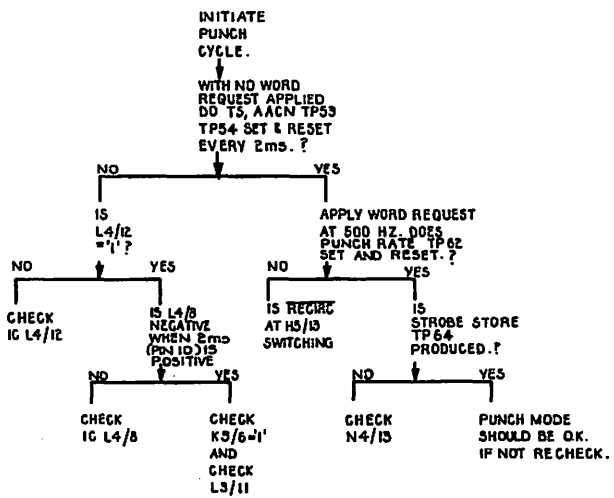
Figure 6-10 Plot Mode Check

CONDITIONS:
901 IN SINGLE TRIGGER MODE, DISPLAYING
RECORD ON MONITOR CRT.
PUNCH MODE STARTED BY FRONT PANEL
SWITCH OR PULSE AT J1/24.
WITH 200 KHZ. WORD REQUEST RATE.



THIS DOES NOT TEST TS, AAGN FLIP FLOPS
OR ANY CIRCUITS THAT INVOLVE STORE RECIRCULATIONS

Figure 6-11 Punch Mode Fast Rate



CONDITIONS:
FAST RATE PUNCH CHECK MUST BE
O.K. BEFORE MAKING THIS CHECK.
901 IN SINGLE TRIGGER MODE,
DISPLAYING RECORD ON MONITOR CRO.
PUNCH MODE STARTED BY FRONT PANEL
SWITCH OR PULSE AT J1/24.

Figure 6-12 Punch Mode Slow Rate

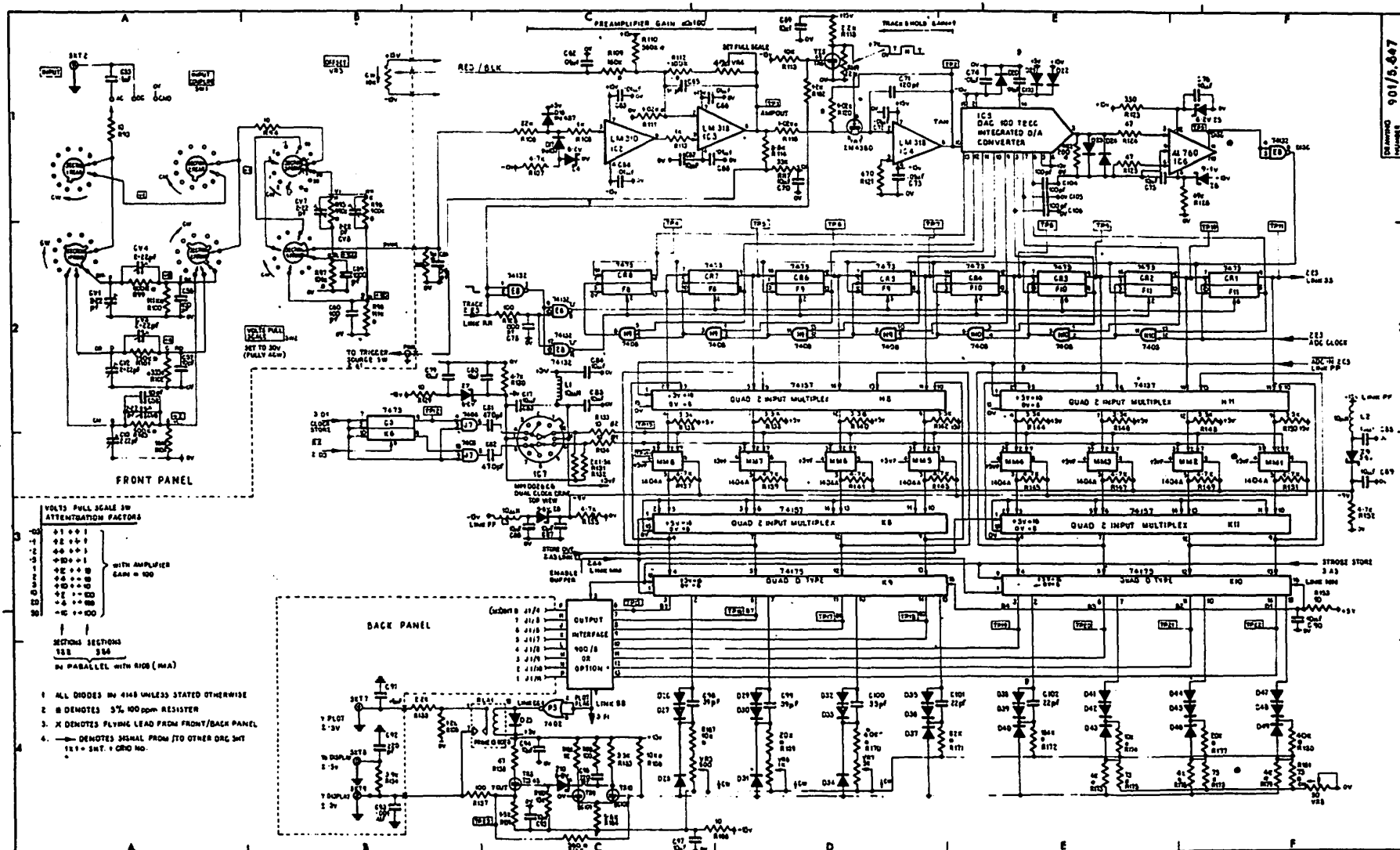


Figure 6-13a Pre-amplifier, Analog-to-Digital Converter Store and Output Digital-to-Analog Converter Logic Diagram

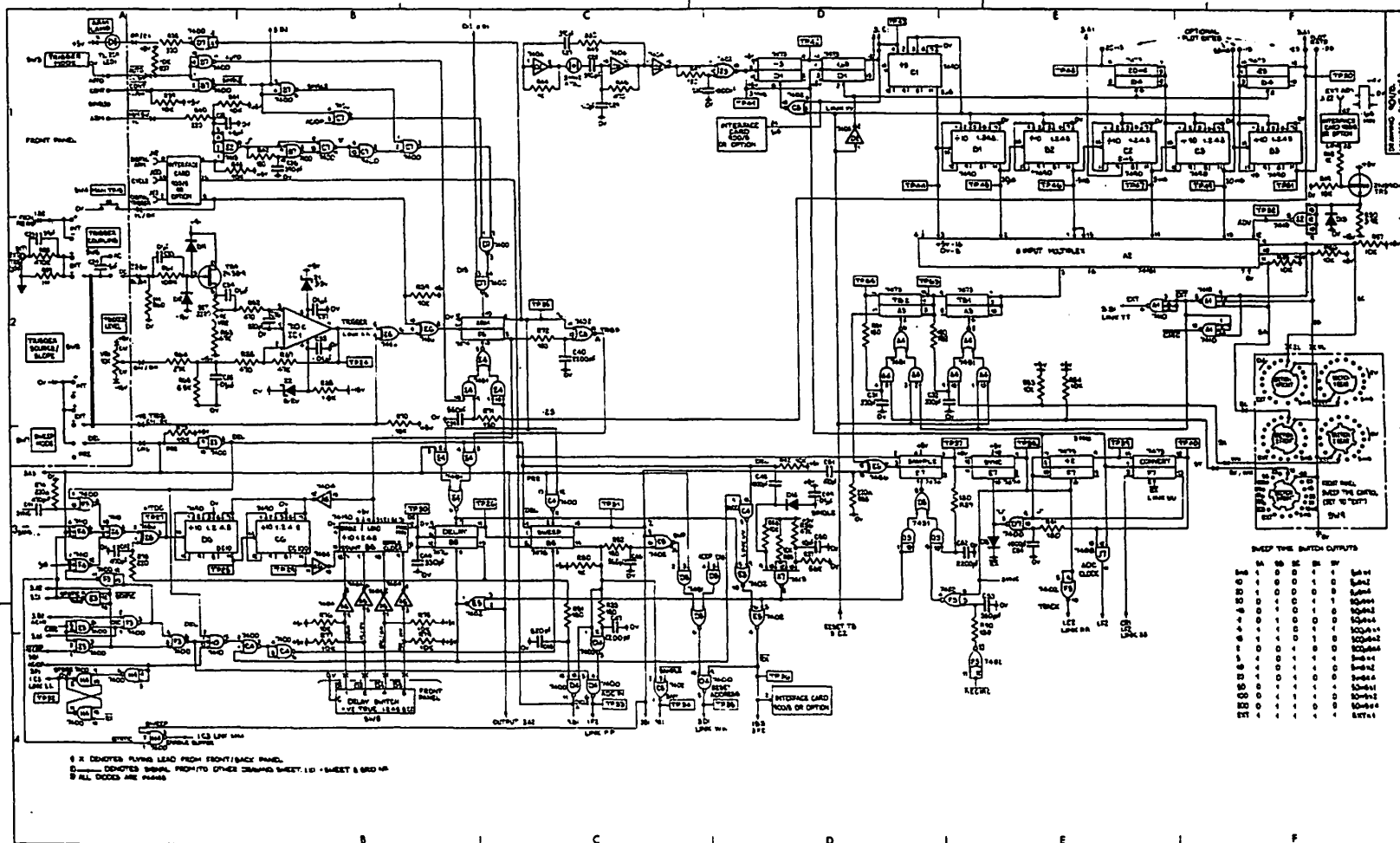


Figure 6-14b Digital Delay, Timebase and Sweep Control Logic Diagram (901/8)

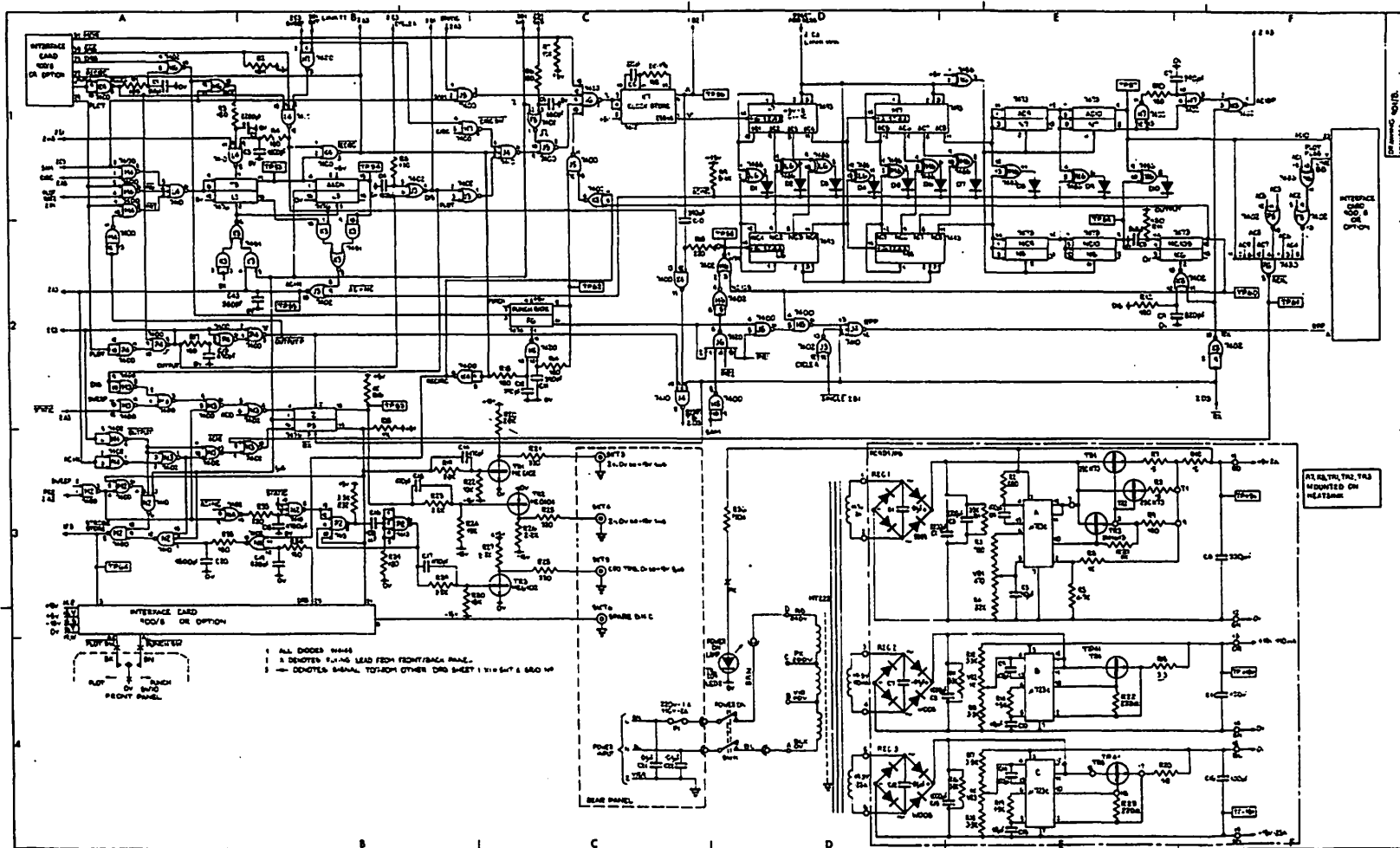


Figure 6-15b Address Recirculation, Output Control and Power Supply Logic Diagram (901/8)



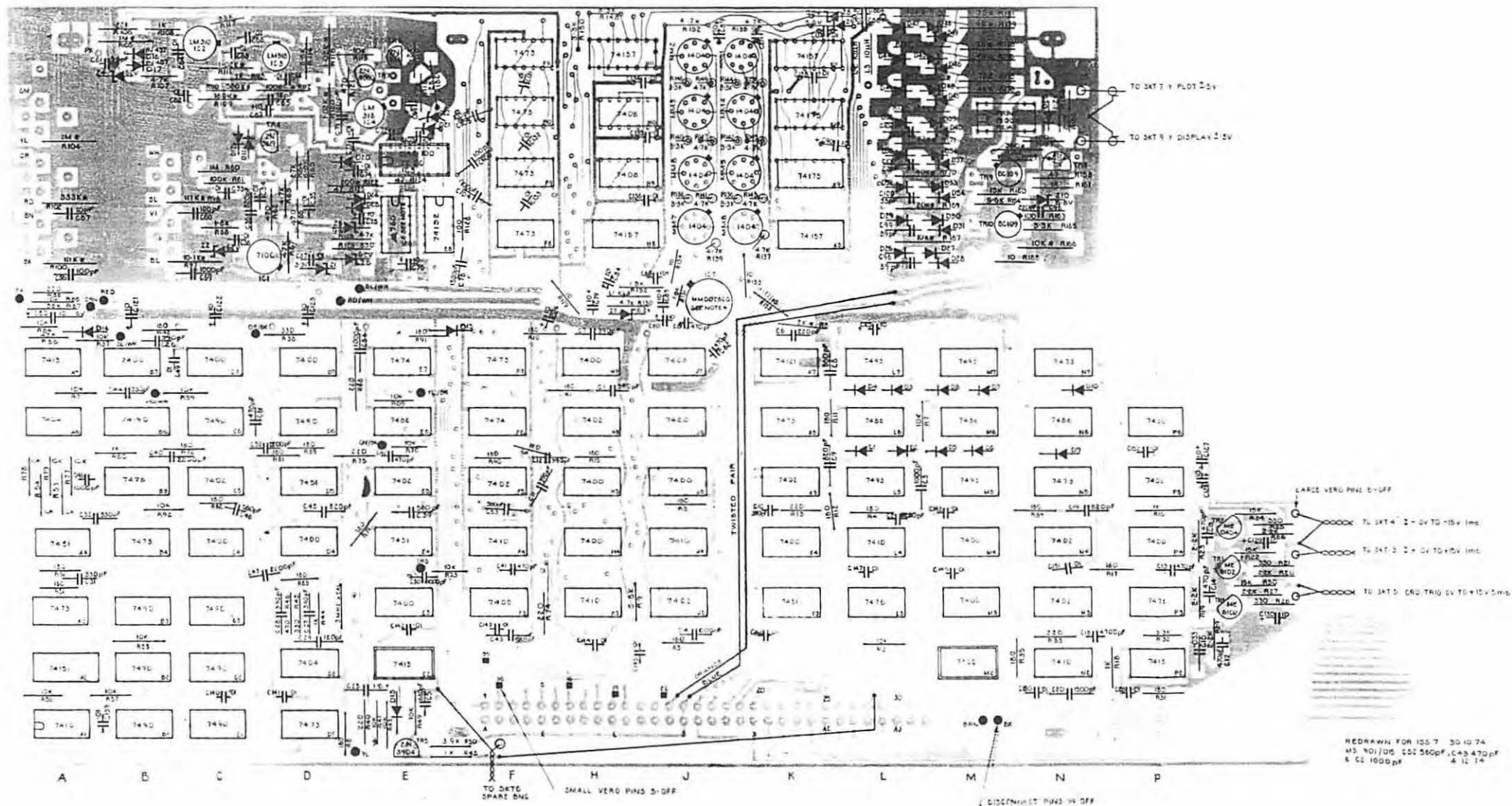


Figure 6-17a Printed circuit board - Topside (901/7)

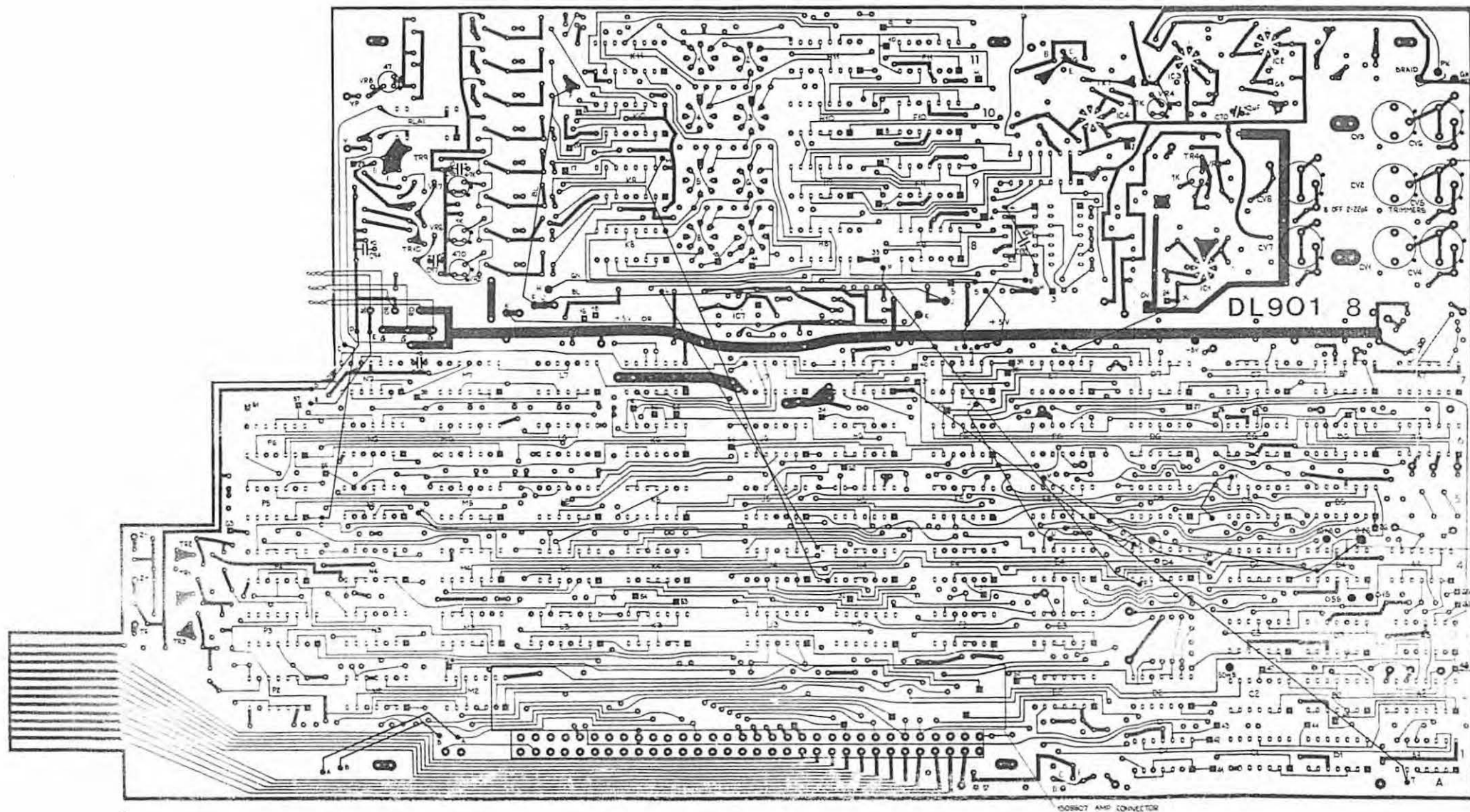


Figure 6-18b Printed circuit board — Underside (901/8)

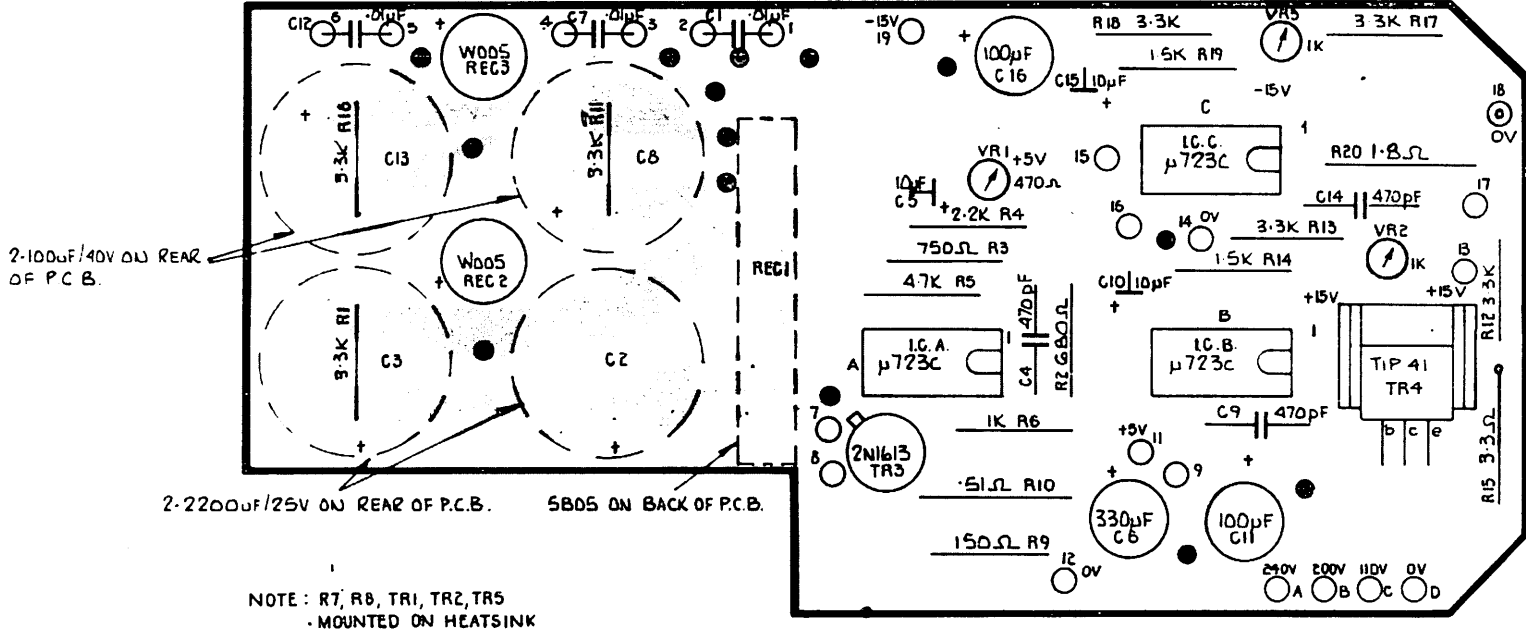


Figure 6-19 Power Supply Printed Circuit Board — Topside

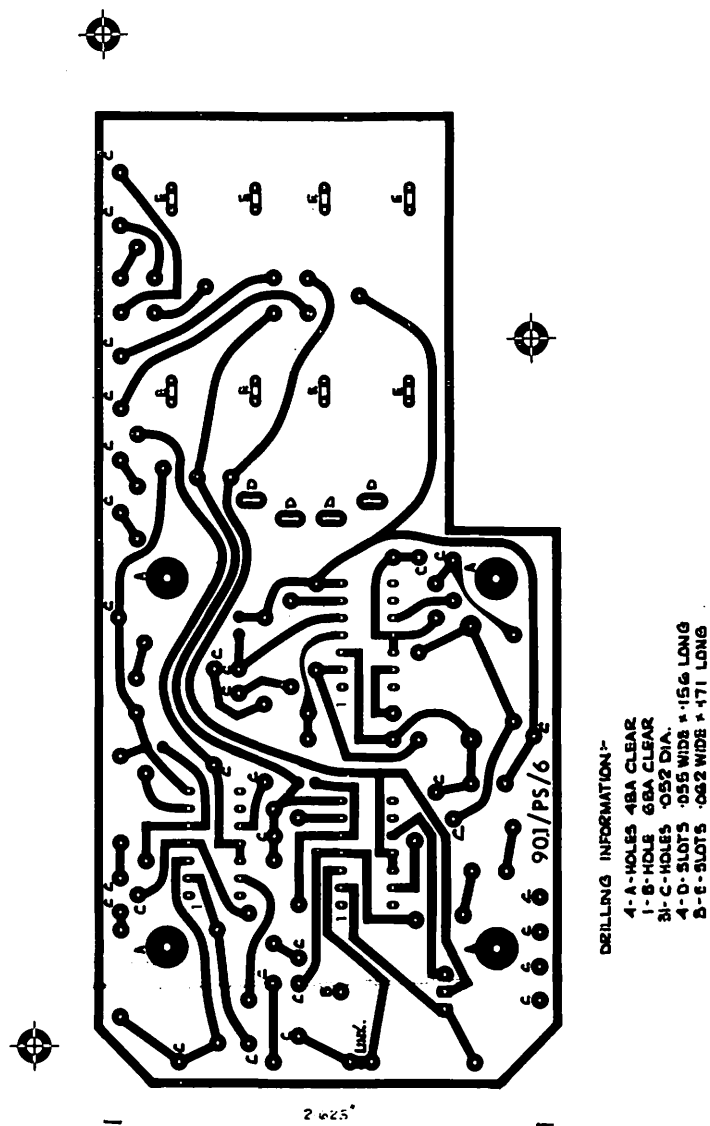


Figure 6-20 Power Supply Printed Circuit Board — Underside.

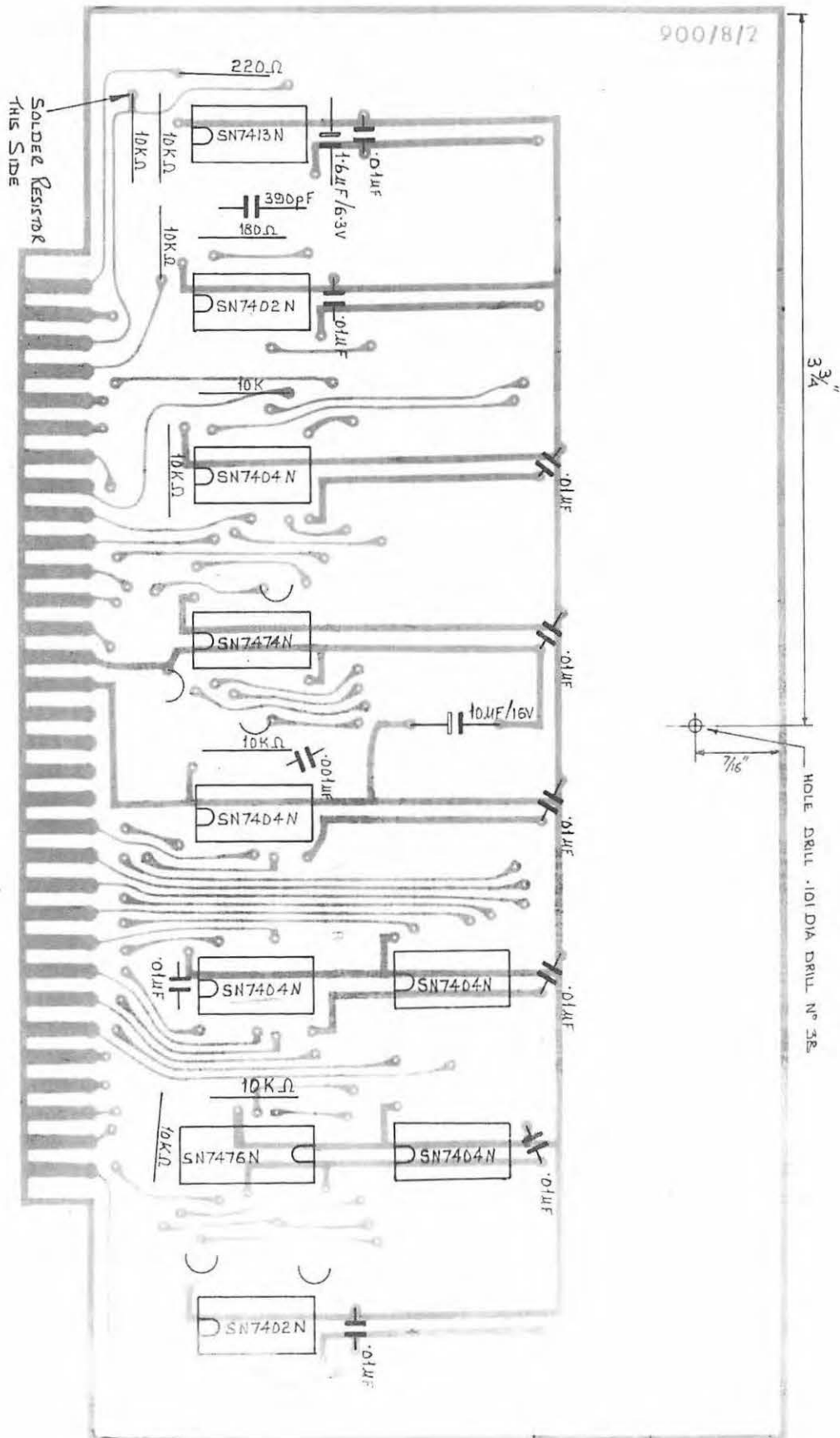


Figure 6-21 Interface Printed Circuit Board — Topside

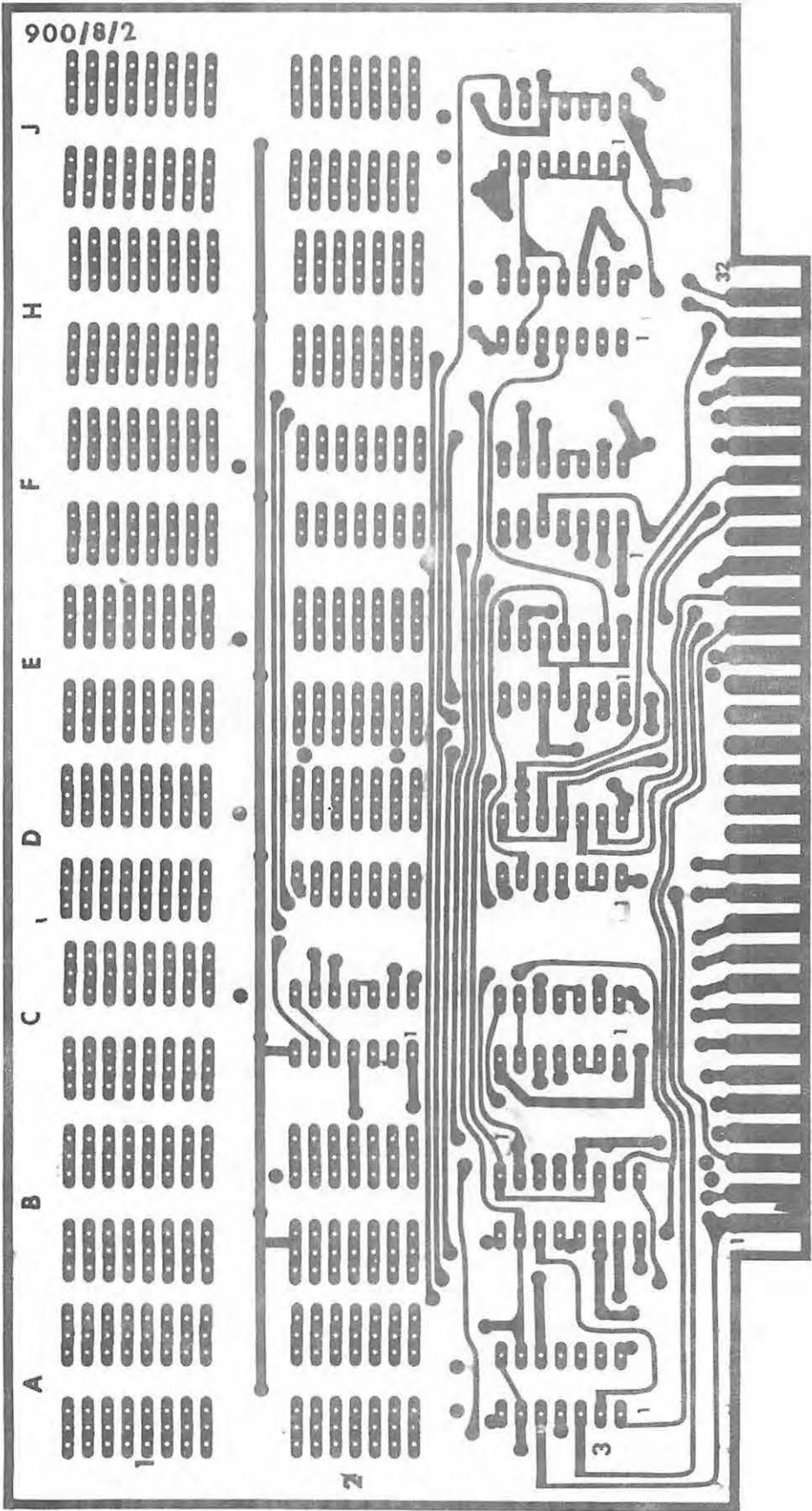


Figure 6-22 Interface Printed Circuit Board — Underside

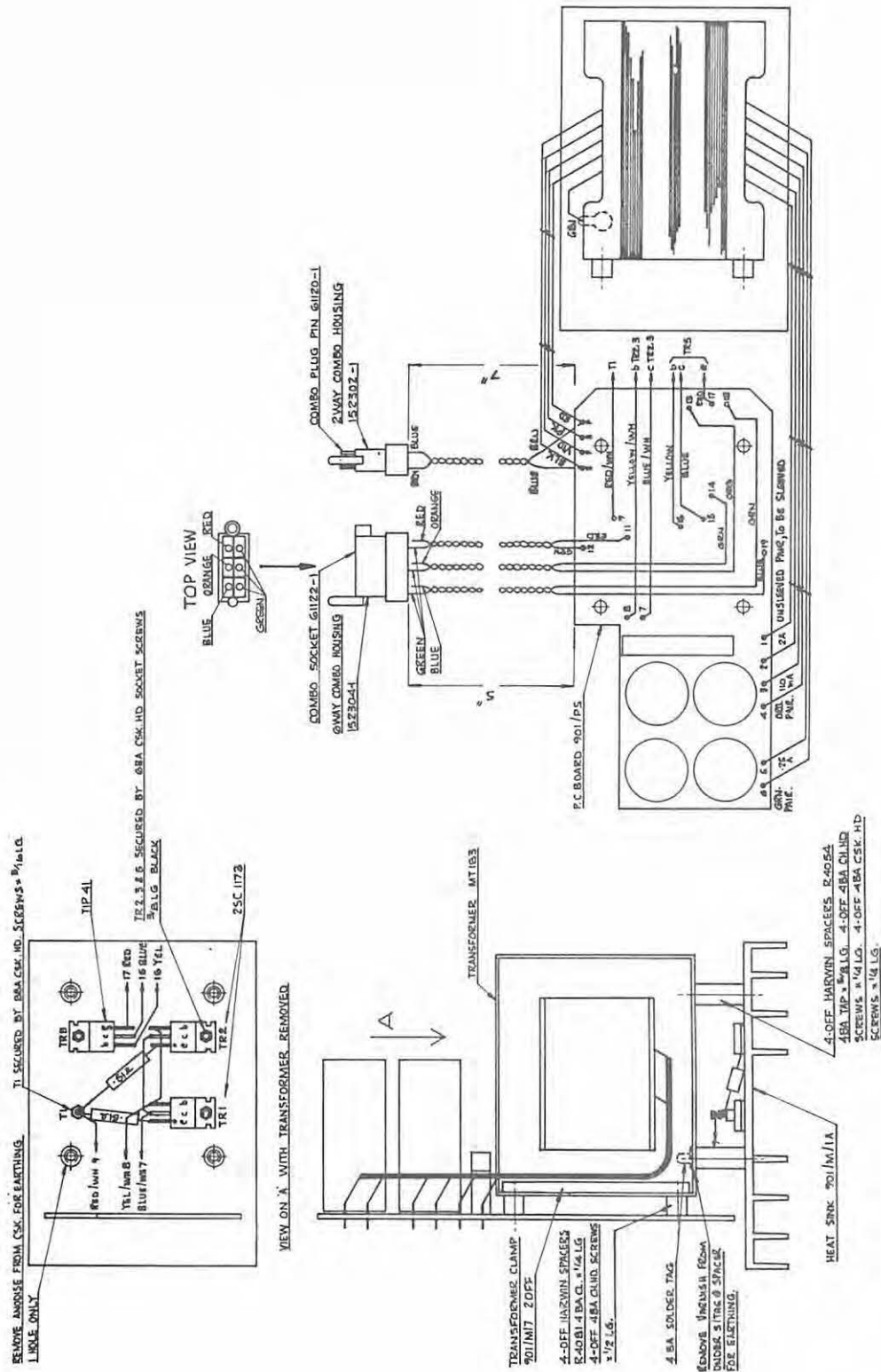


Figure 6-23 Power Supply Assembly and Wiring Diagram

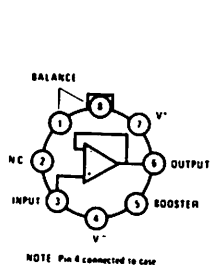
7 ADDITIONAL INFORMATION

7.1 SIGNAL INDEX

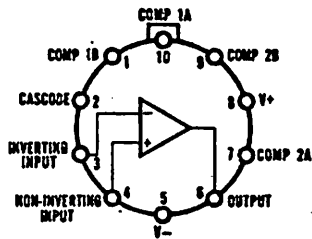
Test Point	Signal Name	Function	Signal Source	Cct. Sheet No. & Grid Ref.
1	AMPOUT	Non-inverting 0V/-5V F.S. pre-amp output.	IC3/6	1/D1
2	TAH	Track and hold circuit output.	IC4/6	1/D1
3	DISC	Negative true ADC discriminator output.	IC6/11	1/F1
4	CR8	Conversion register most significant bit.	F8/12	1/C2
5	CR7	Conversion register 2nd M.S. bit	F8/9	1/D2
6	CR6	Conversion register 3rd M.S. bit	F9/12	1/D2
7	CR5	Conversion register 4th M.S. bit	F9/9	1/D2
8	CR4	Conversion register 5th M.S. bit	F10/12	1/E2
9	CR3	Conversion register 6th M.S. bit	F10/9	1/E2
10	CR2	Conversion register 7th M.S. bit	F11/12	1/E2
11	CR1	Conversion register least significant bit.	F11/9	1/F2
12	CS	Demultiplexes CLOCK STORE to two phase clock drivers.	K6/9	1/B2
13	Ø2	MOS shift register clock phase 2	IC7/12	1/C3
14	Ø1	MOS shift register clock phase 1	IC7/10	1/C3
15	B8	Output buffer register most significant bit.	K9/3	1/C3
16	B7	Output buffer register 2nd MS bit	K9/6	1/D3
17	B6	Output buffer register 3rd MS bit	K9/11	1/D3
18	B5	Output buffer register 4th MS bit	K9/14	1/D3
19	B4	Output buffer register 5th MS bit	K10/3	1/E3
20	B3	Output buffer register 6th MS bit	K10/6	1/E3
21	B2	Output buffer register 7th MS bit	K10/11	1/F3
22	B1	Output buffer register least significant bit	K10/14	1/F3
23	Y OUT	Y axis digital-to-analog converter output 1V F.S.	TR8/e	1/C4
24	TRIGGER	Trigger discriminator output.	IC1/7	2/B2
25	ARM	Flip-flop set to arm 901.	F6/9	2/C2
26	DELAY	Flip-flop set for 901 delay period.	B5/11	2/B3
27	+1TDC	Negative transition increments delay counter.	E6/3	2/A3
28	DC 10	1st decade ($\div 10$) delay counter	D6/11	2/A3
29	DC 100	2nd decade ($\div 10$) delay counter	C6/11	2/B3
30	DE	Negative transition indicates end of delay period.	B6/12	2/B3
31	SWEEP	Flip-flop set when 901 recording.	B5/15	2/C3
32	STORE OUT	Set to allow store content to be recirculated.	H4/8	2/A4
33	ADCIN	Low to gate new samples into store.	D4/6	2/C4
34	SAM	Logical AND of SAMPLE and SWEEP flip-flops.	C5/1	2/C4
35	RESET ADDRESS	High to reset AC and N counters	D4/8	2/C4
36	RX	Low to initialise recorder	E5/4	2/D4
37	SAMPLE	Initiates A/D converter sequence	E7/5	2/D3
38	SYNC	Synchronises SAMPLE to 3MHz clock	E7/9	2/E3
39	$\div 2$	Produces Track/Hold changeover delay	F7/9	2/E3
40	CONVERT	Gates 3MHz clock to produce analog-to-digital converter pulses.	F7/12	2/E3
41	3MHz	Buffered oscillator output.	E5/13	2/D1
42	$\div 3$	With 1µs flip-flop divides 3MHz down to 1MHz.	D1/9	2/D1
43	1µs	1MHz output from $\div 3$ counter	D1/12	2/D1
44	5µs	5µs output from timebase divider.	C1/11	2/D1
45	50µs	50µs output from timebase divider.	B1/11	2/E1

Test Point	Signal Name	Function	Signal Source	Cct. Sheet No. & Grid Re.
46	,5ms	0,5ms output from timebase divider.	B2/11	2/E1
47	5ms	5ms output from timebase divider.	C2/11	2/E1
48	20ms	20ms output from timebase divider.	B4/9	2/E1
49	50ms	50ms output from timebase divider.	C3/11	2/F1
50	,2s	0,2s output from timebase divider.	B4/12	2/F1
51	,5s	0,5s output from timebase divider.	B3/11	2/F1
52	ADV	Buffered external advance input.	E2/8	2/F2
53	TS	Set for store access in recirculation modes.	L3/11	3/B1
54	AACN	Set to gate $\overline{AC}=\overline{NC}$ to produce $AC=N$.	L3/15	3/B1
55	AC=N	Equivalence of AC and N counters	J3/10	3/B2
56	CLOCK STORE	250ns mono shifts store data one place	K7/6	3/C1
57	AC10	Last Address Counter flip-flop	N7/9	3/E1
58	+1TN	Negative transition increments N counter.	H6/1	3/D2
59	NC10	Last N counter flip-flop	N5/9	3/E2
60	NC10S	Set on N counter overflow	K6/12	3/F2
61	$\overline{AC1K}$	Low when $AC=1000$ (1001 in PLOT).	P6/8	3/F2
62	PUNCH RATE	Set to access store in digital output	F6/5	3/C2
63	Z	High for 1st 1000 addresses to brighten CRO trace.	P3/15	3/B2
64	STROBE STORE	Positive transition sets store output buffer	M2/8	3/A3
65	TB1	With TB2 divides timebase output $\div 1, \div 2, \div 4$.	A3/9	2/E2
66	TB2	With TB1 divides timebase output $\div 1, \div 2, \div 4$.	A3/12	2/D2
—	TRIGP	Initialises 901 when triggered (ARM reset)	C5/13	2/C2
—	CYCLE A	High when 901 in record mode	D4/11	2/C4
—	SWP	Resets Address Counter at end of Pretrigger sweep.	C5/4	2/C3
—	2ms	Positive transition initiates store recirculation.	C2/9	2/E1
—	AC10P	Produced on Address Counter overflow	K5/1	3/F1
—	DIS	High when 901 in display mode	J3/4	3/B1
—	RECIRC	High when 901 recirculating store in record mode	K4/6	3/B2
—	RESET TB	High to reset timebase.	J4/8	3/C2
—	RPP	Terminates plot/punch mode	J4/12	3/D2
—	OUTPUT	High in plot/punch modes	P4/8	3/B2
REQ	REQ	Set when digital output requested	E3/5	} Interface 900/8
PUNCH	PUNCH	Set when digital output in progress	B3/11	
DRS	DRS	High indicates valid data at output connector.	E3/9	
PLOT	PLOT	Set when plot mode in progress.	B3/15	

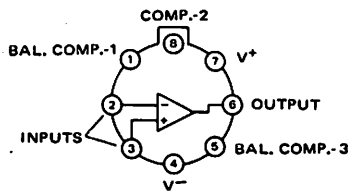
7.2 INTEGRATED CIRCUITS CONNECTION DIAGRAMS



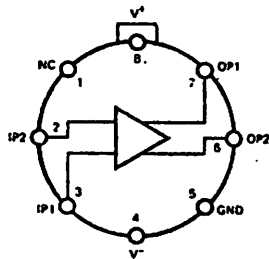
LM310 Voltage Follower



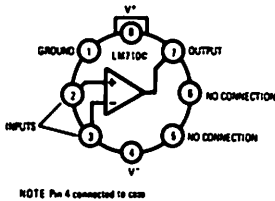
µA 715 [Fitted Early Units Only]



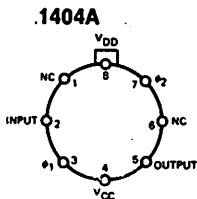
LM318 OPAMP [Used Currently]



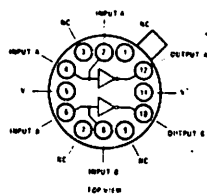
µA 760 Voltage Comparator



LM710C Voltage Comparator



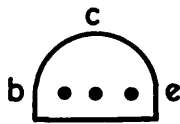
Dynamic Shift Register



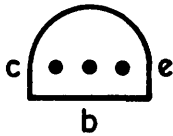
Dynamic Store Clock Driver

Note : All components viewed from top

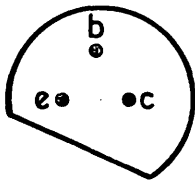
7.3 TRANSISTOR & FET CONNECTION DIAGRAMS



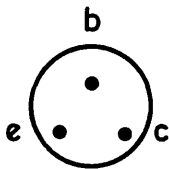
TIS48
(NPN)



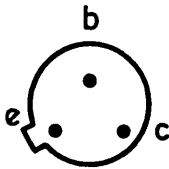
2N3904
(NPN)



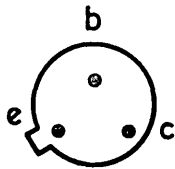
ME0404-2
(PNP)



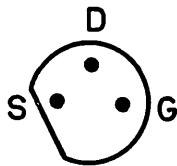
ME6102
(NPN)



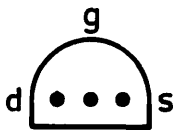
BC109
(NPN)



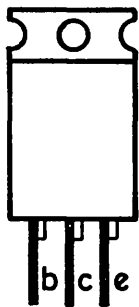
2N1613
(NPN)



2N4360
FET P CHANNEL



2N3819
FET N CHANNEL



TIP41
(2SC1173)
(NPN)

Note : All components viewed from bottom.

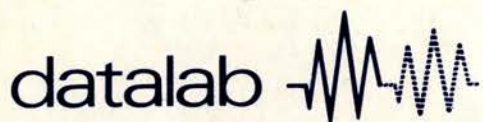
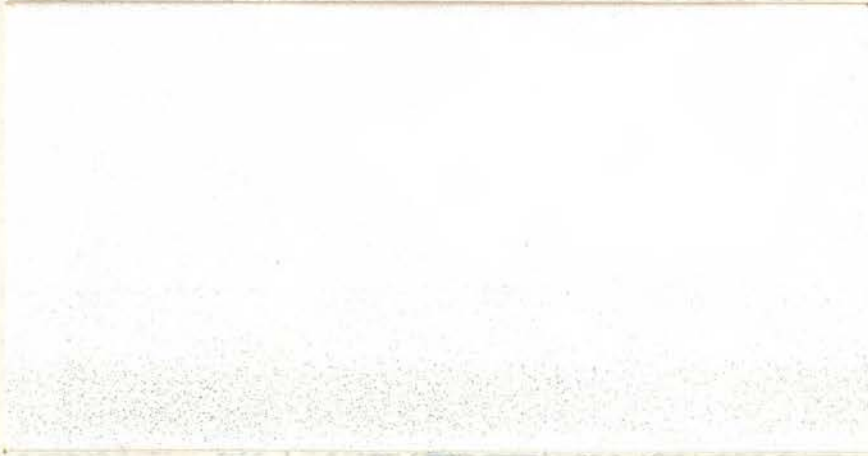
BAE DUNSFOLD
ASD 212
2 OF 3

81372

TECHNICAL INFORMATION

ASAP

157934

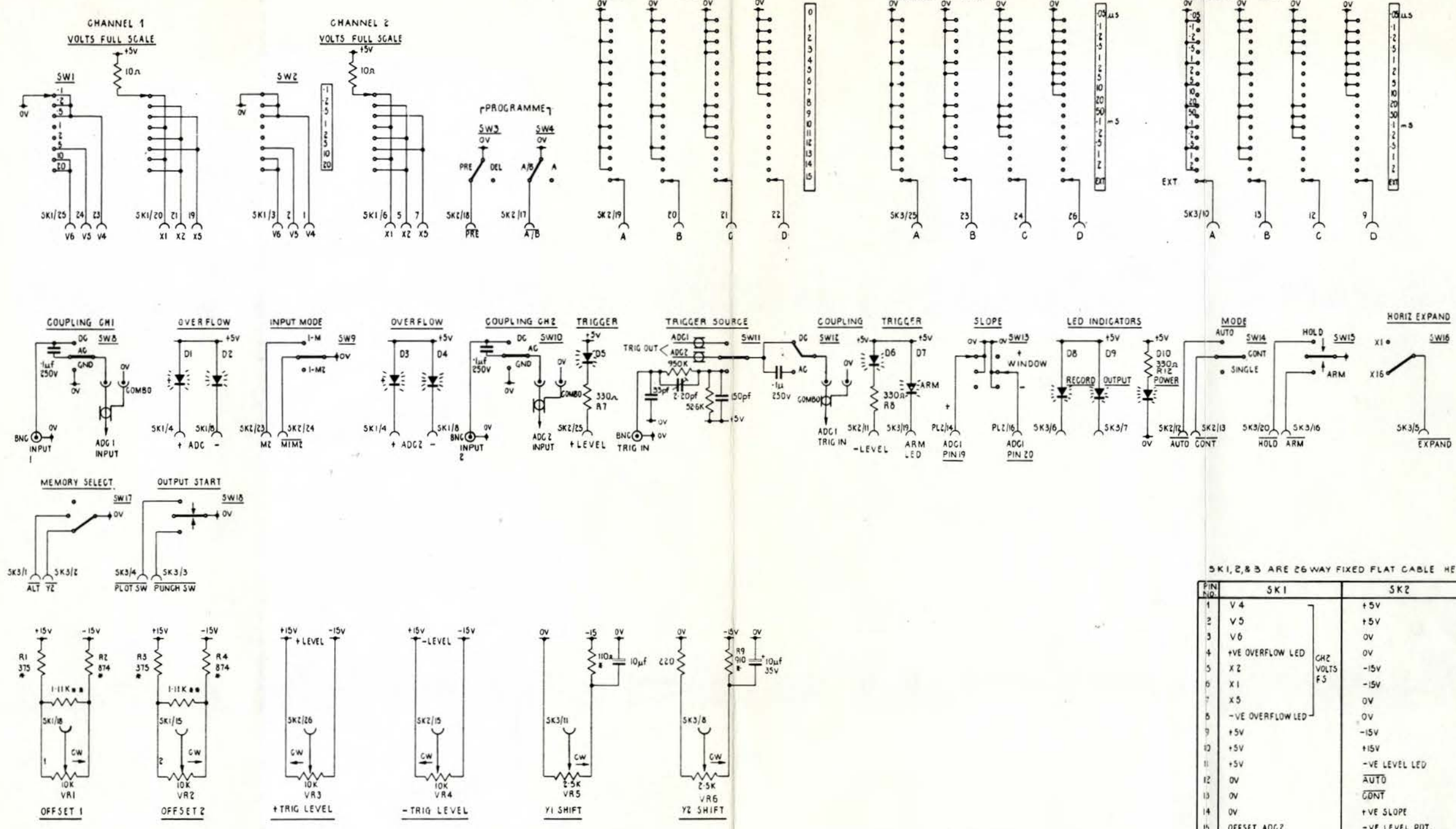


DL910, DL912
TRANSIENT RECORDERS
CIRCUIT DIAGRAMS

14.9.82.

DL910, DL912 CIRCUIT DIAGRAMS

Number	Description
910/1/3	FRONT PANEL
910/2/3 Sht 1	CONTROL & TIMEBASE
" Sht 2	MEMORY ADDRESSING
" Sht 3	DISPLAY
910/2/4 Sht 1	CONTROL & TIMEBASE
" Sht 2	MEMORY ADDRESSING
" Sht 3	DISPLAY
910/3/1,2	PRE AMP, ADC & TRIGGER
910/4/1	4K8 MEMORY
910/6/1,2	900/GPIB/IO INTERFACE OPTION
900/8/6,7 &8	STD. BINARY TTL INTERFACE
910/PS/1	POWER SUPPLY
910/A/7	MECHANICAL ASSEMBLY



SK1, 2, 3 ARE 26 WAY FIXED FLAT CABLE HEADERS

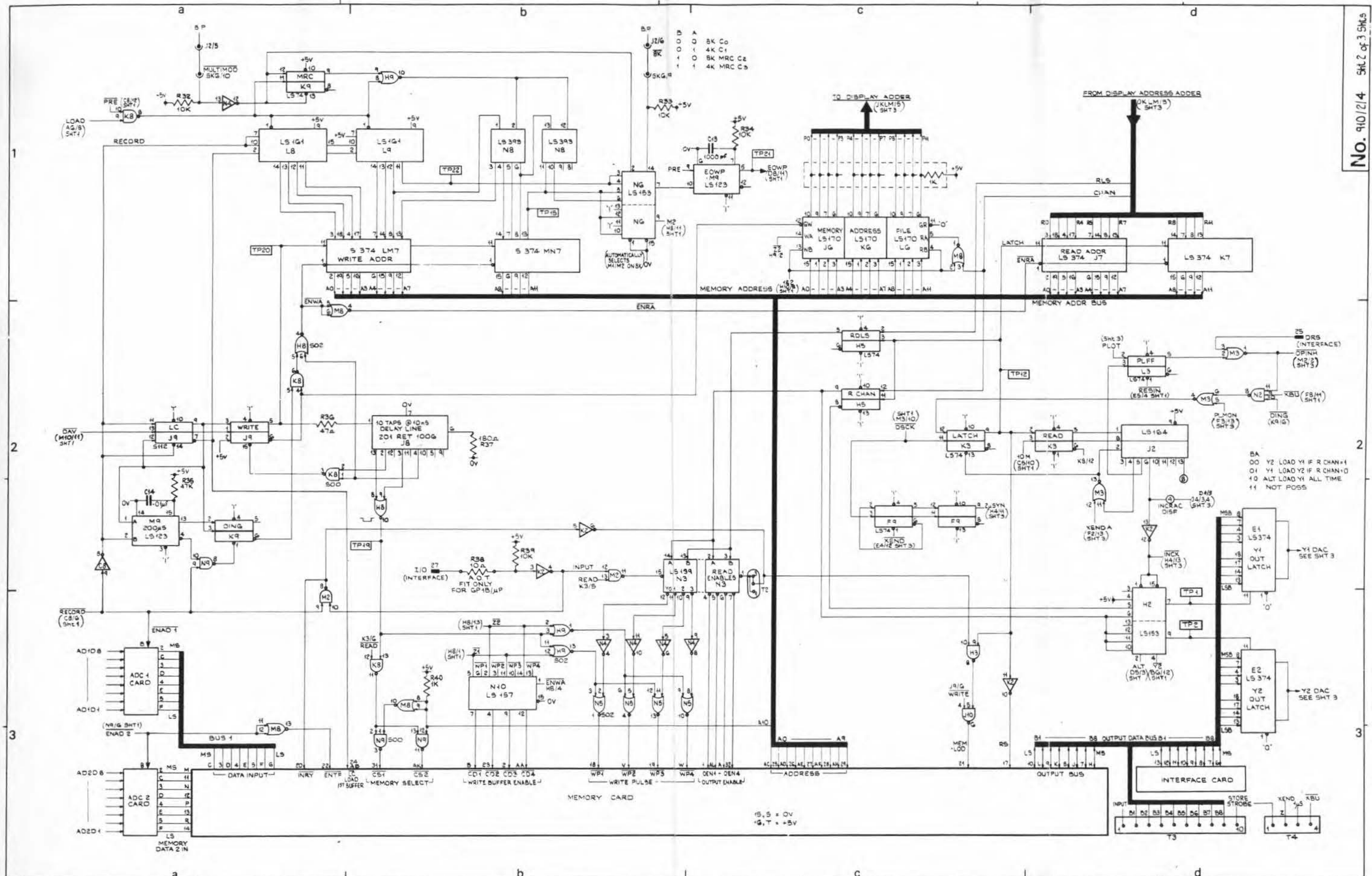
PIN NO.	SK1	SK2	SK3
1	V4	+5V	ALT
2	V5	+5V	Y2
3	V6	0V	PUNCH SW
4	+VE OVERFLOW LED	0V	PLOT SW
5	X2	-15V	EXPAND
6	X1	-15V	RECORD LED
7	X3	0V	OUTPUT LED
8	-VE OVERFLOW LED	0V	Y2 SHIFT POT.
9	+5V	-15V	D] SAMPLE B SW.
10	+5V	+15V	A]
11	+5V	-VE LEVEL LED	Y1 SHIFT POT.
12	0V	AUTO	C] SAMPLE B SW.
13	0V	CONT	B]
14	0V	+VE SLOPE	0V
15	OFFSET ADG2	-VE LEVEL POT.	0V
16	0V	-VE SLOPE	ARM
17	0V	A/B	+5
18	OFFSET ADG1	PRE	+5
19	X5	A]	ARM LED
20	X1	B] DELAY SW	HOLD
21	X2	C]	NG
22	+VE OVERFLOW LED	D]	NG
23	V4	M2	B]
24	V5	M1 M2	C] SAMPLE A SW.
25	V6	+VE LEVEL LED	A]
26	-VE OVERFLOW LED	+VE LEVEL POT.	D]

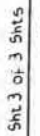
material		title	
finish		DL 910/912 FRONT PANEL SWITCHES	
scale			
all dimensions in millimetres			
tolerance unless stated - 0.4			
1 MAR 82	date		
alterations			


drawn
checked
sagrowed

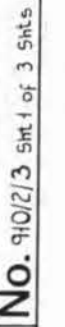
datalab

No. 910/1/2




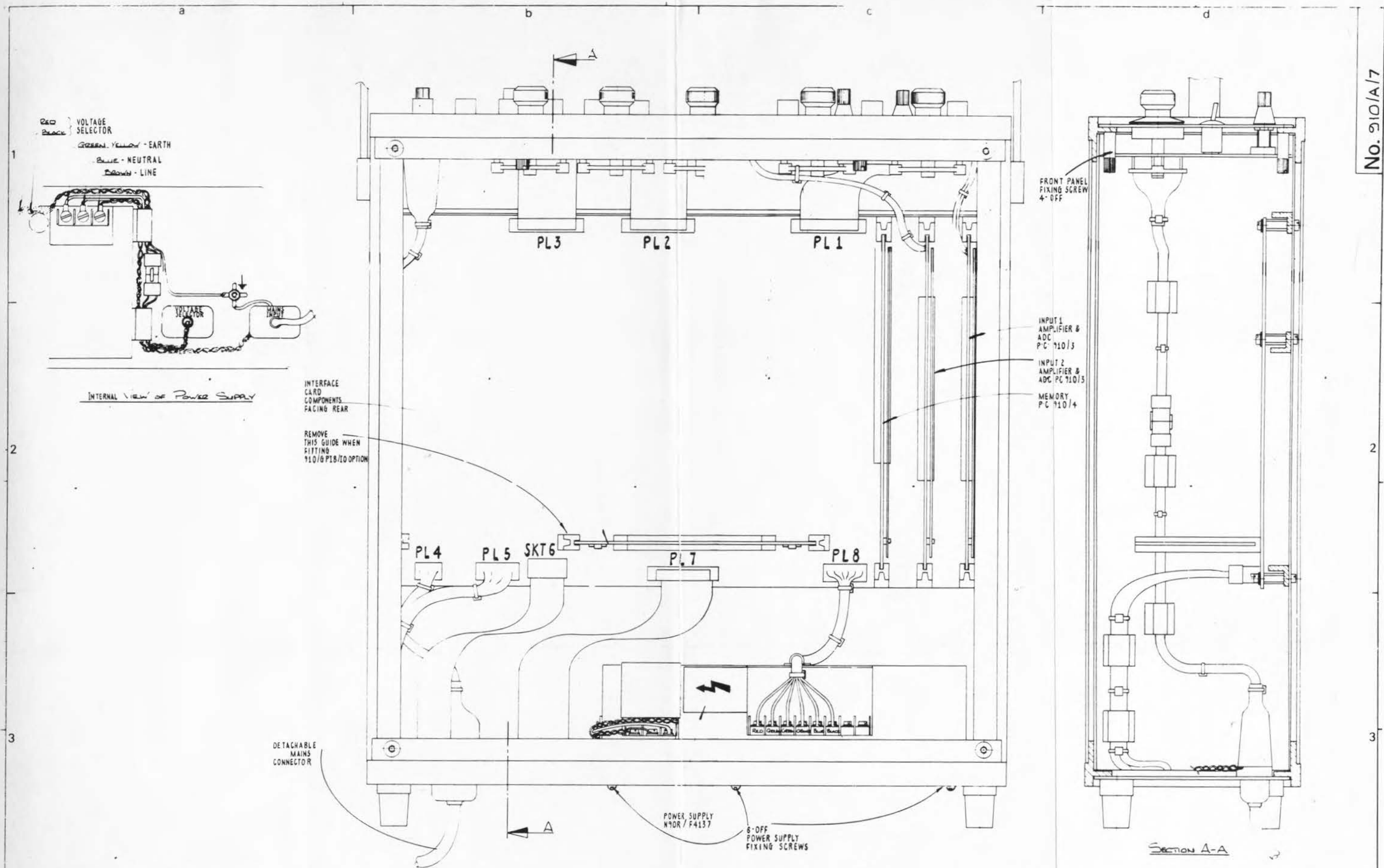
NO. 937/2/3

drawn	
DAQ	
traced	
checked	
approved	No. 000/000




			material
			finish
3	8-1-82	MO 940/015	scale
4		HOLES FOR T1, T2 & T3 ADDED UPDATED TO ISSUE 3	
1	17.0.81		all dimensions tolerance unless
100	date	alterations	

drawn DAG	
traced	
checked	
approved <i>[Signature]</i>	
No. 940/2/3 Sht 1 of 3 Shts	

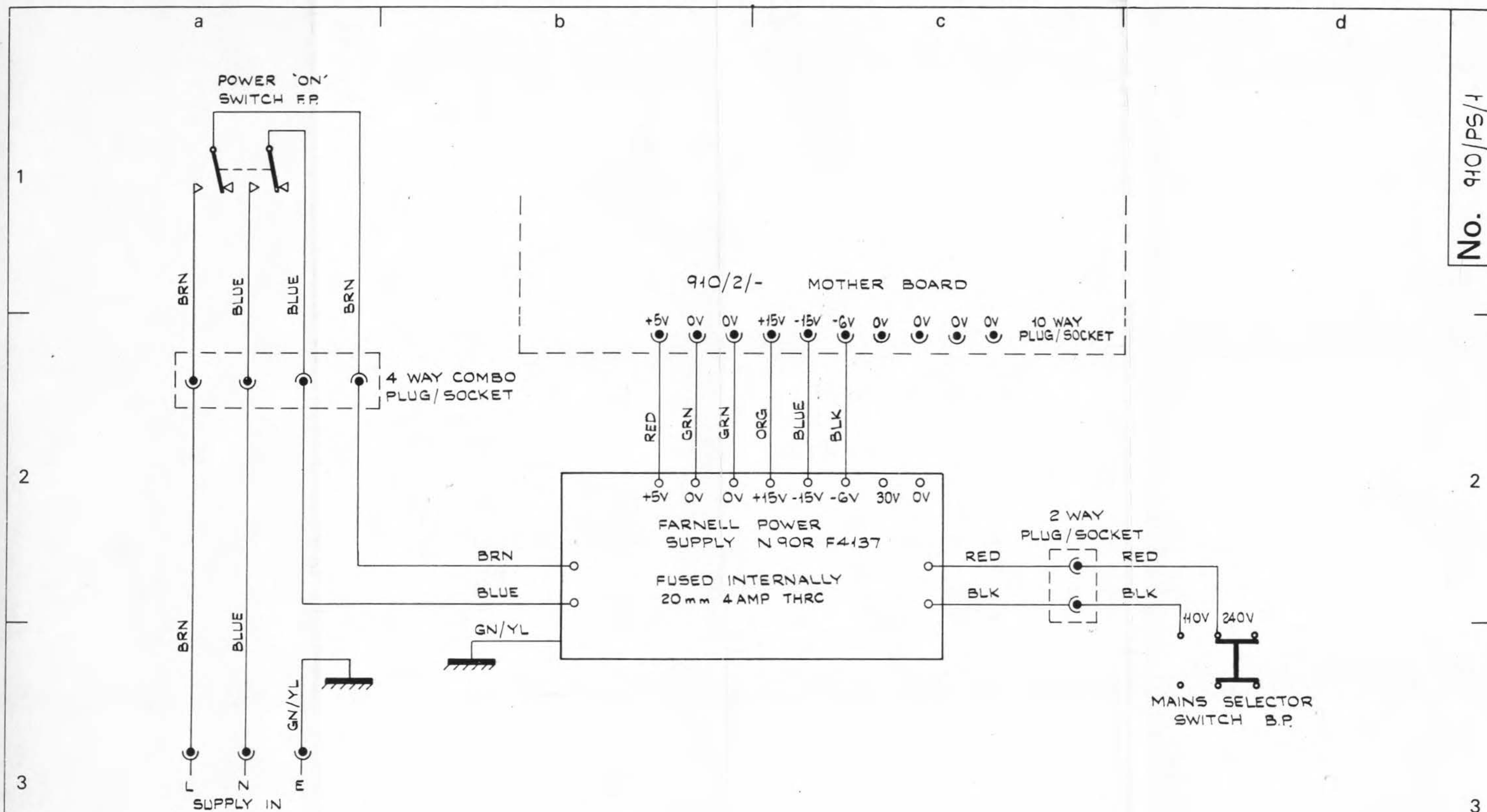


a		material	b		c		d
		finish					drawn AJT
		scale Full Size					traced
		all dimensions in millimetres tolerance unless stated ± 0.4					checked
1	MARCH 82						approved
ISS	date	alterations					

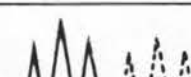
DL 910/912 MECHANICAL ASSEMBLY

datalab 
 No. 910/A/7

No. 910/A/7



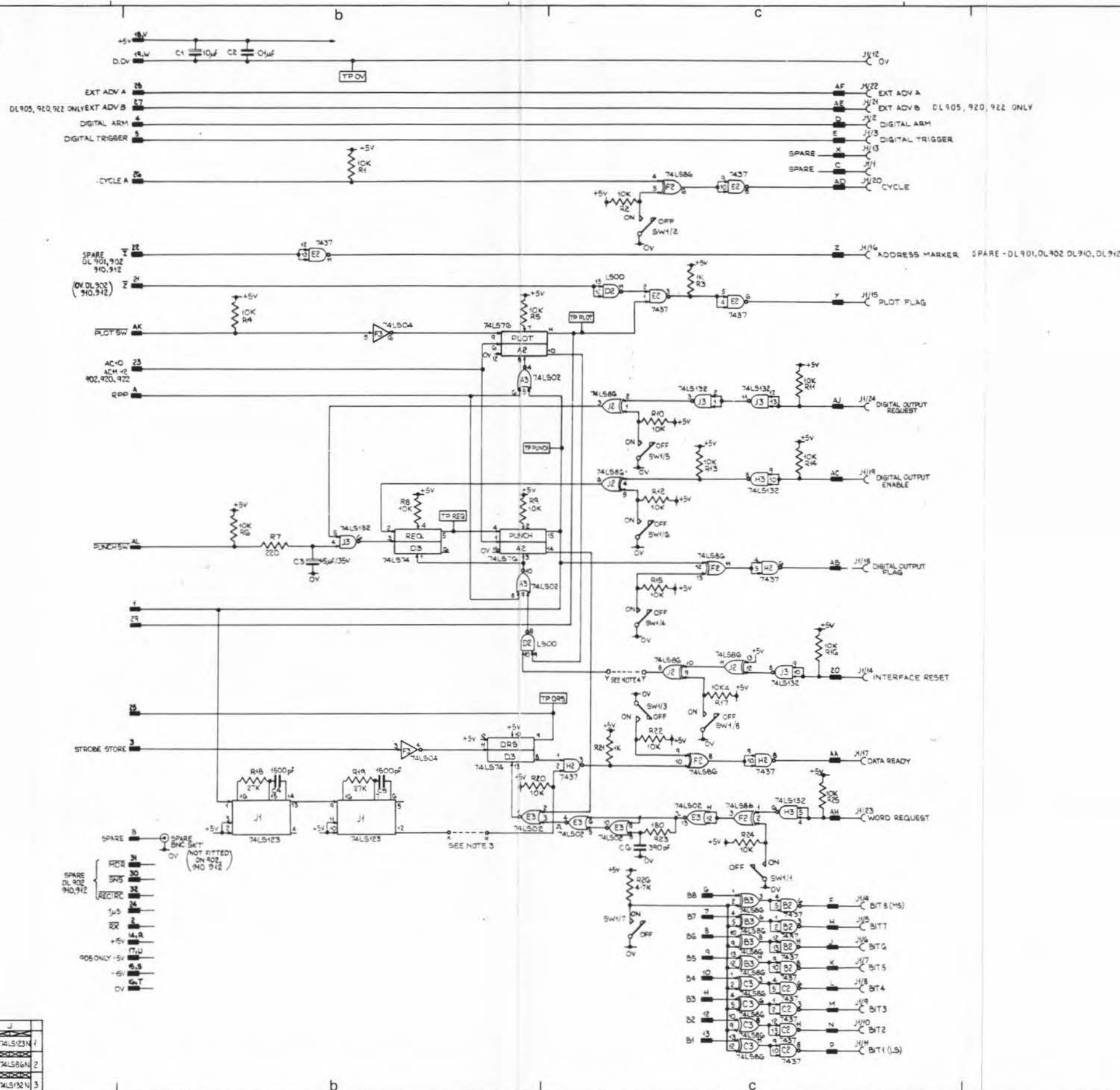
No. 910/PS/1

a			b		c		d	
			material	/	910/912 MAINS WIRING		drawn	
			finish	/			traced	
			scale	/			D.A.G.	
			all dimensions in millimetres				checked	
			tolerance unless stated ± 0.4				approved	
1	7-5-82							No. 910/PS/1
ISS	Date	alterations						

1. SW1 'ON' POSITION	SELECTS GROUND TRUE LOGIC NOTATION
SW1 'OFF' POSITION	SELECTS POSITIVE TRUE LOGIC NOTATION
2. SIGNAL	SWITCH 1 ROCKER NO
WORD REQUEST	1
CYCLE	2
DATA READY	3
DIGITAL OUTPUT FLAG	4
DIGITAL OUTPUT REQUEST	5
DIGITAL OUTPUT ENABLE	6
DATA BITS 1-6	7
INTERFACE RESET	8
NOT USED	9
NOT USED	10

LINK HOLES XX TO GENERATE DATA READY
RESPONSE TO WORD REQUEST TERMINATING
OUTPUT - SEE ALSO INTERFACE OPERATING
INSTRUCTIONS

4. LINK HOLES YY TO ENABLE INTERFACE RESET SIGNAL - SEE ALSO INTERFACE OPERATING INSTRUCTIONS.



● DENOTES SIGNAL SOURCE		MK II TTL OUTPUT INTERFAC	
9008/16			
32	AL		
31	RECEIVE	BLACK	FP
30	TX	TX	FP
29	TX	TX	FP
28	TX	TX	FP
27	TX	TX	FP
26	TX	TX	FP
25	TX	TX	FP
24	TX	TX	FP
23	TX	TX	FP
22	TX	TX	FP
21	TX	TX	FP
20	TX	TX	FP
19	TX	TX	FP
18	TX	TX	FP
17	TX	TX	FP
16	TX	TX	FP
15	TX	TX	FP
14	TX	TX	FP
13	TX	TX	FP
12	TX	TX	FP
11	TX	TX	FP
10	TX	TX	FP
9	TX	TX	FP
8	TX	TX	FP
7	TX	TX	FP
6	TX	TX	FP
5	TX	TX	FP
4	TX	TX	FP
3	TX	TX	FP
2	TX	TX	FP
1	TX	TX	FP

No 900/8/6 & 7.8

2

3


A	B	C	D	E	F	G	H	I	J
									SN74LS02N
SN74LS76N	SN74S77N	SN74S77N	SN74LS00N	SN74S77N	SN74LS06N	SN74S77N	SN74LS86N		
SN74LS02N	SN74LS06N	SN74LS06N	SN74LS74N	SN74LS02N	SN74LS04N	SN74LS32N	SN74LS32N		

			material
			finish
2	18-5-88	MS500/158	scale
1	4-5-76		all dimensions in millimetres tolerances stated ± 0.4
see	date	alterations	

DL 900 SERIES TRANSIENT RECORDERS - OUTPUT INTERFACE - STANDARD BINARY-TTL VERSION MK II

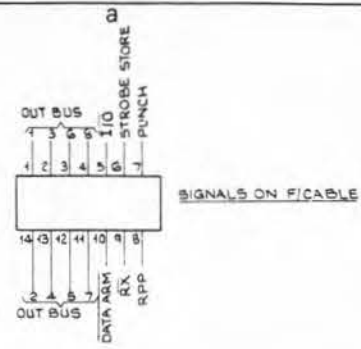
DL 904, 902, 910, 912 - INTERFACE CARD POSN. DL 905 - CARD POS'N 13. DL 920 - CARD POS'N 9. DL 922 - CARD POS'N 9.

drawn
traced
checked
approved

datalab 

No. 900/8/647,8

M



910 DATA BUS → 88 87 86 85 84 83 82 81
9 8 7 6 5 4 3 2 1

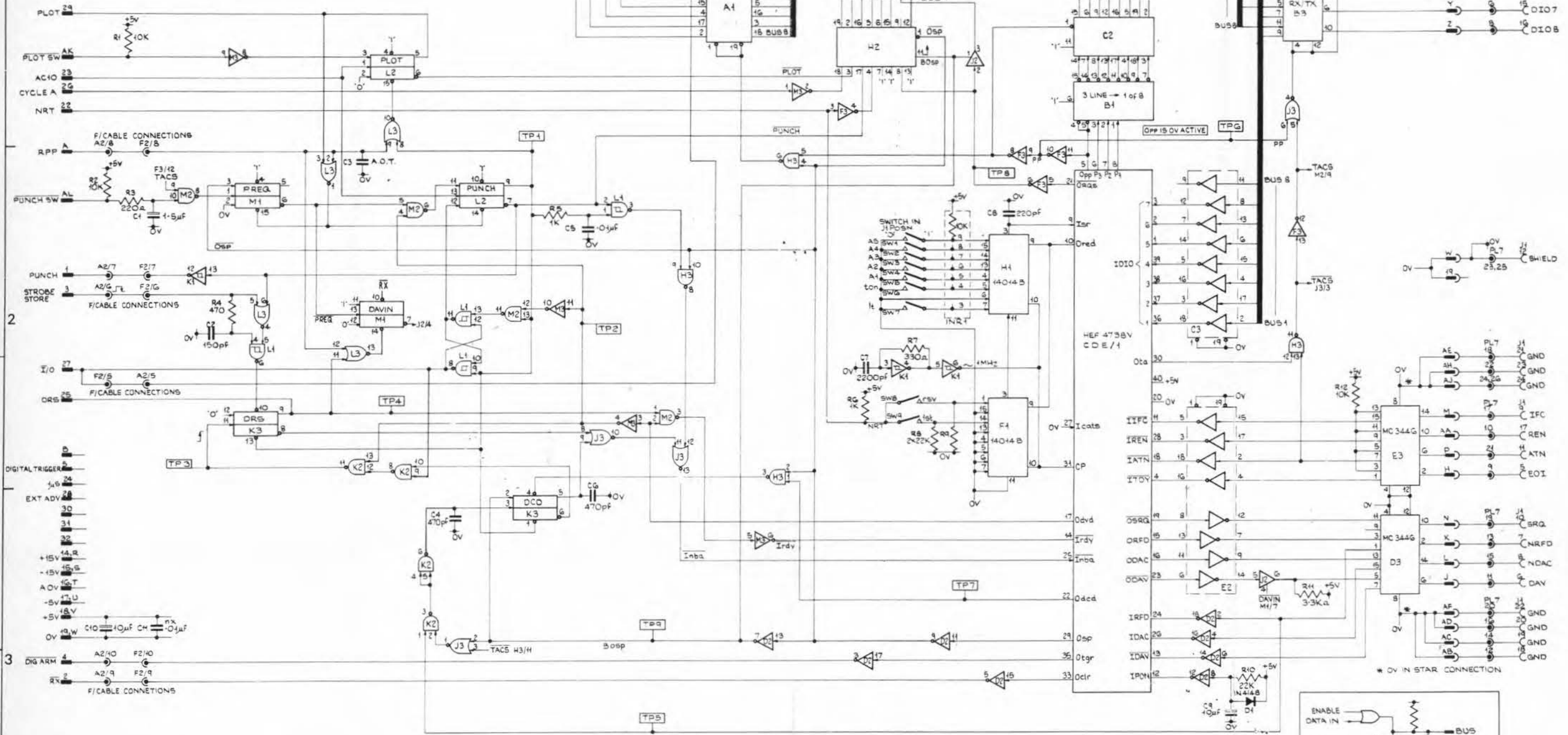
INBUS

OUTBUS

FLAT CABLE CONNECTIONS

(910) B.P.
J1 (LS)
DIO 1
DIO 2
DIO 3
DIO 4
DIO 5
DIO 6
DIO 7
DIO 8

No. 910/6/1 & 2,3



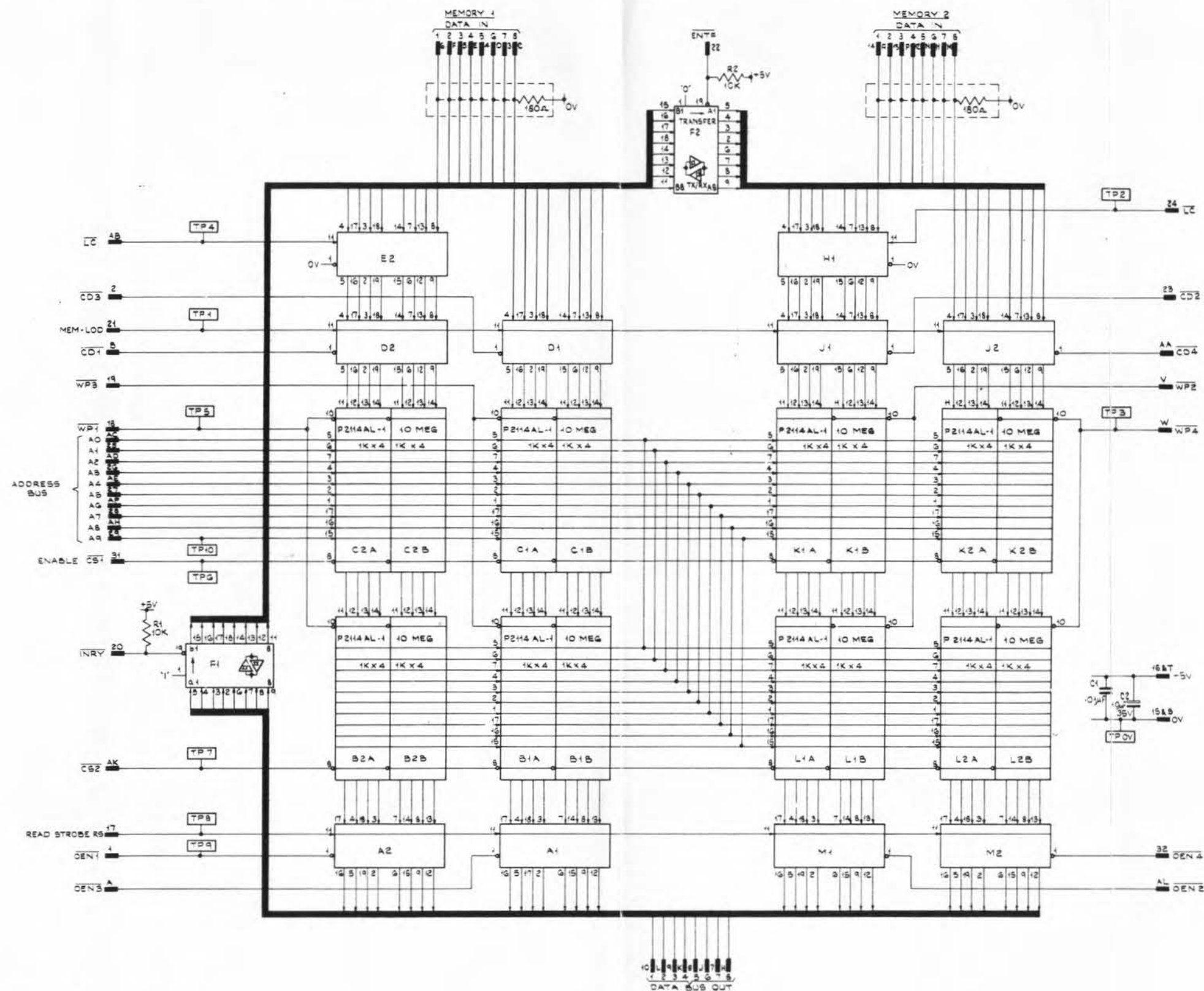
A	B	C	D	E	F	G	H	I	J	K	L	M
LS 240	LS 138	HEF 4738V	44014B	44014B	44014B	44014B	44014B	44014B	44014B	44014B	44014B	44014B
F/CABLE	344G	LS 373	LS 240	LS 240	F/CABLE	LS 374	LS 12G	LS 500	LS 142	LS 500	LS 500	LS 500
LS 240	344G	LS 240	344G	344G	LS 04	LS 00	LS 02	LS 74	LS 02	LS 04	LS 04	LS 04

910/912 GPIB IEEE 488 1978 BUS INTERFACE - OPTION 900/GPIB/IO

drawn D.A.G.
traced
checked
approved

datalab

No. 910/6/1 & 2,3




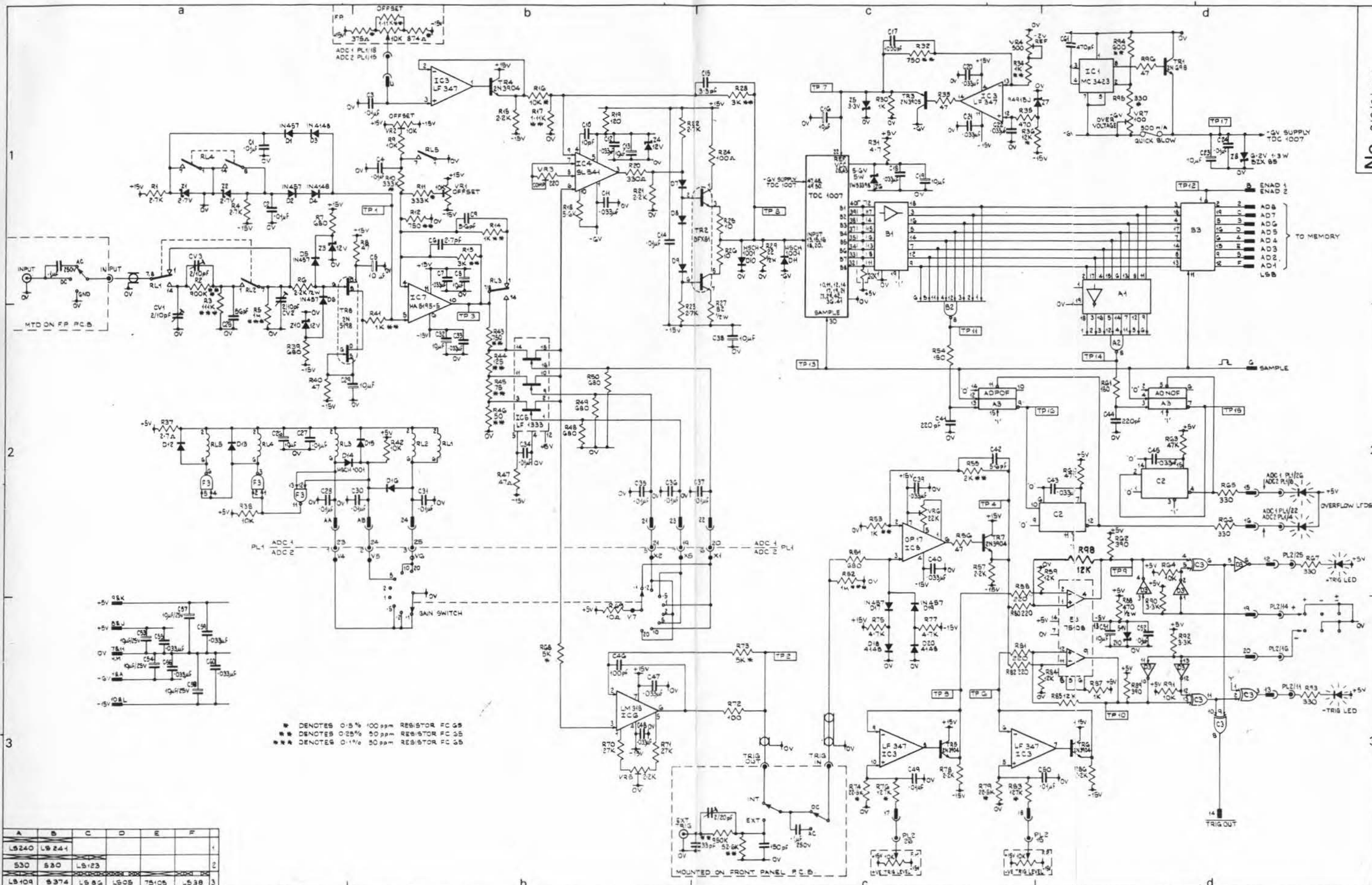
A	B	C	D	E	F	H	J	K	L	M
SN74LS374N	P2H4AL-1	P2H4AL-1	SN74LS374N		SN74LS245N	SN74LS374N	SN74LS374N	P2H4AL-1	P2H4AL-1	SN74LS374N
	P2H4AL-1	P2H4AL-1						P2H4AL-1	P2H4AL-1	
SN74LS374N	P2H4AL-1	P2H4AL-1	SN74LS374N	SN74LS374N	SN74LS245N		SN74LS374N	P2H4AL-1	P2H4AL-1	SN74LS374N
	P2H4AL-1	P2H4AL-1						P2H4AL-1	P2H4AL-1	

material	title
finish	
scale	
all dimensions in millimetres tolerance unless stated ± 0.4	
1 27-4-81	
iss date	alterations

20 MEG MEMORY
2 off 4K x 8

drawn
traced
checked
approved

datalab 
No. 910/4/1



A	B	C	D	E	F
LS240	LS241				1
530	530	LS123			2
LS109	LS374	LS86	LS05	75105	LS38

material	finish	scale	all dimensions in millimetres tolerance unless stated ± 0.4
3 AUG 82 CR 249			
2 17.9.81			
1 23-3-81			
iss date			

1 CHANNEL 20 MEG
PRE-AMP, ADC AND TRIGGER

drawn	J. A. G.
traced	
checked	
approved	
datalab	
No. 910/3/1 & 2	

No. 910/3/1 & 2

