PRC 420

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420 TEAM

SERVICE MANUAL
FOR
PRC420 HF TRANSCEIVER

Volume 2
3rd. Line Servicing

P.D.L.

630/HA/38180-3

SERVICE MANUAL

FOR

PRC420 HF TRANSCEIVER

VOLUME 2

CONTENTS

PART	TITLE
3	Third line servicing

P.D.L.

630/HA/38180-3

SERVICE MANUAL

FOR

PRC420 HF TRANSCEIVER

PART 3

THIRD LINE SERVICING

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THIRD LINE SERVICING

OF

PRC420 HF TRANSCEIVER

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INTRODUCTION

1. Part 3 of the service manual gives information additional to that given in Parts 1 and 2 such that Parts 1, 2 and 3 together with the test procedures given in Part 4 provide all the information required by a third line servicing technician.

2. The subject matter of this part of the manual is sub-divided into fourteen sections as follows:

(1) Section 1 (this section): gives general and specific information common to all fourteen sections.

(2) Section 2: gives specific information on the transceiver which may be required to effect repair of the radio at third line and includes a point-to-point wiring schedule for the unit.

(3) Sections 3 to 14: each detail one module which can be separately tested at third line, and which may well be sent to third line for repair as a separate item. Each section includes a circuit description, a list of components, and a layout drawing showing the location of individual components in the module.

REPAIR POLICY

3. Repair at third line will consist of the reinstatement of faulty equipment, assembly or module by the replacement of faulty component parts.

4. Any item which cannot be repaired at third line should, in accordance with local instructions, either be scrapped or returned to the manufacturer for repair. Items returned to the manufacturer should be packed in the container in which the replacement was received.

5. The provision (in Part 4) of test procedures for each module should not be taken to imply that a complete transceiver returned to third line for repair should automatically be disassembled before subjecting the unit to any tests.

REPAIR TECHNIQUES

6. The following paragraphs provide a guide to techniques employed in the replacement of defective components, the repair of printed circuit boards (pcb's), and some special precautions which should be observed when handling static sensitive devices, such as MOS components.

CAUTION ...

1. DC voltages in excess of 3V must not be applied to any circuit unless otherwise stipulated.

2. Buzzer circuits must not be used for continuity or any other test under any circumstances.

Soldering

7. Excess heat can damage insulation, components, etc. For all soldering and unsoldering operations, use a heat controlled iron set at 325°C ± 25°C and apply the heat for no more than 5 seconds. A tool which removes excess solder must be employed.

8. For all soldering use solder, resin cored, 60/40 tin lead Type 1 to British Standard BS441.

Preliminary inspection - printed circuit boards

9. Examine the pcb for:

(1) Damage and deterioration, including scorching, cracking and distortion.

(2) Short circuits between adjacent printed conductors and between wiring posts and adjacent conductors, caused either by an excess of solder or by the presence of dirt.

(3) Physical damage to the printed conductors, sufficient to cause open circuits to exist or develop.

(4) Loose or damaged wiring posts.

(5) Loose or damaged components mounted on the pcb.

Repair of printed circuit boards

10. When fitting a component to a printed circuit board the following procedure should be observed:

(1) Prior to soldering, clean the areas to be soldered using the minimum amount of cleaning fluid, (see para.11). Allow the area to dry before proceeding.

(2) If an insulating pad was used to separate the body of the original component from the panel, check that this pad is still serviceable, if necessary use a new pad.

(3) Position the component, including insulating pad if required, in its appropriate location on the panel.

(4) Solder the connections between the component and the panel taking care that neither too little nor too much solder is used. In particular, ensure that the solder does not reduce, or close, the gap to an adjacent track.

(5) Crop excess wire.

(6) Remove flux residue by the cleaning procedure given in sub-para.(1).

11. The recommended cleaning fluid is trichlorotrifluoroethane. Common proprietary names are Freon, Isceon 113 and Arklone P.

Replacing MOS components

12. Some of the integrated circuits used on the pcb's in this unit are MOS components, and are therefore static sensitive devices. These components, which are identified in the components lists in Sections 3 to 14, should be protected from the damage caused by voltages associated with electro-static charge. The following recommendations cover the necessary precautions which should be taken.

(1) Packaging. Each MOS component should be individually packaged, with all leads shorted together and/or in a protective conductive package, eg. a transparent bag of conductive plastic. Note that most plastic materials are not conductive.

(2) Labelling. Each package containing an MOS component should carry a label which identifies the component as an MOS device, otherwise the component may be damaged by lack of the necessary precautions during handling or by unauthorised testing.

(3) Special working conditions. The following special conditions are necessary wherever the repairing of pcb's involves the changing of MOS components:

(a) Proximity to machines such as RF generators, and welding machines should be avoided.

(b) Operator contact with any cable, conduit or apparatus with a supply in excess of 24V ac should be avoided.

(c) Work-bench, floor, seat cover and operator foot-rest should all have conductive mat cover (not bare metal) and should all be grounded, together with any other fixtures and equipment within reach of the operator. Single point earthing is preferred. The operator should wear a quick release skin contact (eg. wrist strap) with leakage resistance to ground of between 100k and 1M ohms and should not wear static generating outer clothing (such as nylon).

(4) Acceptance inspection. This should be limited to verification of identity and quantity, without removal from the manufacturer's package.

(5) Assembly procedures and precautions.

(a) Before removing an MOS component from its conductive package, the operator should hold the package and simultaneously touch the bench top to dissipate any electrostatic charge.

(b) If a pre-forming tool is used to shape the leads, the tool should be electrically bonded to the bench top.

(c) A low voltage soldering iron, with earth tip, and isolated from mains by a transformer, should be used.

(d) All fixtures used for holding pcb's and MOS components should be made of conductive material and be bonded to the bench top.

Storage of printed circuit boards

13. Storage of a pcb should be in reasonably cool and dry conditions, in an atmosphere free from corrosive fumes. The pcb should be wrapped or enclosed in a box to exclude dust (any purpose built packaging should be preserved for this purpose). The storage life of a pcb is indefinite providing these conditions are maintained.

TESTING AFTER REPAIR

General

14. Any item to be returned to the second line facility as a serviceable spare, or to be fitted to its parent assembly at third line, must satisfy all the tests in the relevant sections of Parts 2 and 4 of this manual.

THIRD LINE SERVICING

OF

PRC420 HF TRANSCEIVER

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ILLUSTRATIONS

Fig.
1 Controls and miscellaneous terminals : wiring

TECHNICAL DESCRIPTION

General

1. The PRC420 Transceiver is of modular construction as described in Parts 1 and 2 of this manual. Modules 2 to 13 are described in Sections 3 to 14 of this part of the manual.

2. Module 1 of the transceiver comprises the cast aluminium case which forms the chassis of the radio, and the desiccator, back-up cell, controls and connectors, mounted thereon.

3. Interconnection between the modules is either directly, using board mounted pins and sockets; by plug and/or socket ended ribbon cable or wiring harness; and by RF cable assemblies. A detailed list of the point-to-point wiring is given in Table 1, and wiring details of the plugs, sockets, and controls mounted on the case (Module 1) are given in Figure 1.

4. The central web of the case provides screening between the top and bottom compartments of the radio, and, additional screening between modules in the same compartment is provided by partitions secured to the casting.

TESTING

5. Testing of the complete radio at 3rd line should be in accordance with the procedures detailed in Part 2, Section 3 of this manual.

COMPONENTS LIST

6. The principal component parts of Module 1 of the radio which may be required at third line, and are not listed elsewhere in the manual are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
IC1	Voltage regulator	National LM317T	415/4/03073
S1	Rotary switch (RF)		408/9/51567
S2	Rotary switch (POWER)		408/9/54008
S3	Rotary switch (MODE)		408/9/51532/002
S4	Rotary switch (REMOTE)		408/9/51532/001
S5	Rotary switch (DISPLAY)		408/9/51559
S6	10-position BCD switch (CHANNEL)		408/9/51520
PBS1,2	Pushbutton (COUNT UP/DOWN)		408/4/51526
R1	Variable resistor (VOLUME)		404/9/08070

Table 1 - Point-to-point wiring

From	To	Wire No.
MODULE 2 - Power Supply Unit		
PL1 = 1 x 4		
PL1 - 1	4 - SK1 - 1 (Eth.)	-
- 2	- 2 (6.2V)	-
- 3	- 3 (24V)	-
- 4	- 4 (10V)	-
PL2 = 2 x 4		
PL2 - 1	1TP3 (Batt. earth)	002
- 2	1TP3 (Vehicle earth)	001
- 3	KEY	-
- 4	1S2/W1	014
- 5	6 - PL1 - 1	003
- 6	1TP4 (Batt. +ve)	004
- 7	11 - PL2 - 4	026
- 8	1S2/6 (Power)	005
PL3 = 2 x 13		
PL3 - 1	3 - PL2 - 7 (earth)	012
- 2	5 - PL1 - 14	016
- 3	KEY	-
- 4	3 - PL2 - 10	007
- 5	3 - PL2 - 9	008
- 6	5 - PL6 - 11	015
- 7	9 - PL10 - 8	018
- 8	10 - PL8 - 3	023
- 9	3 - PL2 - 2	011
- 10	9 - PL5 - 2	020
- 11	5 - PL6 - 8	013
- 12	9 - PL10 - 6	021
- 13	10 - PL8 - 1	024
- 14	11 - PL1 - 1	028
- 15	3 - PL1 - 16	006
- 16	9 - PL10 - 1	017
- 17	3 - PL2 - 3	010
- 18	12 - PL1 - 3	030
- 19	10 - PL8 - 2	022
- 20	9 - PL10 - 7	019
- 21	3 - PL2 - 1	009
- 22	11 - PL1 - 2	027
- 23	12 - PL1 - 1	031
- 24	11 - PL2 - 2	025
- 25	12 - PL1 - 5	029
- 26	12 - PL1 - 7	032

From	To	Wire No.
MODULE 3 - AF/AM/SSB		
PL1 = 2 x 13		
PL1 - 1	KEY	-
- 2	N/C	-
- 3	1VR/A (Volume - top)	052
- 4	9 - PL1 - 1	050
- 5	1VR/C (Volume - wiper)	049
- 6	9 - PL2 - 5	053
- 7	9 - PL1 - 20	034
- 8	9 - PL10 - 9	035
- 9	13 - PL1 - 1	041
- 10	13 - PL1 - 2	040
- 11	4 - PL1 - 6	045
- 12	9 - PL2 - 8	Scr.
- 13	9 - PL2 - 7	Scr.
- 14	9 - PL1 - 11	051
- 15	9 - PL1 - 6	036
- 16	2 - PL3 - 15	006
- 17	9 - PL10 - 2	033
- 18	9 - PL1 - 19	037
- 19	1S4/7 (Remote)	038
- 20	Wire 92 & 119	039
- 21	1VR/B (Volume - return)	048
- 22	6 - PL1 - 8	042
- 23	6 - PL1 - 20	043
- 24	4 - PL1 - 8	044
- 25	9 - PL2 - 4	047
- 26	9 - PL2 - 3	046
PL2 = 2 x 7		
PL2 - 1	2 - PL3 - 21	009
- 2	2 - PL3 - 9	011
- 3	2 - PL3 - 17	010
- 4	13 - PL1 - 5	058
- 5	6 - PL1 - 13	055
- 6	4 - PL1 - 9	057
- 7	2 - PL3 - 1	012
- 8	KEY	-
- 9	2 - PL3 - 5	008
- 10	2 - PL3 - 4	007
- 11	13 - PL1 - 8	059
- 12	6 - PL1 - 5	054
- 13	4 - PL1 - 7	056
- 14	N/C	-

continued ...

Table 1 continued ...

From	To	Wire No.
SK1-SK15	Module 7 PL1-PL15	
MODULE 4 - Remote control		
PL1 = 2 x 5		
PL1 - 1	1TP9 (Line -ve)	062
- 2	KEY	-
- 3	1S4/4 (Remote)	060
- 4	9 - PL1 - 9	063
- 5	6 - PL1 - 6	064
- 6	3 - PL1 - 11	045
- 7	3 - PL2 - 13	056
- 8	3 - PL1 - 24	044
- 9	3 - PL2 - 6	057
- 10	1TP8 (Line +ve)	061
SK1/1-4	2/PL1/1 - 2/PL1/4	-
MODULE 5 - Microprocessor		
PL1 - 20 pins		
PL1 - 1	1S5/2 (Digit select) 10M	076
- 2	KEY	-
- 3	1S6/8 (Channel select) MSB	068
- 4	1S5/6 (Dig.sel.) 1 kHz	072
- 5	13 - PL1 - 3	081
- 6	1S5/8 (Dig.sel.) Dim	078
- 7	6 - PL1 - 3	083
- 8	1S6/4 (Chan.sel.)	067
- 9	1S6/1 (Chan.sel.)	065
- 10	1S1/3 RF switch	093
- 11	1S5/1 (Dig.sel.) Normal	077
- 12	1S3/W1 (Mode switch)	069
- 13	1S3/W2	070
- 14	2 - PL3 - 2	016
- 15	1S5/7 (Dig.sel.) 100 Hz	071
- 16	1S1/1 RF switch	086
- 17	6 - PL1 - 19	085
- 18	6 - PL1 - 22	084
- 19	6 - PL1 - 21	082
- 20	1S6/2 (Chan.sel.)	066

From	To	Wire No.
SK2 = 14-way - Ribbon		
PL2 - 1	9 - PL4 - 6	-
- 2	9 - PL4 - 7	-
- 3	9 - PL4 - 8	-
- 4	9 - PL4 - 9	-
- 5	N/C	-
- 6	N/C	-
- 7	N/C	-
- 8	N/C	-
- 9	N/C	-
- 10	9 - PL4 - 5	-
- 11	9 - PL4 - 4	-
- 12	N/C	-
- 13	9 - PL4 - 2	-
- 14	9 - PL4 - 1	-
SK3 - 14-way		
PL3 - 1	8 - PL1 - 7	-
- 2	8 - PL1 - 6	-
- 3	8 - PL1 - 5	-
- 4	8 - PL1 - 4	-
- 5	8 - PL1 - 3	-
- 6	8 - PL1 - 2	-
- 7	8 - PL1 - 1	-
- 8	8 - PL1 - 14	-
- 9	8 - PL1 - 13	-
- 10	8 - PL1 - 12	-
- 11	8 - PL1 - 11	-
- 12	8 - PL1 - 10	-
- 14	8 - PL1 - 8	-
PL4 - 14-way		
PL4 - 1	-	-
- 2	-	-
- 3	10 - PL3 - 6	-
- 4	10 - PL3 - 7	-
- 5	10 - PL3 - 8	-
- 6	10 - PL3 - 9	-
- 7	10 - PL3 - 10	-
- 8	10 - PL3 - 5	-
- 9	10 - PL3 - 4	-
- 10	10 - PL3 - 3	-
- 11	10 - PL3 - 2	-
- 12	-	-
- 13	-	-
- 14	-	-

continued ...

Table 1 continued ...

From	To	Wire No.
SK5/1 to 40	Module 12 - PL6/1 to 40	
PL6 = 18 pins		
PL6 - 1	9 - PL2 - 2	087
- 2	9 - PL2 - 6	Scr.
- 3	WIRES 39 & 119	092
- 4	1TP10	145
- 5	9 - PL10 - 3	095
- 6	KEY	-
- 7	1S2b (Power)	139
- 8	2 - PL3 - 11	013
- 9	1S7/3 (Increment)	079
- 10	1TP5 (Memory Batt.)	088
- 11	2 - PL3 - 6	015
- 12	9 - PL1 - 17	091
- 13	12 - PL1 - 2	090
- 14	12 - PL1 - 4	089
- 15	1S8/3 (Decrement)	080
- 16	1S5/3 (Dig.sel.) 1M	075
- 17	1S5/4 100k	074
- 18	1S5/5 10k	073
MODULE 6 - Filter board - rear		
PL1 = 24 pins		
PL1 - 1	2 - PL2 - 5	003
- 2	9 - PL1 - 15	097
- 3	5 - PL1 - 7	083
- 4	9 - PL1 - 3	096
- 5	3 - PL2 - 12	054
- 6	4 - PL1 - 5	064
- 7	9 - PL10 - 5	105
- 8	3 - PL1 - 22	042
- 9	1IC1 pin 2 (V out)	099
- 10	9 - PL1 - 4	104
- 11	9 - PL1 - 14	100
- 12	WIRE 143	142
- 13	3 - PL2 - 5	055
- 14	1TP3 (Earth)	103
- 15	KEY	-
- 16	9 - PL10 - 11	101
- 17	9 - PL10 - 10	098
- 18	13 - PL1 - 7	136
- 19	5 - PL1 - 17	085
- 20	3 - PL1 - 23	043
- 21	5 - PL1 - 19	082
PL1 - 22	5 - PL1 - 18	084
- 23	9 - PL10 - 12	102
- 24	WIRE 142	143
SK1 (ATU)		
SK1 - A	READY I/P	-
- B	FAULT I/P	-
- C	24V UNREG O/P	-
- D	ATU PRESENT I/P	-
- E	EARTH	-
- F	Tx/Rx IND. O/P	-
- G	RESET O/P	-
SK5 (ANCILL.)		
SK5 - A	MIC. A	-
- B	MIC. B	-
- C	+24V	-
- D	AF O/P	-
- E	EARTH	-
- F	PRESSEL	-
- G	BCD CH. (MSB)	-
- H	BCD CH.	-
- J	BCD CH.	-
- K	BCD CH. (LSB)	-
PL4 (POWER)		
PL4 - A	SYSTEM ON/OFF	-
- B	RELAY DRIVE O/P	-
- C	VEHICLE SUPPLY I/P	-
- D	PA PRESENT I/P	-
- E	EARTH	-
- F	EARTH	-
- G	VEHICLE SUPPLY I/P	-
MODULE 7 - IF		
PL1 = 8 pins		
PL1 - 1	11 - PL1 - 6	110
- 2	10 - PL8 - 5	Scr.
- 3	KEY	-
- 4	9 - PL5 - 6	108
- 5	11 - PL1 - 3	Scr.
- 6	10 - PL8 - 4	109
- 7	9 - PL1 - 5	106
- 8	9 - PL5 - 3	Scr.

continued ...

Table 1 continued ...

From	To	Wire No.
PL2 = 4 pins		
PL2 - 1	Earth	-
- 2	KEY	-
- 3	9 - PL3 - 4	107
- 4	9 - PL3 - 1	Scr.
Pins 1-15 Module 3/SK1-15		
MODULE 8 - Display		
PL1 = 14 pins - Ribbon		
PL1 - 1	5 - SK3 - 8	-
- 2	5 - SK3 - 9	-
- 3	5 - SK3 - 10	-
- 4	5 - SK3 - 11	-
- 5	5 - SK3 - 12	-
- 6	5 - SK3 - 13	-
- 7	5 - SK3 - 14	-
- 8	5 - SK3 - 1	-
- 9	5 - SK3 - 2	-
- 10	5 - SK3 - 3	-
- 11	5 - SK3 - 4	-
- 12	5 - SK3 - 5	-
- 13	5 - SK3 - 6	-
- 14	5 - SK3 - 7	-
PL3 = 4 pins		
PL3 - 1	N/C	-
- 2	11C1/1 Volt.Reg. (Adj.)	112
- 3	11C1/2 Volt.Reg. (V out)	113
- 4	KEY	-
MODULE 9 - Synthesiser		
PL1 = 22 pins		
PL1 - 1	3 - PL1 - 4	050
- 2	KEY	-
- 3	6 - PL1 - 4	096
- 4	6 - PL1 - 10	104
- 5	7 - PL1 - 7	106
- 6	3 - PL1 - 15	036
- 7	1S2/3 (Power)	118
- 8	1S4/7 (Remote)	116

From	To	Wire No.
PL1 - 9	4 - PL1 - 4	063
- 10	WIRES 39 & 92	119
- 11	3 - PL1 - 14	051
- 12	13 - PL1 - 6	115
- 13	9-PL3-2	147
- 14	6 - PL1 - 11	100
- 15	6 - PL1 - 2	097
- 16	11 - PL2 - 3	120
- 17	5 - PL6 - 12	091
- 18	11 - PL1 - 4	121
- 19	3 - PL1 - 18	037
- 20	3 - PL1 - 7	034
- 21	9 - PL3 - 3	114
- 22	1S4/8 (Remote)	117
PL2 = 8 pins		
PL2 - 1	KEY	-
- 2	5 - PL6 - 1	087
- 3	3 - PL1 - 26	046
- 4	3 - PL1 - 25	047
- 5	3 - PL1 - 6	053
- 6	5 - PL6 - 2	Scr.
- 7	3 - PL1 - 13	Scr.
- 8	3 - PL1 - 12	Scr.
PL3 = 8 pins		
PL3 - 1	7 - PL2 - 4	Scr.
- 2	(9) - PL1 - 13	147
- 3	(9) - 1- 21	114
- 4	7 - PL2 - 3	107
- 5	11 - PL2 - 5	122
- 6		-
- 7		-
- 8	KEY	-
PL4 = 10 pins - Ribbon		
PL4 - 1	5 - SK2 - 14	-
- 2	5 - SK2 - 13	-
- 3	N/C	-
- 4	5 - SK2 - 11	-
- 5	5 - SK2 - 10	-
- 6	5 - SK2 - 1	-
- 7	5 - SK2 - 2	-
- 8	5 - SK2 - 3	-
- 9	5 - SK2 - 4	-
- 10	N/C	-

continued ...

Table 1 continued ...

From	To	Wire No.
PL5 = 6 pins		
PL5 - 1	10 - PL7 - 2	Scr.
- 2	2 - PL3 - 10	020
- 3	7 - PL1 - 8	Scr.
- 4	10 - PL7 - 1	123
- 5	KEY	-
- 6	7 - PL1 - 4	108
PL6/1-12	(9) upper SK8/1-12	-
PL7/1-5	(9) upper SK9/1-5	-
PL10 = 12 pins		
PL10- 1	2 - PL3 - 16	017
- 2	3 - PL1 - 17	033
- 3	5 - PL6 - 5	095
- 4	KEY	-
- 5	6 - PL1 - 7	105
- 6	2 - PL3 - 12	021
- 7	2 - PL3 - 20	019
- 8	2 - PL3 - 7	018
- 9	3 - PL1 - 8	035
- 10	6 - PL1 - 17	098
- 11	6 - PL1 - 16	101
- 12	6 - PL1 - 23	102
MODULE 10 - Band-pass filters		
SK1	12 - PL3	CO-AX
SK2/1-6	10(lower) - PL9/1-6	-
PL3 = 10 pins - Ribbon		
PL3 - 1	N/C	-
- 2	5 - PL4 - 11	-
- 3	5 - PL4 - 10	-
- 4	5 - PL4 - 9	-
- 5	5 - PL4 - 8	-
- 6	5 - PL4 - 3	-
- 7	5 - PL4 - 4	-
- 8	5 - PL4 - 5	-
- 9	5 - PL4 - 6	-
- 10	5 - PL4 - 7	-
SK4/1-6	10(lower) - PL6/1-6	-

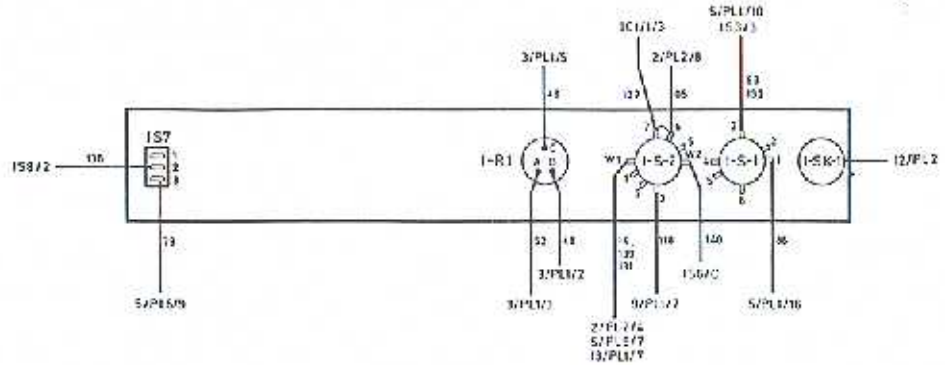
From	To	Wire No.
PL7 = 6 pins		
PL7 - 1	9 - PL5 - 4	123
- 2	9 - PL5 - 1	Scr.
- 3	11 - PL4 - 2	Scr.
- 4	KEY	-
- 5	SPARE	-
- 6	11 - PL4 - 4	124
PL8 = 6 pins		
PL8 - 1	2 - PL3 - 13	024
- 2	2 - PL3 - 19	022
- 3	2 - PL3 - 8	023
- 4	7 - PL1 - 6	109
- 5	7 - PL1 - 2	Scr.
- 6	KEY	-
MODULE 11 - Power amplifier		
PL1 = 6 pins		
PL1 - 1	2 - PL3 - 14	028
- 2	2 - PL3 - 22	027
- 3	7 - PL1 - 5	Scr.
- 4	9 - PL1 - 18	121
- 5	KEY	-
- 6	7 - PL1 - 1	110
PL2 = 8 pins		
PL2 - 1	KEY	-
- 2	2 - PL3 - 24	025
- 3	9 - PL1 - 16	120
- 4	2 - PL2 - 7	026
- 5	9 - PL3 - 5	122
- 6	12 - PL1 - 10	128
- 7	12 - PL1 - 9	127
- 8	12 - PL8 - 2	126
PL3 (CO-AX) FLYING LEAD from MODULE 10		
PL4 = 3 pins		
PL4 - 1	KEY	-
- 2	10 - PL7 - 3	Scr.
- 3	10 - PL7 - 6	124

continued ...

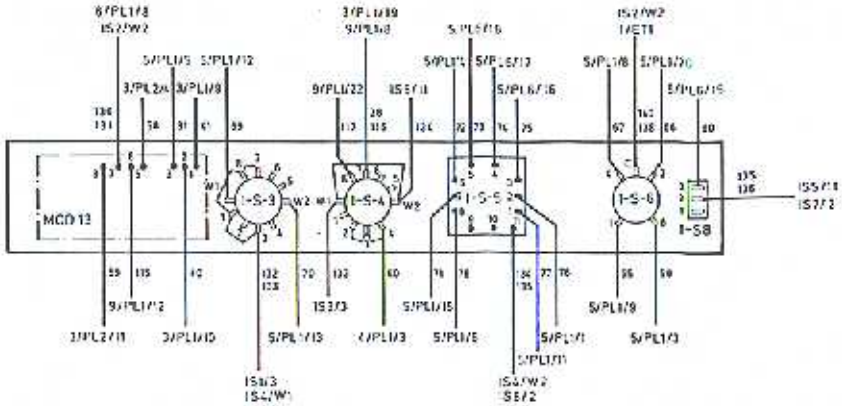
Table 1 continued ...

From	To	Wire No.
MODULE 12 - ATU		
PL1 = 2 x 5		
PL1 - 1	2 - PL3 - 23	031
- 2	5 - PL6 - 13	090
- 3	2 - PL3 - 18	030
- 4	5 - PL6 - 14	089
- 5	2 - PL3 - 25	029
- 6	KEY	-
- 7	2 - PL3 - 26	032
- 8	N/C	-
- 9	11 - PL2 - 7	127
- 10	11 - PL2 - 6	128
PL2	50 ohm socket (RF)	CO-AX
PL3	10 - SK1	CO-AX
PL6/1-40	5 - SK5/1-40	-
PL7/1-7	(12) - SK10/1-6	-
PL8/1	1 TP10	111
PL8/2	11 - PL2 - 8	126
PL9	TP7 (whip antenna SK)	

From	To	Wire No.
MODULE 13 - Filter board - front		
PL1 = 8 pins		
PL1 - 1	3 - PL1 - 9	041
- 2	3 - PL1 - 10	040
- 3	5 - PL1 - 5	081
- 4	KEY	-
- 5	3 - PL2 - 4	058
- 6	9 - PL1 - 12	115
- 7	1S2/W1	131
- 8	3- PL2 - 11	059
SK2 (SECURE)		
SK2 - A	MIC. A	-
- B	MIC. B	-
- C	24V O/P	-
- D	HEADPHONE	-
- E	EARTH	-
- F	PRESSEL	-
- G	HEADPHONE	-
SK3 (AUDIO)		
SK3 - A	MIC. A	-
- B	MIC. B	-
- C	WRITE I/P	-
- D	HEADPHONE	-
- E	EARTH	-
- F	PRESSEL	-
- G	HEADPHONE	-

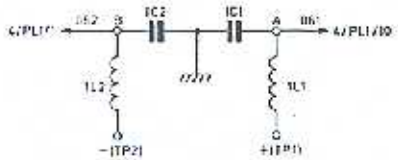


VIEW INSIDE FRONT PANEL - UPPER COMPARTMENT

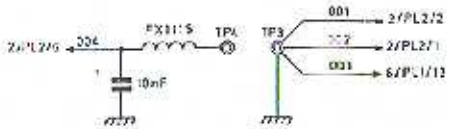


VIEW INSIDE FRONT PANEL - LOWER COMPARTMENT

MEMORY BATTERY (IPS)



REMOTE TERMINALS



BATTERY TERMINALS

NOTE

(1) PREFIX TO PLUG AND PIN NUMBER INDICATES MODULE NUMBER
e.g. S/PL1/6 = MODULE S/PLUG 1/PIN 6

(2) WHERE TERMINALS WITH MORE THAN ONE LE... WIRE DESTINATIONS ARE SHOWN IN THE... SAME SEQUENCE AS THE WIRE IDENT... e.g. IN IS1/1, WIRE 93 GOES TO S/PL1/90, WIRE 132 TO IS3/3

Fig 1 Controls and miscellaneous terminals – wiring

COMPONENTS LIST

13. The principal component parts of the power supply board 419/1/51162 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C1	330nF 5% 100V	Siemens B32560-D1334J	435/4/90317/018
C2	470nF 5% 100V	Siemens B32560-D1474J	435/4/90317/019
C3	22uF 20% 35V	BS9073 F002 or F005	402/4/55748/015
C4,11	82pF 2% 100V	Mullard 632-34829	400/4/20674/021
C5,12	68nF 5% 100V	Siemens B32560-D1683J	435/4/90317/012
C6	100pF 2% 100V	Mullard 632-34101	400/4/20674/022
C7	2.2nF 10% 100V	Wima FKS2	435/4/90821/012
C8	68uF 20% 3V	ITT TAP Type 68/3	402/4/57081/006
C9	150uF 10% 16V	BS9073 N001 CIHBAD	402/4/55733/150
C10	4.7uF 20% 16V	BS9073 F002 or F005	402/4/55746/011
C13	220uF 10% 10V	BS9073 N001 CIHBAD	402/4/56303/220
C14	100nF 5% 100V	Siemens B32560-D1104J	435/4/90317/014
	RESISTORS		
R1	0.10 ohms 10% 2.5W	Wirewound	403/4/07306/010
R2	47 ohms 2% 0.25W	Fixed film metal oxide	403/4/05521/470
R3	56k 2% 0.25W	Fixed film metal oxide	403/4/05524/560
R4,8	5.6k 2% 0.25W	Fixed film metal oxide	403/4/05523/560
R5	2.7k 2% 0.25W	Fixed film metal oxide	403/4/05523/270
R6	15k 2% 0.25W	Fixed film metal oxide	403/4/05524/150
R7	56 ohms 2% 0.25W	Fixed film metal oxide	403/4/05521/560
R9	220 ohms 2% 0.25W	Fixed film metal oxide	403/4/05522/220
R10	0.82 ohm 5% 0.5W	Fixed film metal oxide	403/4/07197/016
R11	16k 2% 0.25W	Fixed film metal oxide	403/4/05524/160
R12,22, 31	Variable 1k 10% 0.5W	Single turn type 3329H/ 81E	
R13	2.7k 2% 0.25W	Fixed film metal oxide	403/4/05523/270
R14,17	20k 2% 0.25W	Fixed film metal oxide	403/4/05524/200
R15	150k 2% 0.25W	Fixed film metal oxide	403/4/05525/150
R16	62k 2% 0.25W	Fixed film metal oxide	403/4/05524/620
R18	2k 2% 0.25W	Fixed film metal oxide	403/4/05523/200
R19,25	47k 2% 0.25W	Fixed film metal oxide	403/4/05524/470
R20	75 ohms 2% 0.25W	Fixed film metal oxide	403/4/05521/750
R21,34	6.2k 2% 0.25W	Fixed film metal oxide	403/4/05523/620
R23	2k 2% 0.25W	Fixed film metal oxide	403/4/05523/200
R24	220 ohms 2% 0.25W	Fixed film metal oxide	403/4/05522/220
R27	220k 2% 0.25W	Fixed film metal oxide	403/4/05525/220
R28	4.7k 2% 0.25W	Fixed film metal oxide	403/4/05523/470
R29	10k 2% 0.25W	Fixed film metal oxide	403/4/05524/100
R30	22k 2% 0.25W	Fixed film metal oxide	403/4/05524/220
R32,35	1k 2% 0.25W	Fixed film metal oxide	403/4/05523/100
R33	6.8k 2% 0.25W	Fixed film metal oxide	403/4/05523/680

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	DIODES		
D1	Reference 91V 5% 5W	Motorola 1N5377B	415/4/05755/091
D2	Regulator 36V 5% 1.3W	Mullard BZV85 C36	415/4/05839/021
D3	Regulator 4.7V 5% 0.4W	EG BZX79-C4V7	415/4/05830/008
D4,10	Switching 75V 750 mA	1N4148	415/4/98869
D5	Regulator 8.2V 5% 0.4W	EG BZX79-C8V2	415/4/05830/014
D6,7	Schottky 30V	Motorola 1N5818	415/4/05791
D8	Regulator 12V 5% 0.4W	EG BZX79-C12	415/4/05830/018
	TRANSISTORS		
TR1,4	P-N-P	Mullard BCY70	417/4/98267/001
TR2,8	N-P-N	BC107	417/4/02028/001
TR3	N-P-N	Texas BFR86	417/4/02132/001
TR5	P-N-P	Texas TIP30C	417/4/01872/004
TR6	N-P-N	Texas TIP35C	417/4/02153/009
TR7, 9-11	P-N-P	Motorola BD510-1	417/4/02129
	INTEGRATED CIRCUITS		
ML1,2	Positive voltage regulator	RCA CA3085AE	445/4/10529/008
ML3*	CMOS Hex Inverter	National CD4069BCNA+	445/4/03234/069
ML4	Transistor Array	RCA CA3096EX	445/4/03276/001
	MISCELLANEOUS		
RLA	Relay 26.5V 600 ohms or, Relay 24V 1250 ohms**	HI-G 2HA-2A-126 Style 02-09-01-12 Type HF	507/9/05097/003 507/4/38441/007
L1	Inductor RF	Plessey	406/1/32281
L2	Inductor RF	Plessey	406/1/32283
L3	Inductor RF	Plessey	406/1/32282
L4	Inductor Fx 1115	Plessey	406/1/32155
FS1	Fuse 5A	Littlefuse 275-5A	518/4/90467/013
PL1	Plug 4-way	75160-109-4	508/9/24124/004

**Some early models only.

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. STATIC SENSITIVE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.

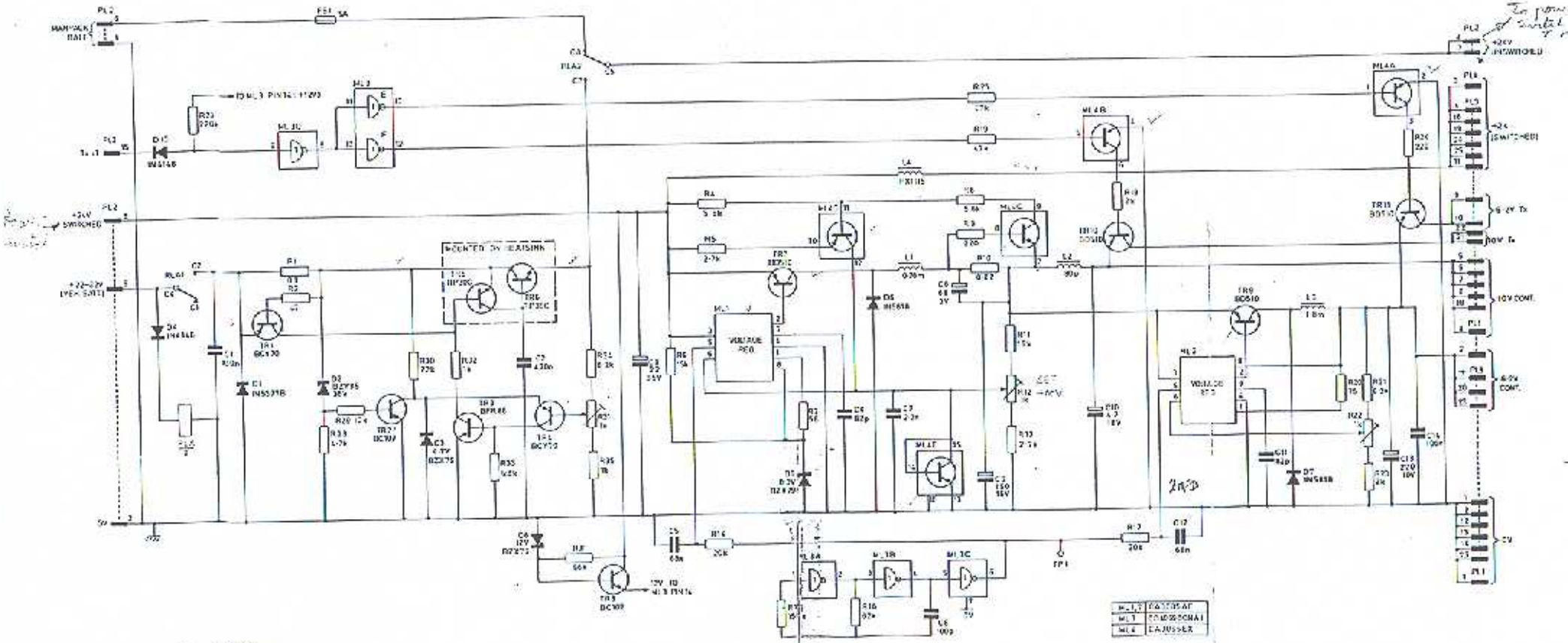


Fig 1 Power supply board : circuit diagram

Fig 1

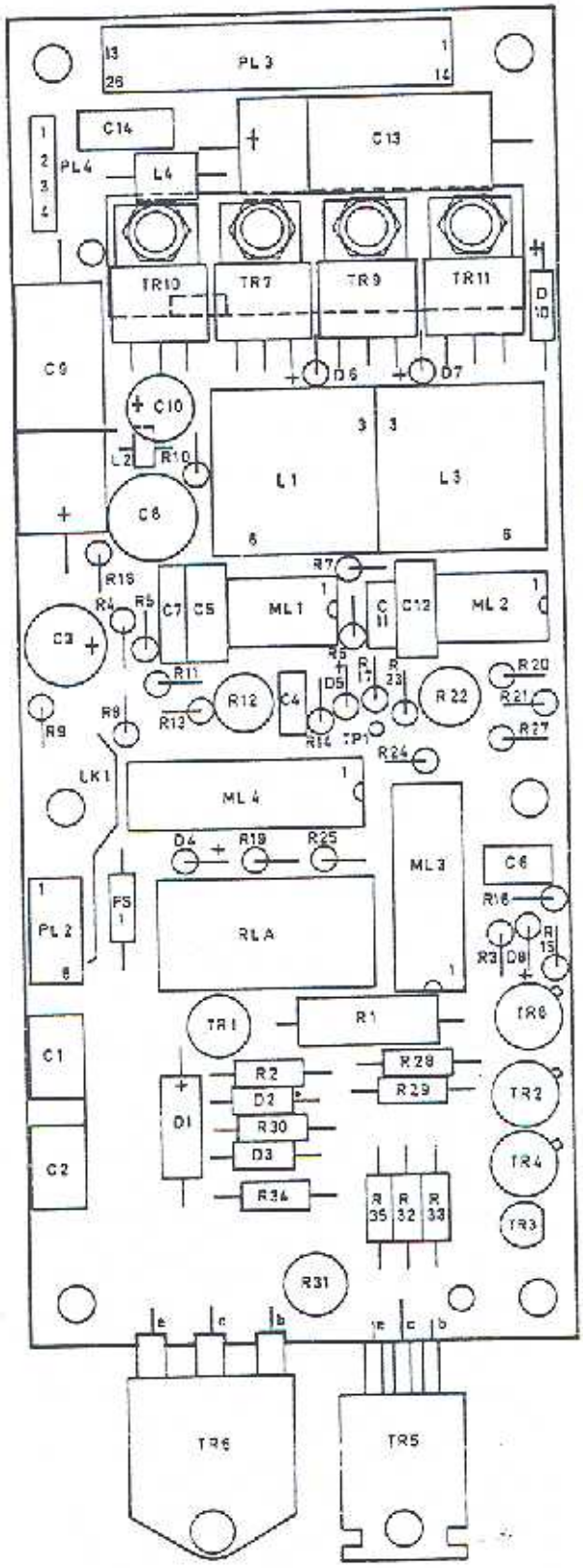


Fig 2 Power supply unit – component layout

THIRD LINE SERVICING

OF

AF/AM/SSB BOARD 419/1/51165

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ILLUSTRATIONS

Fig.
1 AF/AM/SSB board : circuit diagram
2 AF/AM/SSB board : component layout

TECHNICAL DESCRIPTION

General

1. This board provides the following circuits for the radio:

   (a) Voice operated gain adjusting device (VOGAD).

   (b) Modulator for AM and SSB transmission.

   (c) RF speech clipper.

   (d) AF stages and AF power amplifier.

2. The VOGAD circuit is switched off when the radio is in the receive mode or when transmitting CW, and is operational when in the transmit mode or when local and remote operators are intercommunicating (Intercom).

3. The modulator stage and the RF speech clipper are only used when the radio is transmitting signals and are disabled by the absence of +6V Tx on PL2/2 and +10V Tx on PL2/1 when the radio is in the receive mode. This conserves battery power.

Circuit description

4. A circuit diagram of the AF/AM/SSB board is given in Fig.1. The description which follows is divided into three parts covering board functions in the transmit, receive, and intercom modes respectively.

Transmit mode

5. Oral AF signals for transmission are received at board inputs PL1/9 and PL1/10, or PL1/11 and PL1/24, or from the remote channel select terminal, on PL1/22 and PL1/23 and presented to the balanced input of a voice operated gain adjusting device (VOGAD) ML1. The function of ML1 is to present a constant AF level into the following modulator stage irrespective of the amplitude of the input signal (ie. whisper or a shout). This provides constant modulation control to ensure the specified pep is achieved on SSB transmissions for AF inputs between 0.2 mV and 20 mV; and that a modulation depth greater than 70% is achieved on AM transmissions for AF inputs between 0.8 mV and 20 mV.

6. The main AF output from the VOGAD at ML1/9 is amplified by ML9B and routed to the modulator stage. During AM transmissions contact ML7A is not operated and the AF signal path is via R51, ML2B, and C32 to the AM modulator ML4 where the audio input is used to modulate the amplitude of a 1.4 MHz IF carrier frequency.

7. The 1.4 MHz is connected to the board at PL1/26 and then via ML5A and C34 to the AM modulator at ML4/8. The modulated 1.4 MHz output on ML4/6 is routed via amplifier ML5C, capacitor C13 and pot. R92, to leave the board at SK10. Potentiometer R108 provides an adjustment to set the depth of amplitude modulation at 75% $\pm$ 5%.

8. Single sideband working (SSB) is signalled by a logic 1 condition on PL1/8. This operates contact ML7A and connects the audio input signal to a second double balanced modulator ML3, in parallel with ML4. The filter networks preceding amplifiers ML2A and ML2B produce a 90° phase difference between the two audio inputs to the modulator. The 1.4 MHz carrier for ML3 is connected at PL1/25 and has a 90° phase difference with the other supply on PL1/26. The outputs of the two double balanced modulators are combined to produce a SSB output consisting of the upper sideband (USB) of the modulation product; both the lower sideband and the 1.4 MHz carrier are suppressed.

9. The potentiometers R105 and R106 are set to optimise carrier rejection to less than −51.5 dB with respect to the USB. Pot. R107 provides an adjustment to optimise LSB rejection. The SSB output is then routed via an RF speech clipping circuit ML5B to the board output at SK6. The clipper circuit provides 15 dB rf speech clipping for AF input levels greater than 0.8 mV.

10. On CW transmissions a logic 1 (Tx) on PL1/18 operates ML7C to connect a 1 kHz modulating signal on PL1/14 to the modulator stage which then operates as described for SSB working to produce a 1.4 MHz USB output at SK6.

11. Speech sidetone during transmission is provided on pin 4 of the VOGAD ML1. From there it is connected by contact ML6A to the AF amplifier stages; via C55, R18, and ML10A/2 to amplifiers serving the local operator; and via C54, R12, and ML9A/2 to the remote audio output on PL2/12 and 13. The AF stages are described in the receive mode part of this description.

12. Sidetone for CW transmissions (1 kHz) is provided at PL1/4 and routed to the AF stages.

13. When the radio is tuning the $\overline{\text{TUNE}}$ input on PL1/20 goes to 0V switching on TR3. The TR3 collector at +10V now overrides any AM selection signal incoming on PL1/8 and prepares the board circuits for the SSB/CW signal required for

the tune sequence and also ensure the correct logic signals for the tune sequence are applied to Module 7 via SK8.

14. Input pin PL1/4 which carries the 1 kHz (CW) sidetone during keying or tuning, is also used to feed warning tones into the AF stages serving the local and remote operators respectively.

Receive mode

15. When the radio is in the receive mode, audio signals recovered from the incoming RF carrier signal are connected to the Rx/AF input SK1 and via ML6C and ML6D to the input of the remote AF amplifier ML9A, and the first stage of the local AF power amplifier at ML10B/6. The remote AF output from ML9A is routed via C14 to output pins PL2/12 and 13.

16. The audio signal for the local operator from ML10B/7 is connected to an external volume control via output pin PL1/3 and back into the board at PL1/5. From here it is routed via the pre-amp ML10A to the base inputs of the push-pull power output transistors TR1 and TR2. The board AF power output on PL2/4 is not less than 840 millivolts into 75 ohms when the external volume control is set at maximum.

Intercom mode

17. Selection of the intercom mode is signalled by a logic 1 on PL1/19. This operates contact ML7B to route the audio output of amplifier ML9B, via C16 and R11, to the remote AF amplifier ML9A, and via C57 and R95, to the input stage of the local AF amplifier. When on intercom a logic 0 on PL1/17 releases ML6D to insert a 3.6k ohm resistor (R20) in series with the incoming signal path. This mutes signals from the receiver and reduces interference while the two operators are communicating.

Testing and alignment

18. Testing and alignment information for this board will be found in Part 4 of this volume.

COMPONENTS LIST

19. The principal component parts of the AF/AM/SSB board 419/1/51165 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C1,4,11, 16,17, 23,35, 36,45, 46,54, 55,56-58,61	100nF 5% 100V	Siemens B32560-D1104J	435/4/90317/014

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C2,3,12, 37-39, 52	22uF 10% 16V	CECC 30201-003/016PT E	402/4/56132/220
C5,6,13, 21,33, 34,40, 41,43, 44,51, 53	10nF 10% 63V	Wima type MK52 or Plessey type 1-68	435/4/90829/023
C7,59, 60	4.7uF 20% 10V	BS9073 F002 or F005	402/4/55745/011
C8	47uF 10% 20V	BS9073 N001 C1HBAC	402/4/56312/470
C9	4.7nF 10% 100V	Wima FKS2	435/4/90821/014
C10,19	2.2uF 20% 16V	BS9073 F002 or F005	402/4/55746/009
C14,31, 32	10uF 10% 20V	CECC 30201-003/016PT D	402/4/56272/100
C15,22	6.8nF 10% 100V	Wima type FK52 or Plessey type 1-68	435/4/90821/006
C18	22nF 5% 250V	Siemens B32560-D3223J	435/4/90317/009
C25,28	2820pF 1% 100V	BS9070 N002 C2AED	438/4/25911/282
C27,30	10nF 5% 100V	Wima FKS2	435/4/90873/007
	RESISTORS		
R1,2,25, 27,29	27 ohms 2% 0.25W	Metal oxide film	403/4/05521/270
R3,41	33k 2% 0.25W	Metal oxide film	403/4/05524/330
R4	1M 5% 0.25W	Mullard type VR25	403/4/07118/001
R5	56k 2% 0.25W	Metal oxide film	403/4/05524/560
R7,23, 24,26, 93,102	220k 2% 0.25W	Metal oxide film	403/4/05525/220
R8	680k 2% 0.25W	Metal oxide film	403/4/07149/680
R11,49	16k 2% 0.25W	Metal oxide film	403/4/05524/160
R12	27k 2% 0.25W	Metal oxide film	403/4/05524/270
R13	160k 2% 0.25W	Metal oxide film	403/4/05525/160
R14	390k 2% 0.25W	Metal oxide film	403/4/07149/390
R15	2.7k 2% 0.25W	Metal oxide film	403/4/05523/270
R16,59, 68,76	1k 2% 0.25W	Metal oxide film	403/4/05523/100
R17	82k 2% 0.25W	Metal oxide film	403/4/05524/820
R18	15k 2% 0.25W	Metal oxide film	403/4/05524/150
R19	120k 2% 0.25W	Metal oxide film	403/4/05525/120
R20	5.6k 2% 0.25W	Metal oxide film	403/4/05523/560
R21,37, 88,114	1.5k 2% 0.25W	Metal oxide film	403/4/05523/150
R22,28, 38,100, 111	100k 2% 0.25W	Metal oxide film	403/4/05524/100

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R30,62, 63,72, 73,80, 81,85, 86	3k 2% 0.25W	Metal oxide film	403/4/05521/300
R31	3.9k 2% 0.25W	Metal oxide film	403/4/05523/390
R32,84	300 ohms 2% 0.25W	Metal oxide film	403/4/05522/300
R33,35, 87	1.8k 2% 0.25W	Metal oxide film	403/4/05523/180
R36,60, 69	680k 2% 0.25W	Metal oxide film	403/4/05525/680
R39	180k 2% 0.25W	Metal oxide film	403/4/05525/180
R40,50	18k 2% 0.25W	Metal oxide film	403/4/05524/180
R42,43, 51,52, 101	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R44,46	51k 2% 0.25W	Metal oxide film	403/4/05524/510
R45,47	91k 2% 0.25W	Metal oxide film	403/4/05524/910
R48	4.7k 2% 0.25W	Metal oxide film	403/4/05523/470
R53,54	4.7 ohms 2% 0.25W	Metal oxide film	403/4/07148/470
R55,57, 64,65	2k 2% 0.25W	Metal oxide film	403/4/05523/200
R56,58, 66,67, 103,113	100 ohms 2% 0.25W	Metal oxide film	403/4/05522/100
R61,71	8.2k 2% 0.25W	Metal oxide film	403/4/05523/820
R77	6.2k 2% 0.25W	Metal oxide film	403/4/05523/630
R78,79	820 ohms 2% 0.25W	Metal oxide film	403/4/05522/820
R82,83	180 ohms 2% 0.25W	Metal oxide film	403/4/05222/180
R90,91	470k 2% 0.25W	Metal oxide film	403/4/07149/470
R92,115	5k 10% 0.5W	Variable - single turn	404/9/05032/005
R95	11k 2% 0.25W	Metal oxide film	403/4/05524/110
R97	330k 2% 0.25W	Metal oxide film	403/4/07149/330
R98,99	1.6k 2% 0.25W	Metal oxide film	403/4/05523/160
R104	200k 10% 0.5W	Variable - 3329E/62P	404/9/05052/014
R105, 106	47k 10% 0.25W	Variable - BS9131/N003	404/4/08062/009
R107	1k 10% 0.5W	Variable - 3329H/81E	404/9/05032/003
R108	500 ohms 10% 0.5W	Variable - single turn	404/9/05032/002
R112	51 ohms 2% 0.25W	Metal oxide film	403/4/05521/510
R110	75k 2% 0.25W	Metal oxide film	403/4/05524/750
	INTEGRATED CIRCUITS		
ML1	AF amp., VOGAD	Plessey SL622C	446/4/00483/003
ML2,9,10	Operational amp.	RCA CA1558E	445/4/10787/003
ML3,4	Double bal. modulator	Plessey SL1596	445/4/10789
ML5	N-P-N transistor array	RCA CA3086E	445/4/03193/007
ML6,7 *	Bi-lateral switch	National CD4066BCN	445/4/03234/066
ML8 *	Quad. NOR gates	National CD4001	445/4/03234/001

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	MISCELLANEOUS		
TR1,3	P-N-P transistor	BCY71	417/4/01721/002
TR2	N-P-N transistor	BC109C	417/4/02028/009
D2-4	Diode, H.S. switching	1N4148	415/4/98869
L4-7	Inductor, 47uH 10%	BS9751 N0001	406/4/32161/033
PL1 (Lower)	Plug, 13-way	Berg 75168-103-13	508/4/22211/013
PL1 (Upper)	Plug, 13-way	Berg 75168-102-13	508/4/22212/013
PL2 (Lower)	Plug, 7-way	Berg 75168-103-07	508/4/22211/007
PL2 (Upper)	Plug, 7-way	Berg 75168-102-7	508/4/22212/007
SK1-15	Socket, 1-way	Berg 75302-001	508/4/22131

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. STATIC SENSITIVE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.

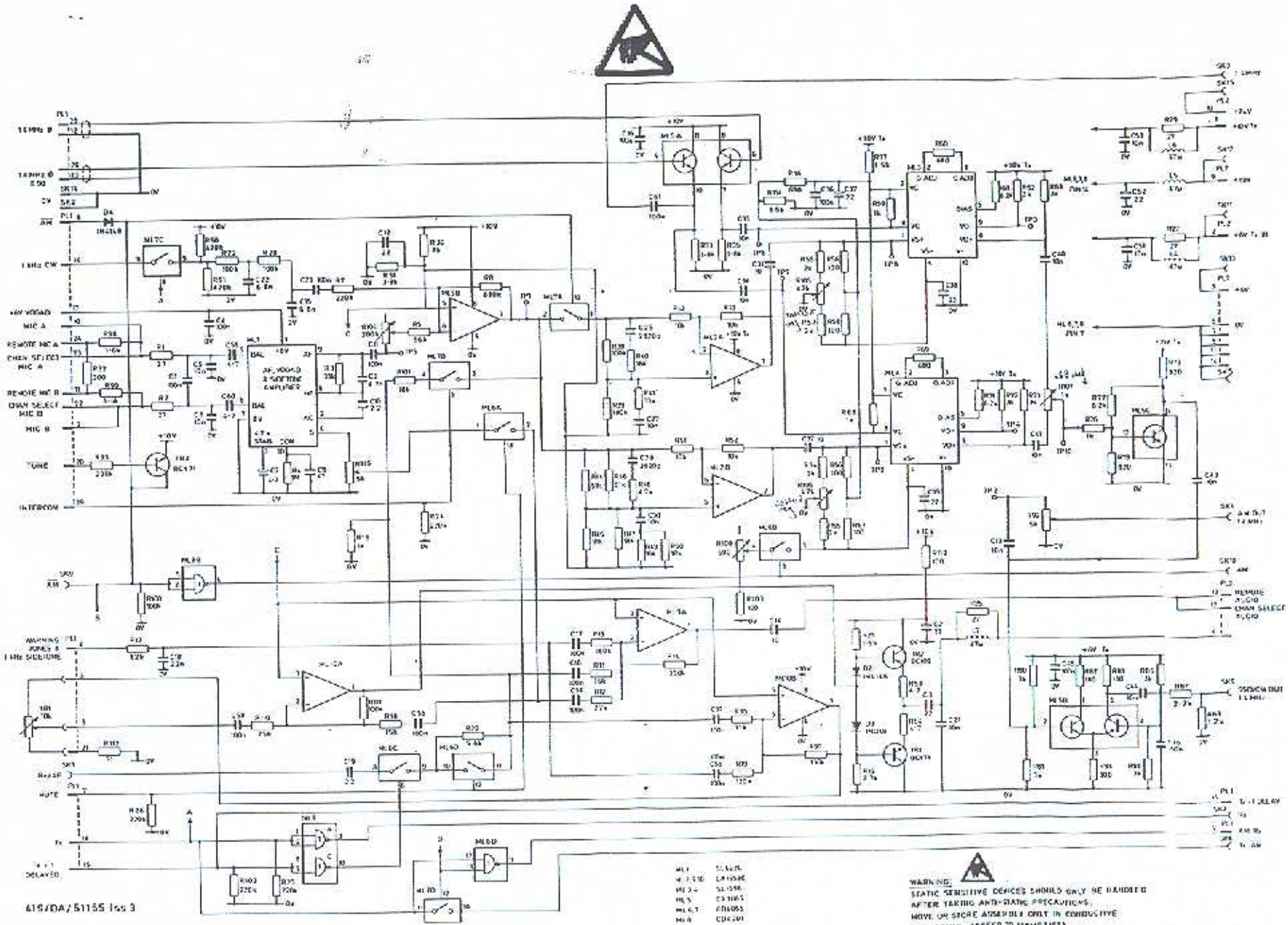

Fig 1 AF/AM/SSB board : circuit diagram

THIRD LINE SERVICING

OF

REMOTE CONTROL BOARD 419/1/51168

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ILLUSTRATIONS

Fig.

1 Remote control board : circuit diagram

2 Remote control board : component layout

TECHNICAL DESCRIPTION

General

1. The Remote Control Board contains a d.c. current sensor and an audio interface circuit to terminate a two-wire line. The logic state ('1' or '0') on the two outputs of the current sensor is controlled by the amount of line current drawn; this d.c. signalling path is unaffected by any audio frequency signals which may be present on the line.

Circuit description

2. A circuit diagram of the Remote Control Board is given in Fig.1.

3. Board terminals PL1/1 and PL1/10 connect the 2-wire line to one side of line transformer T1. The microphone and AF tone inputs to the board are connected to the other winding of the transformer via contacts of relay RLA.

4. Transistors TR2, TR3, and TR4 and their associated circuitry provide a +17.5V (± 0.5V) regulated supply for the current sensing function of ML1. To conserve battery power the regulator is only switched on when remote facilities are required; switch on is effected by the +10V REMOTE condition on PL1/3 which turns on transistors TR2, TR3 and TR4. When TR4 is conducting the +28V supply on SK1/3 is connected to drive the regulator. Potentiometer R5 provides an adjustment to set the regulator output voltage; diode D5 provides temperature compensation.

5. The 6V logic voltage for ML1 is supplied from SK1/2 via TR5 and TR6 which form an electrical switch; switch on is again effected by a +10V condition on PL1/3.

6. Signals from a remote operator are effected by changes in the terminating resistance at the remote end of the external line. The consequent changes in line current drawn are detected by ML1, and logic signals are generated in accordance with Table 1.

Table 1 - Signals derived from line current

Line Current (mA)	ML1 logic output		Board outputs		Relay RLA Tx/Rx
	A (Pin 1)	B (Pin 12)	+10V CALL PL1/4	0V PRESSEL PL1/5	
0- 4	0	0	0V	10V	Rx
8-14.5	1	0	0V	0V	Tx
20-34	0	1	+10V	10V	Rx

7. When the A output of ML1 goes to logic 1 (remote pressel operated), transistor TR7 is switched on, and relay RLA operates to connect the line transformer to the microphone connections at PL1/6 and PL1/8. Logic 1 on the A output of ML1 also turns on TR10; with TR10 conducting, 0V is connected to the 0V PRESSEL output at PL1/5.

8. When the B output of ML1 goes to logic 1 (CALL signal initiated), transistor TR8 is switched off removing the 1 kilohm path to ground via R20, thus producing a +10V CALL signal at PL1/4.

9. When the +10V REMOTE input (PL1/3) is switched externally to 0V (radio on local control) a remote operator can still initiate a CALL signal by putting a short circuit condition on the line terminals. This puts a ground condition via D3 (avalanched), D2, and R24 to switch on TR9. With TR9 conducting resistor R19 is short circuited, and the voltage on PL1/4 rises to +10 volts.

Testing and alignment

10. Testing and alignment information for this board will be found in Part 4 of this volume.

COMPONENTS LIST

11. The principal component parts of Remote Control Board 419/1/51168 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C1,2,10, 11	10nF 5% 63V	Wima type MKS2	435/4/90829/023
C3	33uF 20% 25V	BS9073 F002 or F005	402/4/55747/016
C4	10uF 20% 25V	BS9073 F002 or F005	402/4/55747/013

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C5	15uF 20% 10V	BS9073 F002 or F005	402/4/55745/014
C6	33uF 20% 10V	BS9073 F002 or F005	402/4/55745/016
C7	68nF 5% 63V	Wima type MKS2	435/4/90829/015
C8,9	10uF 20% 10V	BS9073 F002 or F005	402/4/55745/013
	RESISTORS		
R1,10, 12	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R2,3,17, 18	27 ohms 2% 0.25W	Metal oxide film	403/4/05521/270
R4,19	18k 2% 0.25W	Metal oxide film	403/4/05524/180
R5	2k 5% 0.5W	Variable - single turn	404/9/05032/004
R6,14	8.2k 2% 0.25W	Metal oxide film	403/4/05523/820
R7	8.2 ohms 2% 0.25W	Metal oxide film	403/4/05521/820
R8	124 ohms 2% 0.25W	Metal oxide film	403/4/05512/124
R9	510 ohms 1% 0.25W	Metal oxide film	403/4/05522/510
R11,23	470 ohms 2% 0.25W	Metal oxide film	403/4/05522/470
R13,20	1k 2% 0.25W	Metal oxide film	403/4/05523/100
R15,21	100k 2% 0.25W	Metal oxide film	403/4/05525/100
R16	1.5k 2% 0.25W	Metal oxide film	403/4/05523/150
R22	22k 2% 0.25W	Metal oxide film	403/4/05524/220
R24	1.2k 2% 0.25W	Metal oxide film	403/4/05523/120
R25	330 ohms 2% 0.25W	Metal oxide film	403/4/05522/330
	SEMICONDUCTORS		
D1,2, 5-7	Diode	1N4148	415/4/98869
D3	Zener diode 5.1V 5%	BZX79-C5V1	415/4/05830/009
D4	Zener diode 5.6V 5%	BZX79-C5V6	415/4/05830/010
TR1,4	P-N-P transistor	BFX38	417/4/02136
TR2,5,9	P-N-P transistor	BCY70	417/4/01721/001
TR3,6-8, 10	N-P-N transistor	BC107B	417/4/02028/004
ML1	Current sensor IC	SB174A	445/4/03425
	MISCELLANEOUS		
L1-4	Inductor 47uH ± 10%	BS9751 N0001	406/4/32161/033
RLA	Relay 600 ohms 26.5V or, Relay 1250 ohms 24V	HI-G 2HA-2A-126 BS9151 F007 02-09-01-12 type HF	507/9/05097/003 507/4/38441/007
T1	Transformer 1:1:1.125	Gardeners GR82212-631-0444	405/9/14360
SK1	Socket 1-way	Berg 75302-001	508/4/22131
PL1 (Upper)	Plug 19-way	Berg 75168-109-05	508/4/22212/005
PL1 (Lower)	Plug 5-way	Berg 75168-103-05	508/4/22211/005

*Some early models only.

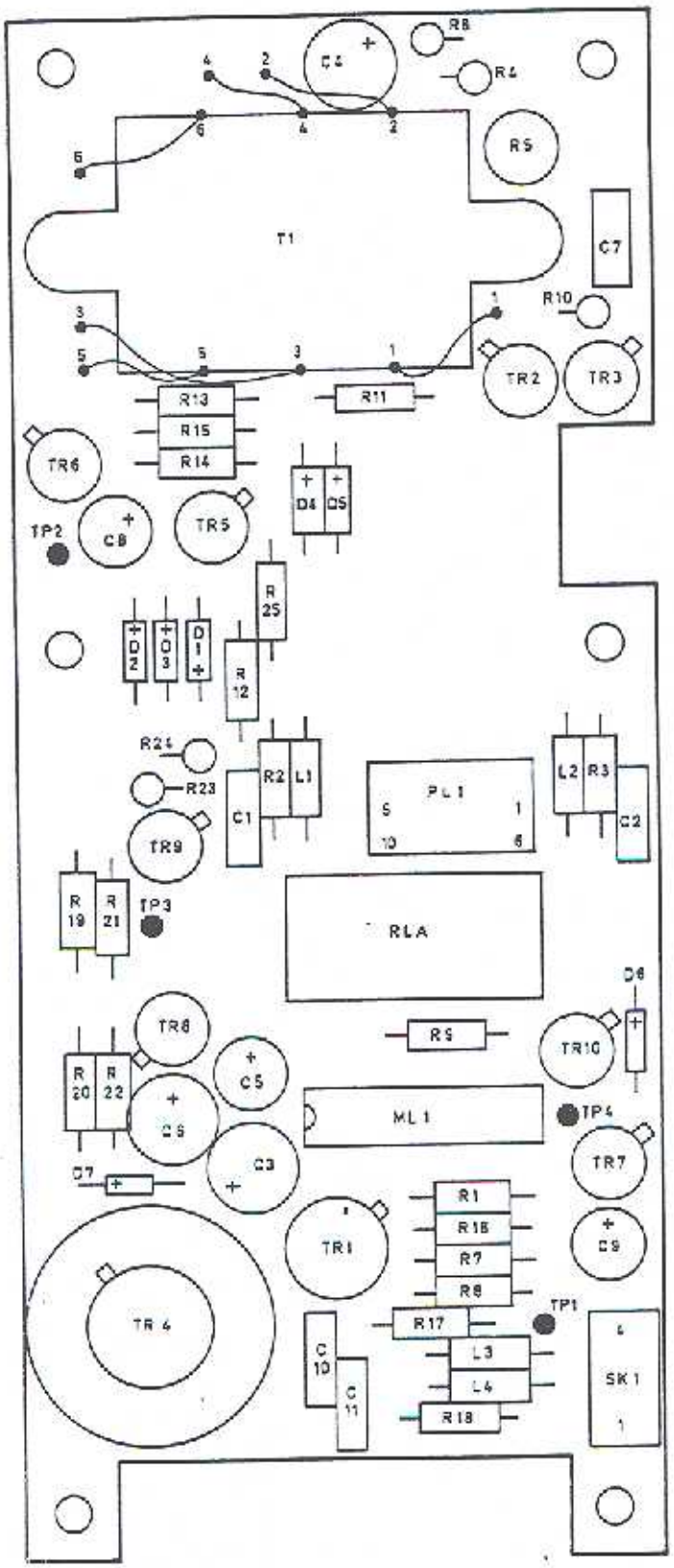

Fig 2 Remote control board – component layout

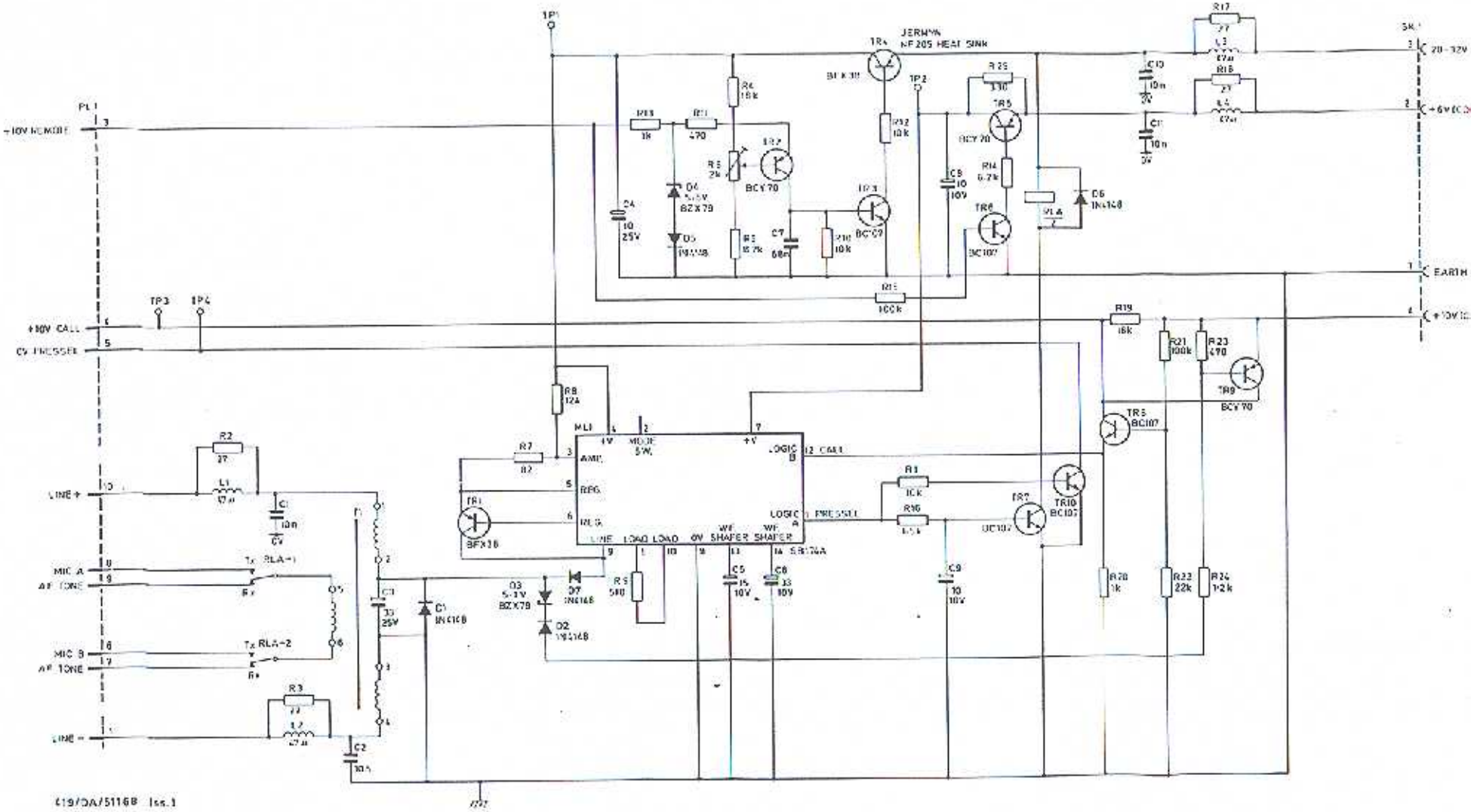

Fig.1 Remote control board : circuit diagram

THIRD LINE SERVICING

OF

MICROPROCESSOR BOARD 419/1/51171

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ILLUSTRATIONS

Fig.

1 Microprocessor timing waveforms
2 Input instruction timing
3 Output instruction timing
4 Microprocessor board: circuit diagram
5 Microprocessor board: component layout
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TECHNICAL DESCRIPTION

Introduction

1. The action of this circuit is not, as in non-microprocessor circuits, decided entirely by hardware configurations. In microprocessor (M/P) circuits it is largely decided by the program data set into the read-only-memory during manufacture. It should be realised therefore, that while a working knowledge of the circuit is useful, the ability of a maintainer to diagnose faults to component level is very limited. While peripheral faults can be dealt with in the usual manner, faults in the M/P controlled part of the circuit are another matter. To diagnose faults in this area it is necessary to employ a suitably programmed computer which can be plugged into the M/P IC socket on the

board which will enable it to communicate with the remainder of the circuit. For this reason the circuit description of the M/P controlled circuitry is limited to an outline of the operation. The remainder of the circuit is described in the usual manner.

General

2. The main function of the M/P Board is to exercise overall control of the Antenna Tuning Unit, Bandpass Filter, Synthesiser and Display modules of the radio.

3. The circuit employs a CMOS microprocessor with 128 x 8 bits of RAM and 2048 x 8 bits of ROM to monitor inputs from the front panel controls on the radio which are connected via its three CMOS input ports, and, after suitable decoding and driving where necessary, effect overall control functions through its three CMOS output ports.

4. Additional control lines provide feedback of information to the M/P Board from the ATU and Synthesiser modules.

5. Peripheral circuitry provides RAM protection during supply failure, clock control, and memory back-up cell trickle charging.

Circuit description

6. A circuit diagram of the Microprocessor Board is given in Figs.4a and 4b.

Microprocessor

7. The heart of the Microprocessor Board is the microprocessor integrated circuit ML4. A brief description of the functions of the various terminals of ML4 as used in this circuit is given in Table 1.

Microprocessor board timing

8. Timing on the Microprocessor Board is derived from the CLOCK INPUT on PL6/1. This is amplified by the TR4 circuit, and again by the high gain amplifier ML8C, before inversion and connection to one input of AND gate ML32C. When ML32C is enabled by a logic 1 condition on DISPLAY NORMAL (PL1/11) or DISPLAY DIM (PL1/6), or by logic 0 on the TUNE INPUT (PL6/3) or the software control line (2) from ML12/19, the clock supply is switched through to the microprocessor. In the absence of a demand for frequency display the input to AND gate ML40C is logic 1, and the clock gate (ML32C) is then controlled by a 'wake-up' circuit comprised of monostables ML41A and ML41B. The 'wake-up' circuit generates a negative going pulse about once every second, which switches on the clock supply to the M/P. In this way the M/P is activated to scan the control line conditions, and execute any instructions generated by the software program.

Table 1 - Microprocessor ML4: terminal functions

Title	Pin	Function
CLK	1	Input for externally generaced single phase clock. The 2.8 Mliz clock frequency is counted down internally to 8 pulses per machine cycle.
$\overline{CLR}$	3	When pin 3 is at '0' the device resets; when pin 3 is at '1' the device runs. When initiated from the reset operation the first machine cycle following $\overline{CLR}$ is always the initialisation cycle, which requires 9 clock pulses, followed by a 'fetch' from location 0000 in the memory.
BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7	15 14 13 12 11 10 9 8	8-bit bi-directional data bus lines used for transferring data between the memory, the microprocessor, and the input/output (I/O) devices.
N0 N1 N2	19 18 17	Used as device selection lines when an I/O instruction is being executed. Defines the input-output port in use.
$\overline{EF1}$ $\overline{EF2}$ $\overline{EF3}$ $\overline{EF4}$	24 23 22 21	These inputs are used as flags carrying status signals from the ATU (phase and conductance), and the Synthesiser (reset and tune).
TPA TPB	34 33	Positive timing pulses occurring once in each machine cycle (FETCH or EXECUTE). TPB follows TPA. Used to interpret codes, and to time inter-action with the data bus.
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7	25 26 27 28 29 30 31 32	8 memory address lines. MA0 to MA3 are utilised as 'chip select' lines to identify which ROM or RAM chip is required in the program. This occurs during the higher-order byte of the M/P 16-bit memory address. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA.
$\overline{MWR}$	35	A negative pulse appearing in a memory-write cycle after the address lines have stabilised.
$\overline{MRD}$	7	A low level on $\overline{MRD}$ indicates a memory read cycle. This output is used to control the three-state outputs from the addressed RAM, and as part of the chip select code to the ROM. It is also used to indicate the direction of data transfer during an I/O instruction to the input/output ports.

9. The clock supply to latch ML7B is used in conjunction with the TPA timing pulse from the M/P to produce a TPA DELAY pulse. The latter is only used during testing and is not part of the normal circuit operation.

Microprocessor (ML4) operation: timing relationships

10. Timing diagrams for the microprocessor are given n Figures 1 to 3. The timing waveforms given in Fig.1 illustrates general signal relationships only and does not represent any specific machine cycle. Figures 2 and 3 provide the timing relationships for input and output instructions respectively.

Input instruction timing (Fig.2)

11. An input instruction permits information from an external source (eg. front panel controls) to be written into RAM. The input instruction is fetched from the ROM during state S0 when ML4/7 asserts $\overline{\text{MRD}}$, and reads into its registers. The instruction is executed during the next machine cycle, state S1, which is a memory write cycle. An active low $\overline{\text{MWR}}$ pulse generated at ML4/35 during this cycle will strobe information on the data bus into the RAM. The high condition on $\overline{\text{MRD}}$ during the memory write cycle disables the ROM output during this period. The N bits (N0-N2) are used to define the source of the data input by selecting one of the three input port devices.

Output instruction timing (Fig.3)

12. An output instruction permits information stored in the memory to be read out to an external device. An output instruction is fetched from ROM during state S0 when ML4/7 asserts $\overline{\text{MRD}}$ and reads into its registers. The instruction is executed during the next machine cycle, state S1, which is now a memory read cycle. During the S1 cycle $\overline{\text{MRD}}$ is again asserted and enables output from the memory onto the bus. Data is valid after the access time has elapsed. The data is then strobed into an output port, and will always be valid when TPB, the N bits, and $\overline{\text{MRD}}$ signals are true. The N bits (N0-N2) are used to define the destination of the data output by selecting one of the three output port devices.

Memory power supply

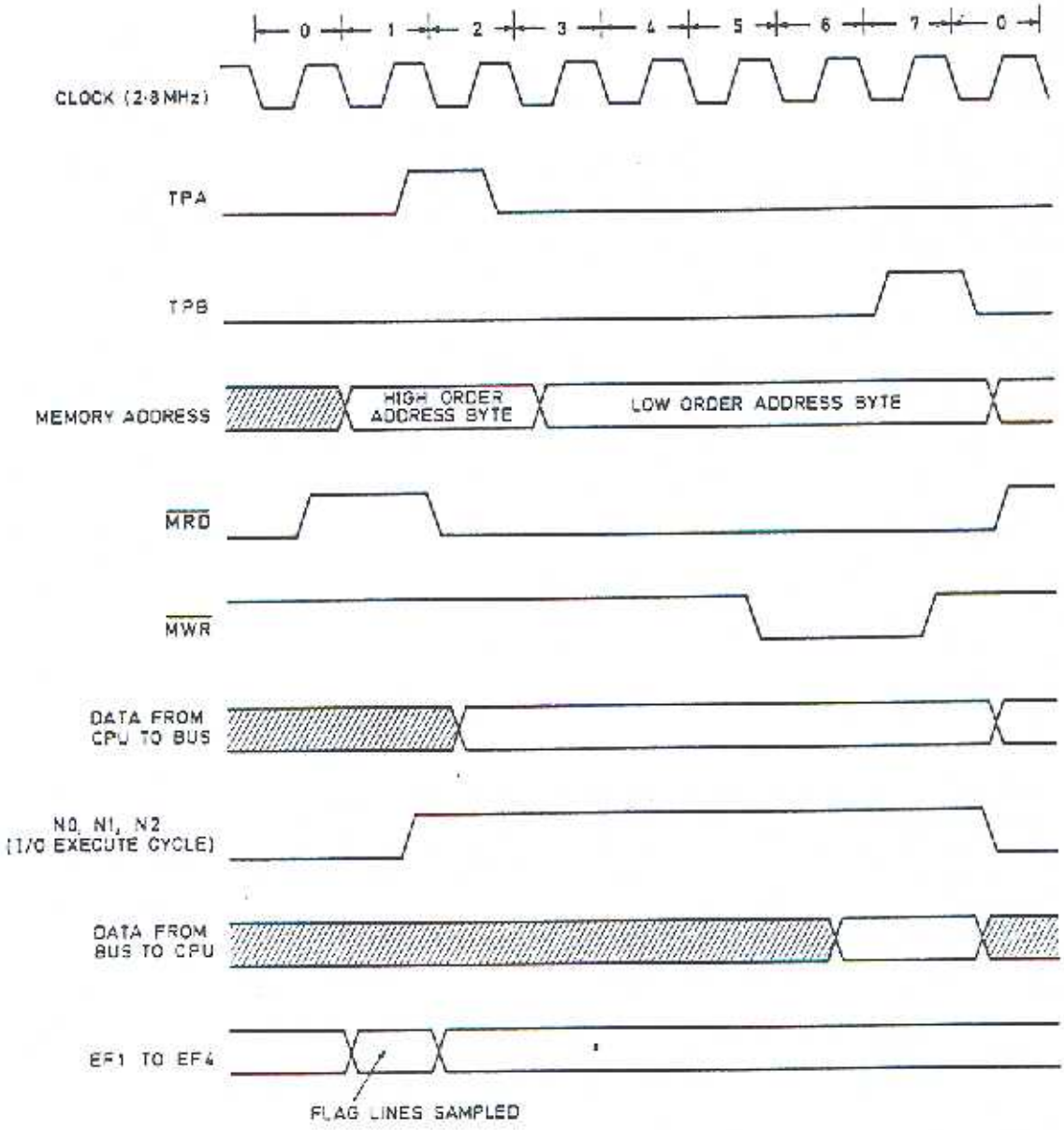
13. If the normal +24V supply is disconnected for any reason the volatile memory of RAM ML3 is maintained by a 3.6V back-up cell.

14. Under normal operating conditions diode D3 is reverse biased by the +10V supply on PL6/11, and D1 is forward biased which provides a trickle charge for the 3.6V back-up cell (PL6/10).

15. If the primary +24V supply should fail or be disconnected, D1 is biased off, and the RAM is supplied via D3 from the back-up cell. Diode D2 prevents the back-up cell from attempting to power the whole board during a power failure.

Supply voltage sensor

16. During normal operation tranistor TR2 is reverse biased by the +24V supply connected to PL6/8; with TR2 off, TR3 is held off maintaining a logic 1 condition on ML5C/9. If the +24 volt input falls to below +15.5V or is interrupted, transistor TR2 turns on, charging C32 and turning on TR3. This produces a logic 0 condition on ML5C/9. Capacitor C32 ensures that ~~when the 10V~~ IF IN THIS CONDITION 10.4V



NOTE: SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD.

Fig 1 Microprocessor timing waveforms

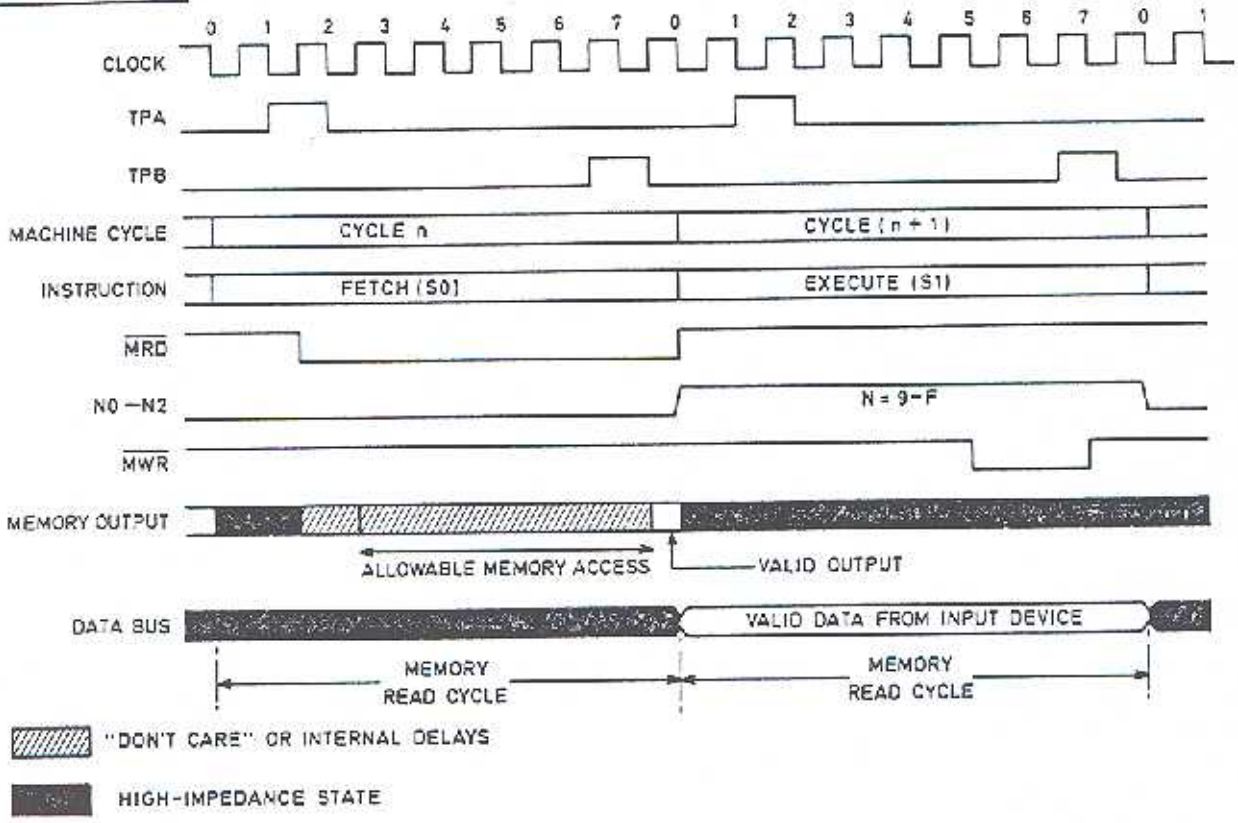


Fig 2 Input instruction timing

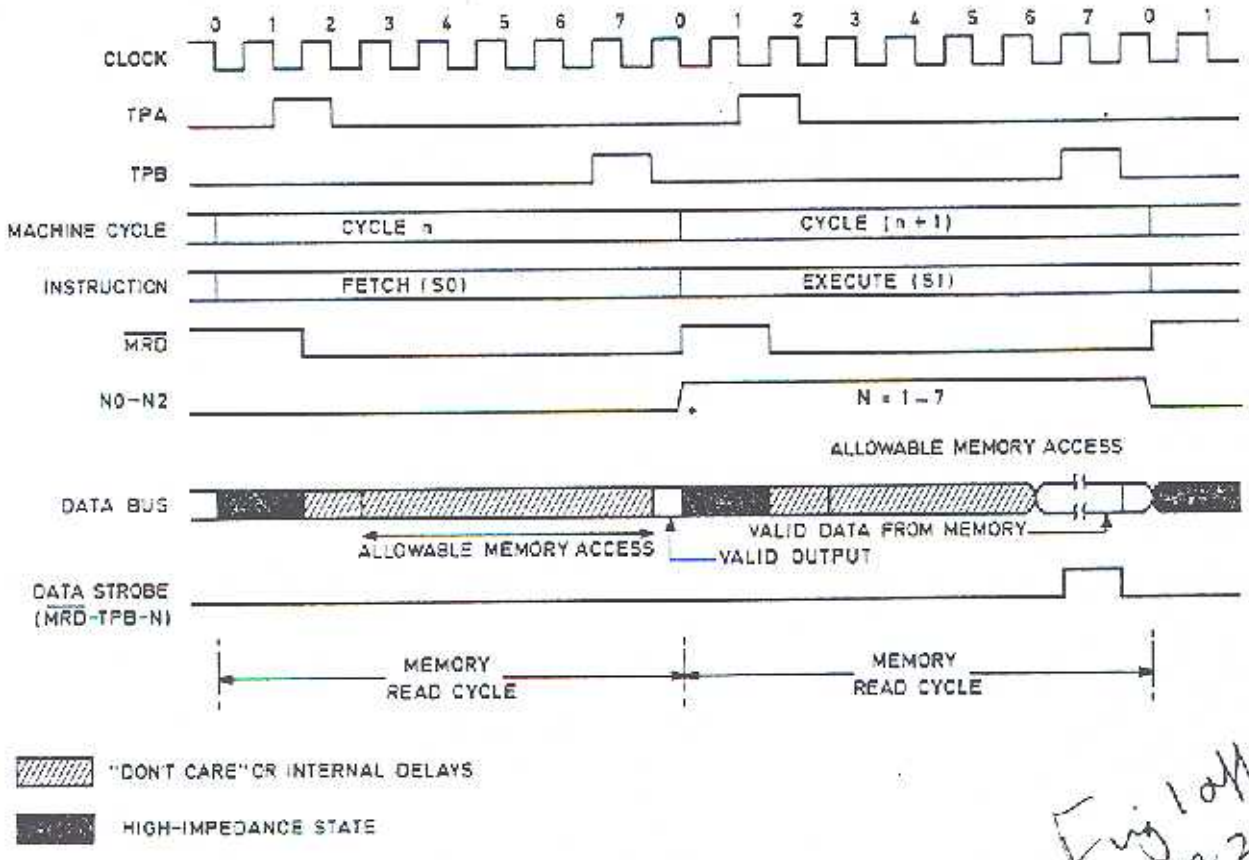


Fig 1 offeset after 2+3 !!

Fig 3 Output instruction timing

Oct.82

momentarily turning

rail collapses and TR2 ~~is turned~~ off, ~~momentarily~~ the input ML5C/9 remains as logic 0 holding the $\overline{CLR}$ input to the microprocessor active to reset the device. The $\overline{CLR}$ signal is also fed to TR1 which acts as an inverter to provide a $\overline{CS2}$ signal for the RAM (ML3), and also ensures the correct non-active logic level when the radio is either ON or OFF.

17. When power is connected to the board a logic 1 is put on the NAND Schmitt ML5C/9, and the voltage on ML5C/8 rises as C1 is charged through R12. When pin 8 reaches CMOS high trigger level the device output will be a logic 0, inverted by ML5D. This logic 1 $\overline{CLR}$ signal enables the start-up of the microprocessor. In this way start-up is delayed after initial switch ON.

Input/output ports

18. Chip selection of ports when an input/output instruction is being executed is effected by a logic 1 condition on the N outputs from the microprocessor as follows:

N0 - input/output 1 (ML9/ML10)
N1 - input/output 2 (ML11/ML12)
N2 - input/output 4 (ML13/ML14)

The N lines terminate on the CS2 inputs of the respective devices. The $\overline{MRD}$ output of the microprocessor connected to the CS1 inputs of the INPUT/OUTPUT devices indicates the direction of data transfer during an I/O instruction. The MODE input controls the sign of the CS1 input (active low for an output port, active high for an input port). When $\overline{MRD}$ is at logic 1 (indicating a memory write cycle), the relevant input port is selected to connect data from the control switches to the data bus and thence to the RAM. When $\overline{MRD}$ is at logic 0 (indicating a memory read cycle), the relevant output port is selected to route control information on the data bus through decoders to the Band-pass Filters, ATU, Synthesiser and Display modules. The data bus levels required to energise the appropriate module outputs are given in Tables 2, 3 and 4.

Table 2 - Output port 1: data bus values for given output functions

OUTPUT ENERGISED	FUNCTION	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7	BUS HEX VALUE
PL4/7	BPF RELAY SET 7	1	0	0	0	0	0	0	0	01
PL4/6	BPF RELAY SET 1	1	1	0	0	0	0	0	0	03
PL4/5	BPF RELAY SET 4	1	0	1	0	0	0	0	0	05
PL4/8	BPF RELAY SET 3	0	1	0	0	0	0	0	0	02
PL4/9	BPF RELAY SET 5	0	0	1	0	0	0	0	0	04
PL4/10	BPF RELAY SET 8	0	1	1	0	0	0	0	0	06
PL4/4	BPF RELAY SET 2	1	1	1	0	0	0	0	0	07
PL6/5	ATU TUNE COMPLETE	0	0	0	0	0	0	1	0	40
PL4/3	RESET BPF RELAYS	0	0	0	0	0	0	0	1	80
PL4/11	BPF RELAY SET 6	0	0	0	1	0	0	0	0	08
PL6/6	N.C. (POLARISING)	0	0	0	0	1	0	0	0	10

NOTE: DO6 of Port 2 must be '0' for above result (see Table 3).

Table 3 - Output port 2: data bus values for given output functions

SK5 PIN NO. ENERGISED	FUNCTION	D00	D01	D02	D03	D04	D05	D06	D07	BUS HEX VALUE
1	SET RLU	0	0	1	1	1	0	0	0	1C
21	RESET RLR	1	0	1	1	1	0	0	0	1D
25	RESET RLL	1	0	0	0	1	1	0	0	31
24	SET RLV	1	1	0	0	1	1	0	0	33
2	SET RLR	0	1	1	0	1	1	0	0	36
23	RESET RLQ	1	0	1	0	1	1	0	0	35
22	RESET RLP	1	1	1	0	1	1	0	0	37
5	RESET RLV/U	0	0	0	0	1	1	0	0	30
4	SET RLQ	0	1	0	0	1	1	0	0	32
3	SET RLP	0	0	1	0	1	1	0	0	34
28	RESET RLB	1	1	0	1	0	1	0	0	2B
29	RESET RLS	1	0	0	1	0	1	0	0	29
6	SET RLL	0	1	1	1	0	1	0	0	2E
27	RESET RLT	1	0	1	1	0	1	0	0	2D
26	RESET RLK	1	1	1	1	0	1	0	0	2F
9	SET RLB	0	0	0	1	0	1	0	0	28
8	SET RLT	0	1	0	1	0	1	0	0	2A
7	SET RLK	0	0	1	1	0	1	0	0	2C
20	RESET RLG	0	1	1	1	1	0	0	0	1E
30	RESET RLM	1	1	0	1	1	0	0	0	1B
31	RESET RLN	1	0	0	1	1	0	0	0	19
11	SET RLM	0	0	0	1	1	0	0	0	18
10	SET RLS	0	1	0	1	1	0	0	0	1A
35	RESET RLF	1	0	0	0	1	0	0	0	11
34	RESET RLE	1	1	0	0	1	0	0	0	13
12	SET RLN	0	1	1	0	1	0	0	0	16
33	RESET RLD	1	0	1	0	1	0	0	0	15
32	RESET RLC	1	1	1	0	1	0	0	0	17
15	SET RLE	0	0	0	0	1	0	0	0	10
14	SET RLD	0	1	0	0	1	0	0	0	12
13	SET RLC	0	0	1	0	1	0	0	0	14
38	SET RLH	1	1	0	1	0	0	0	0	0B
39	SET RLG	1	0	0	1	0	0	0	0	09
16	SET RLF	0	1	1	1	0	0	0	0	0E
37	RLA ATU	1	0	1	1	0	0	0	0	0D
36	SET RLJ	1	1	1	1	0	0	0	0	0F
19	RESET RLH	0	0	0	1	0	0	0	0	08
18	RLA 50 ohm	0	1	0	1	0	0	0	0	0A
17	RESET RLJ	0	0	1	1	0	0	0	0	0C

Table 4 - Output port 4: data bus values for given output functions

OUTPUT ENER-GISED	FUNCTION	DO0	DO1	DO2	DO3	DO4	DO5	DO6	DO7	BUS HEX VALUE
PL2 3	SYNTH. ADDRESS 1 (VCO/MODE)	0	0	0	0	1	0	0	0	10*
PL2 12	SYNTH. ADDRESS 2	0	0	0	0	0	1	0	0	20*
PL2 4	SYNTH. ADDRESS 3 (PROG. ENABLE 2)	0	0	0	0	1	1	0	0	30*
PL2 11	SYNTH. ADDRESS 4 (PROG. ENABLE 3)	0	0	0	0	0	0	1	0	40*
PL2 5	SYNTH. ADDRESS 5	0	0	0	0	1	0	1	0	50*
PL2 10	SYNTH. ADDRESS 6 (SYNTH. P.C.)	0	0	0	0	0	1	1	0	60*
PL3 10	DISP. ADDRESS 1	0	0	0	0	1	0	0	0	10
PL3 5	DISP. ADDRESS 2	0	0	0	0	0	1	0	0	20
PL3 11	DISP. ADDRESS 3	0	0	0	0	1	1	0	0	30
PL3 4	DISP. ADDRESS 4	0	0	0	0	0	0	1	0	40
PL3 12	DISP. ADDRESS 5	0	0	0	0	1	0	1	0	50
PL3 3	DISP. ADDRESS 6	0	0	0	0	0	1	1	0	60
PL3 1	DISP. ENABLE	0	0	0	0	0	0	0	1	80
PL2 13	SYNTH.FREQ. DATA 3	0	0	0	1	0	0	0	0	08
PL2 2	SYNTH.FREQ. DATA 2	0	0	1	0	0	0	0	0	04
PL2 14	SYNTH.FREQ. DATA 1	0	1	0	0	0	0	0	0	02
PL2 1	SYNTH.FREQ. DATA 0	1	0	0	0	0	0	0	0	01
PL3 8	DISP.FREQ. DATA 3	0	0	0	1	0	0	0	0	08
PL3 7	DISP.FREQ. DATA 2	0	0	1	0	0	0	0	0	04
PL3 9	DISP.FREQ. DATA 1	0	1	0	0	0	0	0	0	02
PL3 6	DISP.FREQ. DATA 0	1	0	0	0	0	0	0	0	01

*DO7 of Port 2 must be '1' for these outputs.

19. The DO3, DO4, and DO5 outputs of O/P port 2 are routed to mux/demux device ML31 where they are used to select the D3 input to one of the five BCD to decimal decoders, ML25 to ML29, and mark it with a logic 0 condition. The unmarked D3 inputs of the other four decorders are all pulled high by ML39A resistors and outputs will occur on unused pins Q8 and Q9. Hence the DO0, DO1 and DO2 outputs of the O/P port 2, which are common to all five decoders, will only cause one of the ATU set/reset lines to be pulsed from the device marked with logic 0.

SOFTWARE

20. A complete print out of the software program used on the microprocessor board is outside the scope of this service manual. As already stated in the introductory paragraph (Para. 1) a suitably programmed computer is required for fault diagnosis in this area. However, to illustrate the basic sequence of operations controlled by the software program, the flow chart in Fig.6 has been appended.

TESTING AND ALIGNMENT

21. Testing information for this board will be found in Part 4 of this manual. There are no alignment adjustments.

COMPONENTS LIST

22. The principal component parts of Microprocessor Board 419/1/51171 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C1	Electrolytic 1uF 20% 35V	BS9073 F002 or F005	402/4/55748/007
C2,4,5, 20,21, 26,28, 31	10nF 20% 63V	Wima MK52	435/4/90829/026
C3	Electrolytic 2.2uF 20% 16V	BS9073 F002 or F005	402/4/55746/009
C22,24, 25	100nF 5% 100V	Siemens B32560-D1104J	435/4/90317/014
C23,30	Electrolytic 22uF 16V	CECC 30201-003/016PTE	402/4/56132/220
C27	470nF 5% 100V	Siemens B32561-D1474J	435/4/90827/003
C29	Electrolytic 4.7uF 10% 16V	CECC 30201-003/016PTC	402/4/56131/470
C32	Electrolytic 4.7uF 10% 16V	CFCC 30201-003	402/4/56171/470
	RESISTORS		
R1,78, 79,81, 82	22k 2% 0.25W	Metal oxide film	403/4/05524/220
R12	560k 5% 0.33W	Metal oxide film	403/4/07177/560
R14	10M 5% 0.25W	Metal oxide film	403/4/07118/013
R26,27, 64,77	220k 2% 0.25W	Metal oxide film	403/4/05525/220
R59	100 ohm 2% 0.25W	Metal oxide film	403/4/05522/100
R63	5.6k 2% 0.25W	Metal oxide film	403/4/05523/560
R65	4.7k 2% 0.25W	Metal oxide film	403/4/05523/470
R66	1.8k 2% 0.25W	Metal oxide film	403/4/05523/180
R67	6.8k 2% 0.25W	Metal oxide film	403/4/05523/680
R68	18k 2% 0.25W	Metal oxide film	403/4/05524/180
R69	4.7M 5% 0.25W	Metal glaze Mullard VF25	403/4/07118/009
R70,	47k 2% 0.25W	Metal oxide film	403/4/05524/470
R71,75	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R72	15k 2% 0.25W	Metal oxide film	403/4/05524/150
R73	1.5k 2% 0.25W	Metal oxide film	403/4/05523/150
R76	100k 2% 0.25W	Metal oxide film	403/4/05525/100
	INTEGRATED CIRCUITS		
ML1*	ROM (Programmed)	HUGHES HCMP 18344-269	445/1/10632/001
ML2*	ROM (Programmed)	HUGHES HCMP 18344-268	445/1/10632/002
ML3*	RAM		445/4/03373/823
ML4*	Microprocessor	CDP1802 AEX	445/4/03373/802

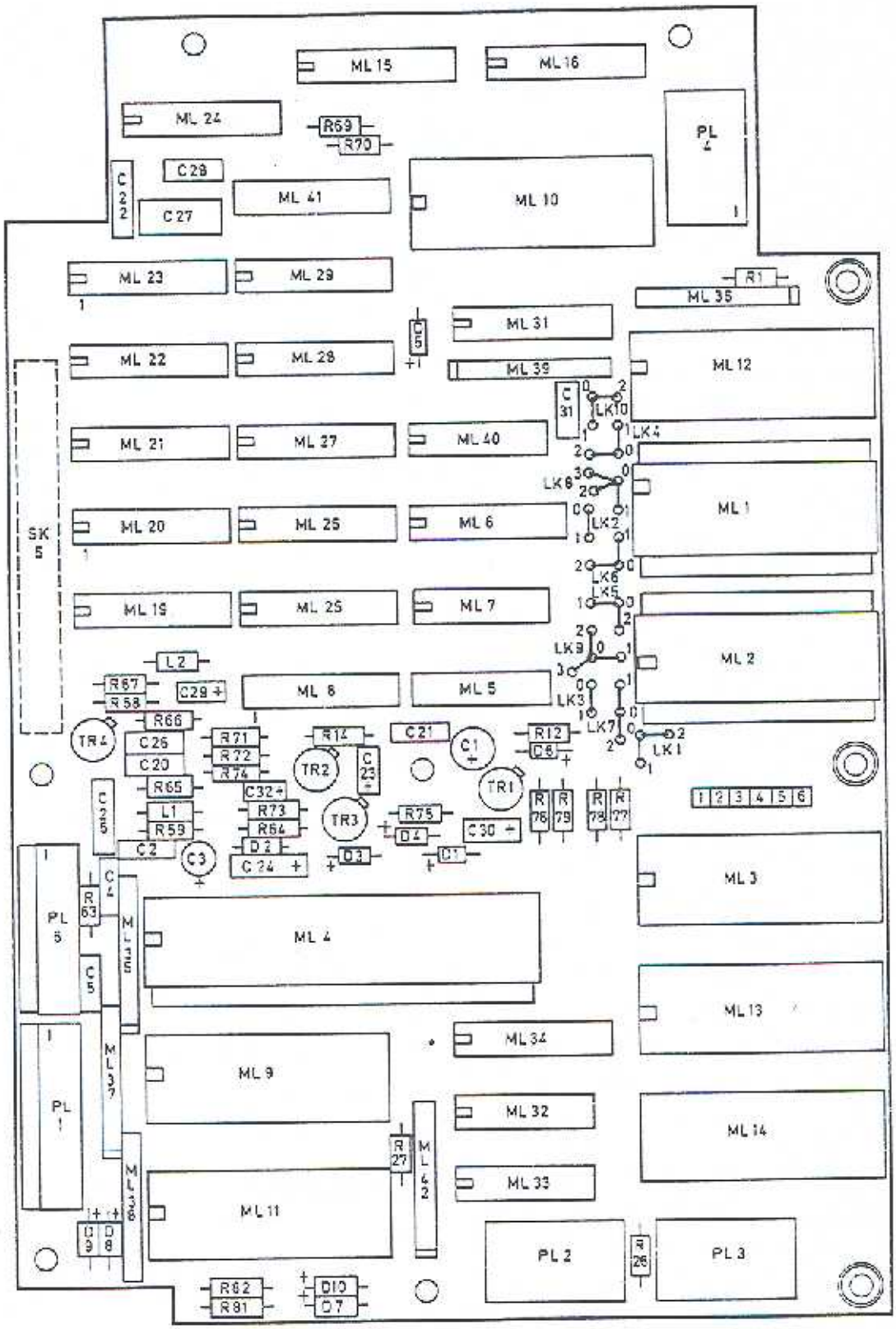
continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
ML5*	Quad 2-input NAND Schmitt	CD4093BCN	445/4/03234/093
ML6*	Quad clocked D-latch	CD4042BCN	445/4/03234/042
ML7*	Dual D type flip-flop	CD4013BCN	445/4/03234/013
ML8*	Hex Inverter/Buffer	CD4049BCN	445/4/03234/049
ML9-14*	Input/Output Port 8-bit	CDP1852EX	445/4/03373/852
ML15, 25-29, 34*	BCD-Decimal Decoder	CD4028BCN	445/4/03234/028
ML16, 19-24	Transistor Array	ULN2004ABU	445/9/03262
ML31*	8 Channel Multiplexer	CD4051BCN	445/4/03234/051
ML32,33, 40*	Quad 2-input AND Gate	CD4081BCN	445/4/03234/081
ML35, 37-39, 42	Resistor network 7 x 220k	Bourns 4308R-101-224	403/4/07075/220
ML36	Resistor network 2 x 22k	Bourns 4308R-101-223	403/4/07074/220
ML41*	Dual monostable	HCF4098BEX	445/4/10806/098
	MISCELLANEOUS		
D1,5,7-10	Diode - switching	IN4148	415/4/98869
D2,3,6	Diode - Schottky	Hewlett Packard HSCH1001	415/4/05789
D4	Diode - 5.6V regulator	BZX79-C5V6	415/4/05830/010
TR1	Transistor N-P-N	BSY95A	417/4/02166
TR2	Transistor P-N-P	BCY70	417/4/01721/001
TR3,4	Transistor N-P-N	BC107B	417/4/02028/004
L1	Inductor RF 15 uH 10%	BS9751 N0001 PATTA	406/4/32161/027
L2	Inductor RF 47 uH 10%	BS9751 N0001 PATTA	406/4/32161/033
PL1 (Lower)	Connector: 2 part, 10 male	Berg 75160-103-10	508/4/22211/010
PL1 (Upper)	Connector: 2 part, 10 male	Berg 75168-109-10	508/4/22212/010
PL6 (Lower)	Connector: 2 part, 9 male	Berg 75168-103-09	508/4/22211/009
PL6 (Upper)	Connector: 2 part, 9 male	Berg 75168-109-09	508/4/22212/009
SK5	Connector 40 contacts	Berg 76325-220	508/4/24138/020

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. THESE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.



TR1 – TR4
COMPONENT SIDE VIEW

Fig 5 Microprocessor board – component layout

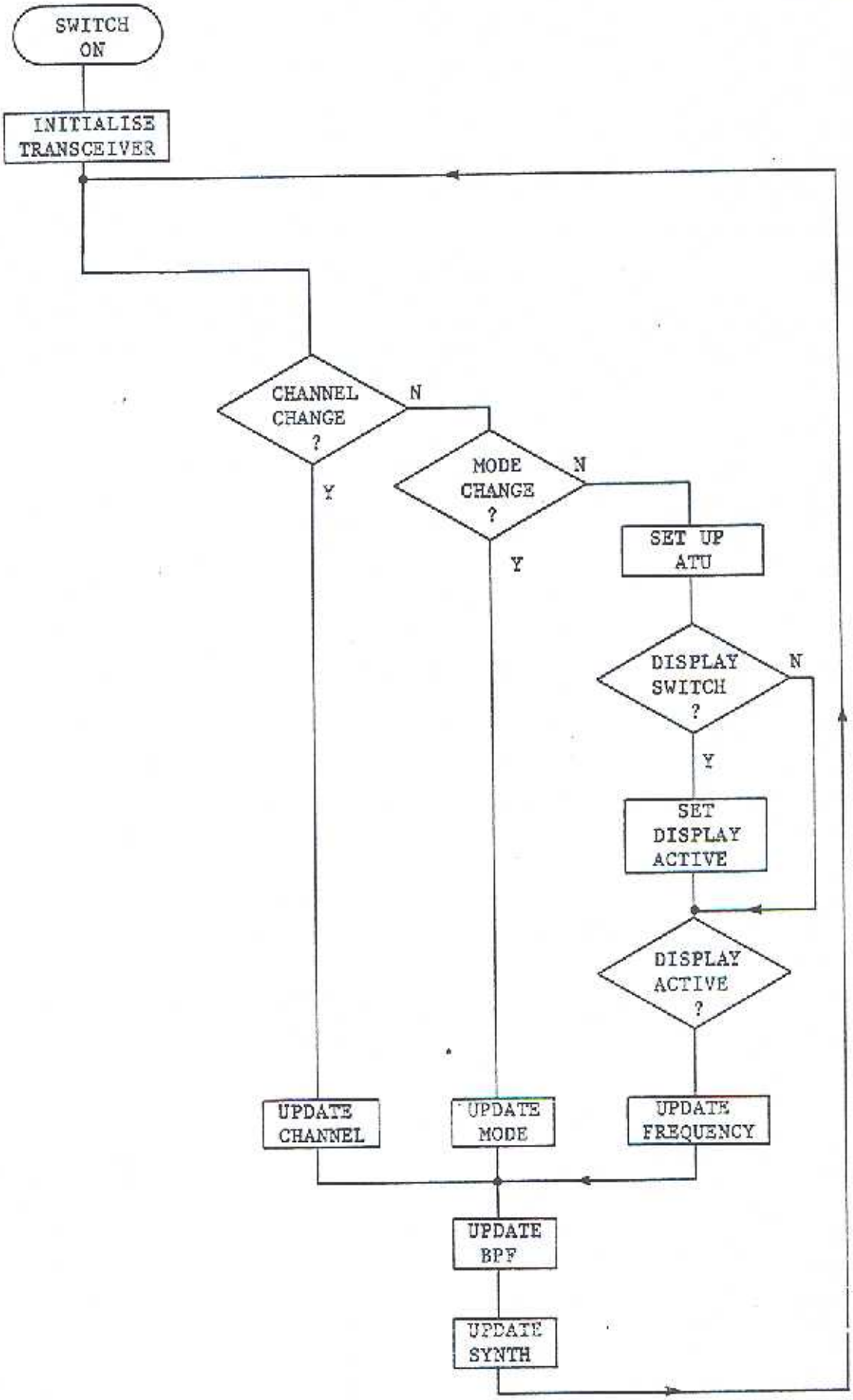


Fig.6 Basic flow chart of software program

Fig 2a

Fig 4a

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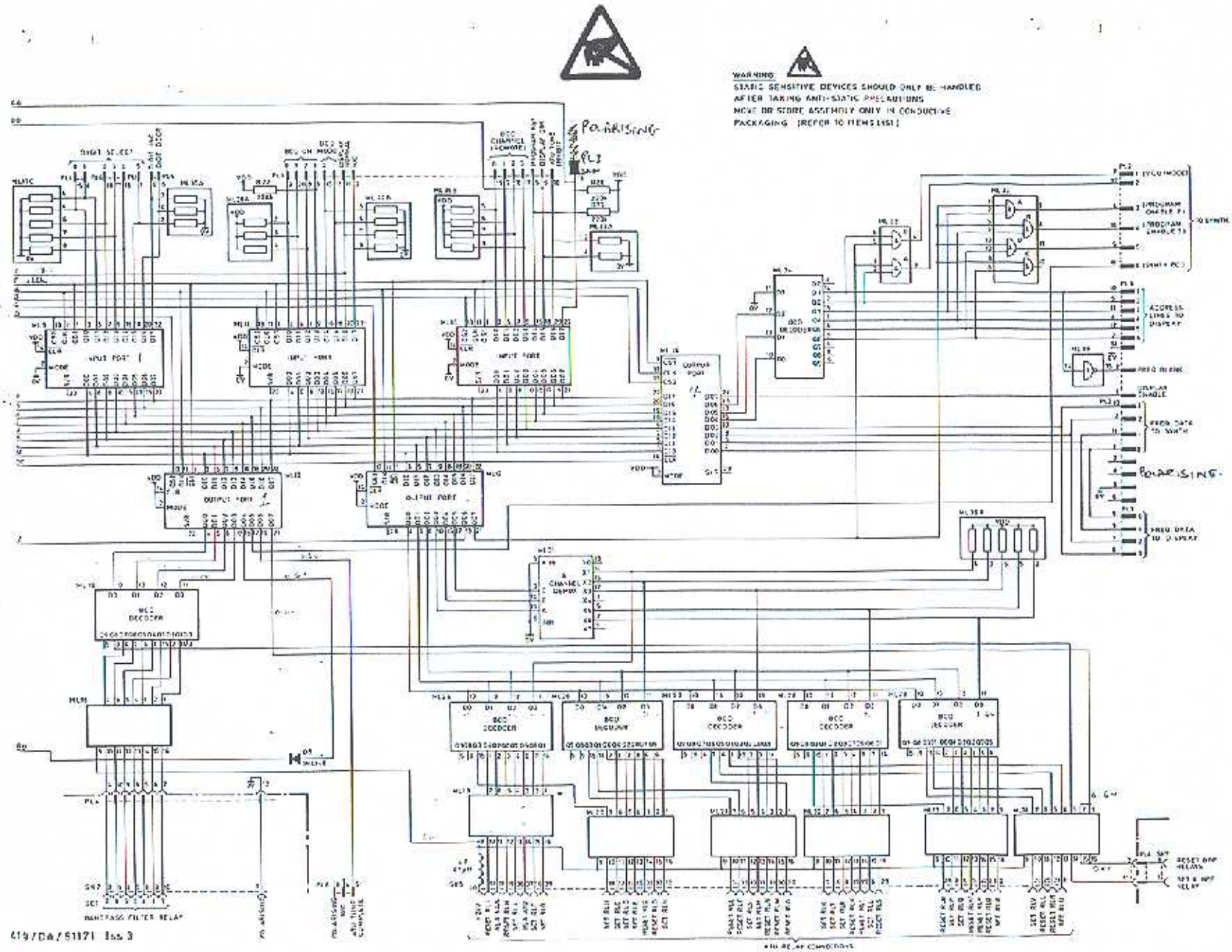

Fig 4b

Microprocessor board : circuit diagram

THIRD LINE SERVICING

OF

FILTER BOARD - REAR 419/1/66405

CONTENTS

	Para.
Technical description	1
Testing and alignment	2
Components list	3

ILLUSTRATIONS

Fig.
1 Filter board - rear : circuit diagram
2 Filter board - rear : component layout

TECHNICAL DESCRIPTION

1. The Filter Board is equipped with bead ferrite inductors and ceramic capacitors to provide decoupling of any ancillary equipment connected to the rear panel connectors on the radio. A circuit diagram of the board is given in Figure 1.

TESTING AND ALIGNMENT

2. Testing of the Filter Board is covered in Part 4 of this manual. There are no alignment adjustments.

COMPONENTS LIST

3. The principal components parts of Filter Board 419/1/66405 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C1-18	Capacitor 10nF 20% 100V	BS9075	400/4/21712/100
L1-12, 14,15, 17-21	Ferrite bead inductor	Mullard FX1115/A1	905/9/98000
R1	Resistor 10k 2% 0.25W	Metal oxide film	403/4/05524/100
PL1 (Lower)	Plug rt. angled 12-way	75168-101-11	508/9/22073/012
PL1 (Upper)	Plug rt. angled 12-way	75168-107-11	508/9/22074/012
PL4	Plug 7-way	Amphenol 620B/5016/10/7PB	508/4/24187
SK1	Socket 7-way	Amphenol 6208/5016/10/7S	508/4/24131/002
SK5	Socket 10-way	Amphenol 6208/5024/12/10S	508/4/24134/001
FS1	Fuse 0.125A	Littlefuse 275/0.125	
FS2	Fuse 2A	Littlefuse 275/2A	518/4/90467/009

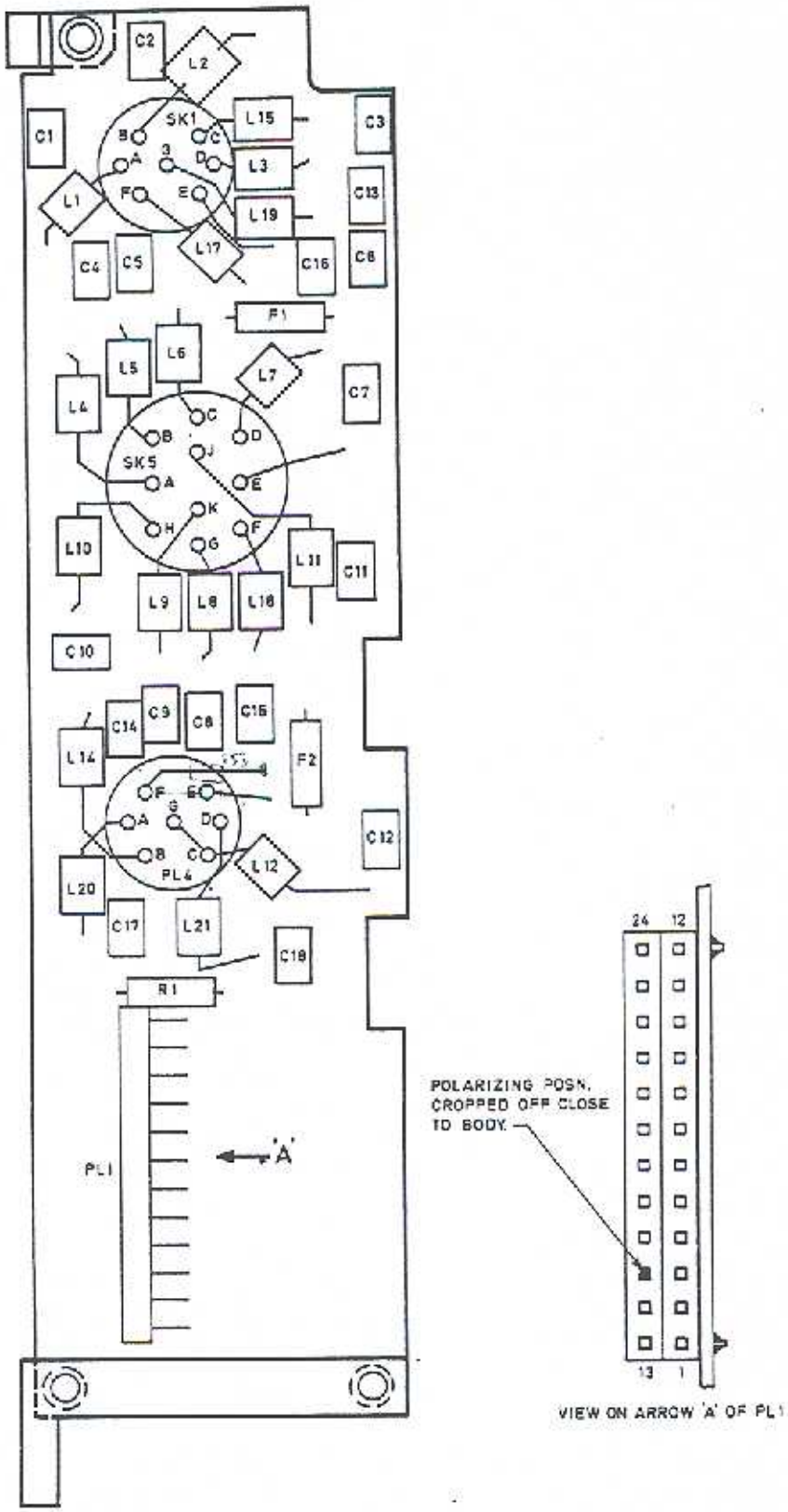

Fig 2 Filter board (rear) – component layout

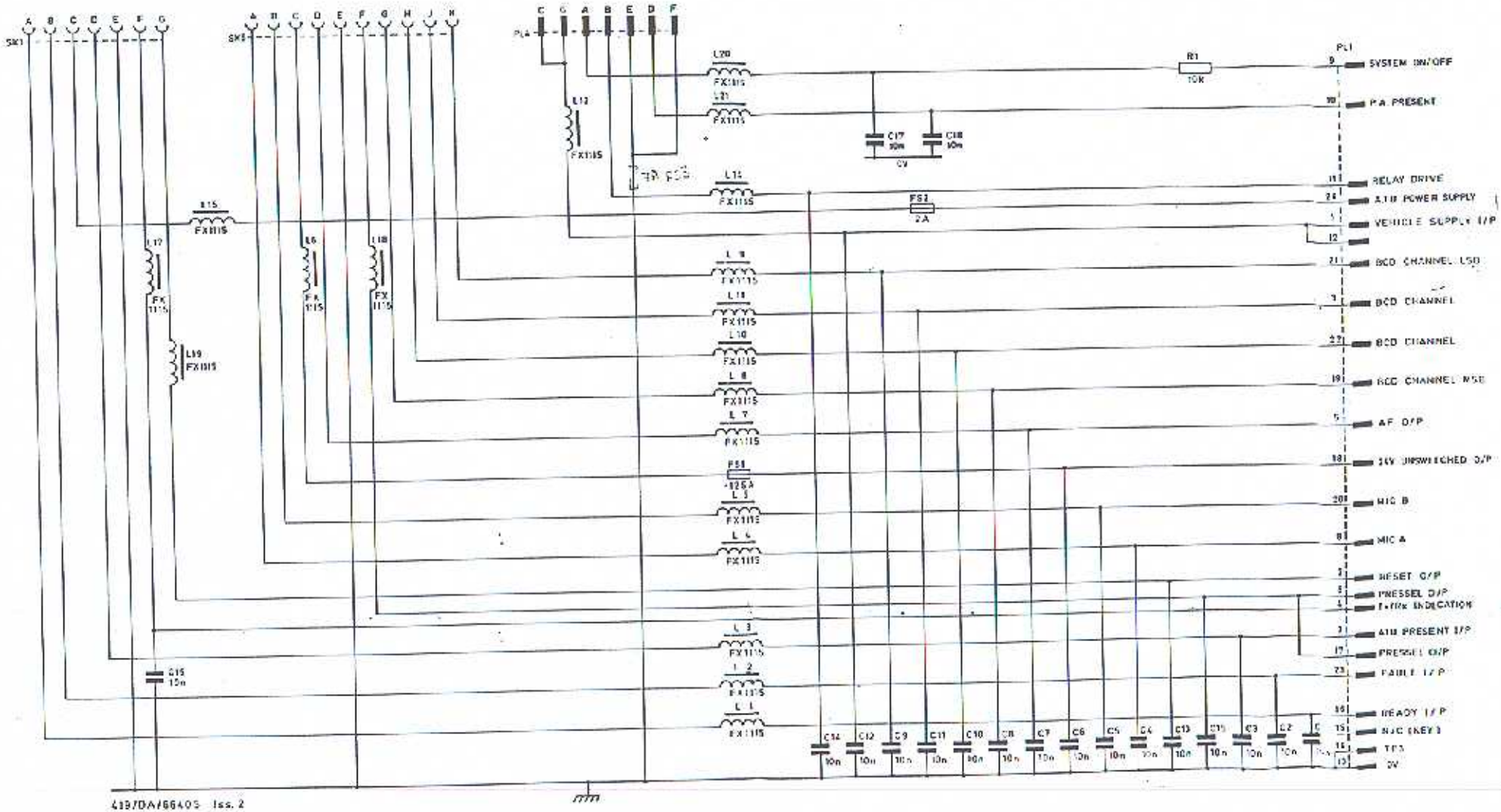

Fig.1 Filter board - rear : circuit diagram

Fig

THIRD LINE SERVICING

OF

INTERMEDIATE FREQUENCY BOARD 419/1/51177

CONTENTS

	Para.
Technical description	
General	1
Circuit description	5
Transmit circuitry	6
Receive circuitry	10
Testing and alignment	14
Components list	15

ILLUSTRATIONS

Fig.

1 IF board : circuit diagram

2 IF board : component layout

TECHNICAL DESCRIPTION

General

1. The Intermediate Frequency Board circuitry is divided into two parts; one serving the transmit (Tx) direction ~~of transmission~~; the other serving the receive (Rx) direction.

2. The transmit circuitry:

   (1) Derives a second IF carrier at 38 MHz from a modulated 1.4 MHz first IF.

   (2) Mixes the second IF (38 MHz) with a frequency in the range 39.5 MHz to 68 MHz, to produce a selected transmission frequency in the range 1.5 MHz to 30 MHz.

3. The receive circuitry:

   (1) Derives a 1.4 MHz second IF from a 38 MHz first IF.

   (2) Demodulates the 1.4 MHz second IF to recover the AF signal component.

   (3) Provides AGC.

4. The board is also equipped with (a) remote controlled switches which are used to discriminate between AM and SSB transmissions; and (b) IF and AF amplifier stages.

Circuit description

5. A circuit diagram of the IF Board is given in Figure 1. The transmit and receive circuitry are treated separately in the following description.

Transmit circuitry

6. An 0V condition on PL1/7 operates reed relays RLA and RLB; contacts RLA1 and RLB1 disconnect the receive path through FL2 and complete the transmit path.

7. Consider first the operation of the circuit for SSB/CW mode. The modulated 1.4 MHz IF enters the board at pin 6 and is connected by contact ML1C to crystal filter FL1 which is tuned to pass the upper sideband of the 1.4 MHz carrier. The USB from the filter is connected via ML2B, LK4 and C29 to pin 7 of the double balanced modulator ML6 which functions as the 1st Tx mixer stage. The BFO input to the mixer enters the board at PL2/3 and is connected to potential divider R24 and R25. Capacitor C30 connects the incoming BFO frequency to ML6/3. The BFO frequency will be 36.6 MHz for LSB transmissions or 39.4 MHz for USB transmissions depending on the mode selected by the external radio controls.

8. The output carrier of the 1st mixer (ML6/6) at the 2nd IF frequency of 38 MHz is amplified by TR10 and TR5 and connected via contact RLA1 operated through the 38 MHz ± 4 kHz bandpass filter FL2, and contact RLB1 operated, to the 2nd Tx mixer MX1. The beat frequency for the 2nd mixer enters the board at PL1/4 and is in the range 39.5 - 68 MHz, depending on the frequency selected for the radio channel in use. The difference frequency in the range 1.5 - 30 MHz leaves the mixer on MX1/3/4, is amplified by the TR2/TR9 circuit, and leaves the board on PL1/1. The output level at PL1/1 is approximately +5 dBm.

9. Bilateral switches ML1, ML2, and ML8 are operated by a logic level 1 on the relevant board pin as follows:

Logic 1 on pin No.	Switch operated	Function
7 (Rx)	ML1B and ML2D if ML1A is operated by $\overline{AM}$ = 1	Routes SSB Rx path via FL1.
8 (Tx $\overline{AM}$)	ML1C and ML2B	Routes SSB and CW Tx path via FL1.
9 ($\overline{AM}$)	ML1A	Completes operate path for ML1B and ML2D.
	ML8B and ML8C	AGC GENERATOR Connects audio output path for SSB Rx.
10 (AM)	ML1D and ML2A	Bypasses FL1 for AM Rx path.
	ML2C	Bypasses FL1 for AM Tx path.
	ML8D	Connects audio output path for AM Rx.

NO TX PATH DESCRIPTION FOR AM — 2ND LO = 36.6 MHz
HIGH ON DIFFERENT PIN, USB FILTER BYPASSED

Receive circuitry

10. Received signals at the first Rx IF carrier frequency of 38 MHz are connected to the board at PL1/6. In the receive mode relays RLA and RLB are released, and the incoming signal is connected via IF amplifier TR11, T2 C3, and C4 to one gate of a dual gate FET TR1. The circuitry of TR1 forms a mixer stage to change the carrier from 1st to 2nd Rx IF, and the BFO frequency for this stage is connected to the second gate of TR1 from PL2/3. The BFO frequency on PL2/3 will be either 36.6 MHz for LSB or AM; or 39.4 MHz for USB or C.W. The output of the mixer is at the 2nd Rx carrier frequency of 1.4 MHz and the routeing from here on depends on whether AM or SSB mode of transmission is in use. Consider first an incoming AM signal.

11. The 1.4 MHz output of TR1 (38 MHz - 36.6 MHz) is routed via C9, ML1D and ML2A to C10 and the base of TR3. The amplified signal on the emitter of TR3 is passed through two further stages of amplification, at ML3 and ML4 to the input of ML5 which combines the functions of AM detector, SSB demodulator, AF amplifier, and AGC generator. In the case of the AM signal being considered, ML5 acts as a detector stage, and linear AF amplifier: the audio output from ML5/1 is connected via contact ML8D to amplifier stages TR7 and TR8. The Rx audio signal leaves the board on output pin 1 at a signal level of approximately 50 mV (AM). *

12. When an SSB signal is being received, the routeing of the 2nd Rx IF from TR1 is via C9, ML1B operated, to the USB pass band filter. Contact ML2D is operated (see para.9) and the output of the filter is connected to the amplifier stages TR3, ML3, and ML4, and into ML5 as before. In ML5 the SSB signal is demodulated and the recovered audio appears on ML5/8; it is then buffered by TR6 and connected via contact ML8C to the AF amplifier stages TR7 and TR8, before leaving the board at pin 1. The level of the (SSB) audio output from the board is about 50 mV.

13. Potentiometer R32 is used to tap off some of the audio power on the emitter of TR6 and feed it via C38, and contact ML8B to the AGC generator ML7. The dc output of ML7 is routed from ML7/2 to join the AGC output of ML5/4 and to form the common AGC line at R14. From here it is routed via LK1 to ML4/7 and ML3/7, and by R48 to the inverting input of operational amplifier ML9(the dc output of ML9/6 is used to control the bias on TR1/gate 1, and hence the signal level into the amplifier stages at TR3/base.) The AGC range is 90 dB min. on SSB, and 60 dB min. on AM.

Testing and alignment

14. Testing and alignment information for this board is given in Part 4 of this manual.

* AM AGC provided by ML5 alone to control ML3, 4 & TR1.

COMPONENTS LIST

15. The principal components of Intermediate Frequency Board 419/1/51177 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C1,6,22-25,27,28-34,36,47-49,53,54,57,59,60	10nF 5% 63V	Wima MKS2	435/4/90829/023
C2,4,11,15,18,44,55	2.2nF		435/4/90821/012
C3	16pF variable 250V	Mullard 809 09003	401/9/32136/003
C5	22pF 2% 100V	Mullard 632-34229	400/4/20674/014
C7,21,42,46,52	100nF 5% 100V	Siemens B32560-D1104J	435/4/90317/014
C8	100pF 1% 400V	BS9070 N002 C2AED-C	438/4/25352/100
C9	52pF variable 300V	Mullard 809 08003	401/4/32131/002
C10,43	1nF 5% 100V	Wima FKS2	435/4/90821/001
C12,14,16	220nF 5% 100V	Siemens B32560-D1224J	435/4/90317/017
C13,17	100pF 2% 100V	Mullard 632-34101	400/4/20674/022
C19,45	47uF 10% 6V	CECC 30201-003	402/4/56122/470
C20	1uF 10% 20V		402/4/56271/100
C26	220pF 2% 100V	Mullard 632-58221	400/4/20674/026
C35,56	100nF 5%	Wima MKS2	435/4/90829/016
C37	6.8uF 10% 10V	CECC 30201-003/016 PTC	402/4/50261/680
C38,50	2.2uF 10% 10V	CECC 30201-003/016 PTB	402/4/56261/220
C39	47uF 10% 20V	CECC 30201-003/016 PTF	402/4/56272/470
C40,41	100uF 10% 10V	CECC 30201-003/016 PTF	402/4/56263/100
C51	22uF 10% 10V	CECC 30201-003/016 PTD	402/4/56262/220
C58	10pF 2% 100V	Mullard 632-10109	400/4/20674/010
C61	18pF 2% 100V	Mullard.632-10189	400/4/20674/013
	RESISTORS		
R1	15k 2% 0.25W	Metal oxide film	403/4/05524/150
R2	36k 2% 0.25W	Metal oxide film	403/4/05524/360
R3	24k 2% 0.25W	Metal oxide film	403/4/05524/240
R4	27k 2% 0.25W	Metal oxide film	403/4/05524/270
R5	270 ohms 2% 0.25W	Metal oxide film	403/4/05522/270
R6	1.5k 2% 0.25W	Metal oxide film	403/4/05523/150
R7	1.2k 2% 0.25W	Metal oxide film	403/4/05523/120
R8	3.9k 2% 0.25W	Metal oxide film	403/4/05523/390
R10,37	390 ohms 2% 0.25W	Metal oxide film	403/4/05522/390

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R11,12, 21,27, 45,51, 52	100 ohms 2% 0.25W	Metal oxide film	403/4/05522/100
R13	470 ohms 2% 0.25W	Metal oxide film	403/4/05522/470
R14,20, 23,28, 33	1k 2% 0.25W	Metal oxide film	403/4/05523/100
R15-18	100k 2% 0.25W	Metal oxide film	403/4/05525/100
R19	2.7k 2% 0.25W	Metal oxide film	403/4/05523/270
R22,30, 57	51 ohms 2% 0.25W	Metal oxide film	403/4/05521/510
R24	680 ohms 2% 0.25W	Metal oxide film	403/4/05522/910
R25	330 ohms 2% 0.25W	Metal oxide film	403/4/05522/330
R26,44	240 ohms 2% 0.25W	Metal oxide film	403/4/05522/240
R29	200 ohms 10% 0.5W	Variable 3329H/81E	404/9/05032/009
R31	20 ohms 2% 0.25W	Metal oxide film	403/4/05521/200
R32	5k 10% 0.5W	Variable	404/9/05032/005
R34,35, 46,47	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R36	7.5k 2% 0.25W	Metal oxide film	403/4/05523/750
R38	68k 2% 0.25W	Metal oxide film	403/4/05524/680
R39	33k 2% 0.25W	Metal oxide film	403/4/05524/330
R40,55	510 ohms 2% 0.25W	Metal oxide film	403/4/05522/510
R41	10 ohms 2% 0.25W	Metal oxide film	403/4/05521/100
R42	1.8k 2% 0.25W	Metal oxide film	403/4/05523/180
R43	2.4k 2% 0.25W	Metal oxide film	403/4/05523/240
R48	9.1k 2% 0.25W	Metal oxide film	403/4/05523/910
R49	130k 2% 0.25W	Metal oxide film	403/4/05524/130
R50	130 ohms 2% 0.25W	Metal oxide film	403/4/05522/130
R53	22 ohms 2% 0.25W	Metal oxide film	403/4/05521/220
R54	150 ohms 2% 0.25W	Metal oxide film	403/4/05522/150
R56	24 ohms 2% 0.25W	Metal oxide film	403/4/05521/240
	TRANSISTORS		
TR1	N-channel: dual gate	RCA 40823	417/4/02040/002
TR2,5,9	N-P-N 1W	2N3866	417/4/01940
TR3,6-8	N-P-N 0.3W	BC109C	417/4/02028/009
TR4,10	N-P-N 0.36W	2N2369A	417/4/00496/000
TR11	N-P-N 200 mW	Texas BF357K	417/4/02162
	INTEGRATED CIRCUITS		
ML1,2,8*	Quad bilateral switch	National CD4066BCNA	445/4/03234/066
ML3,4	Linear IF amplifier	Plessey SL1612C	445/4/10799
ML5	Linear AF amplifier	Plessey SL623C	445/4/10801
ML6	Double bal. modulator	Plessey SL1640C	445/4/10802
ML7	AM amp./AGC generator	Plessey SL1621C	445/4/10800

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	INTEGRATED CIRCUITS contd		
ML9	Operational amp.	RCA CA3130EX	445/4/03193/003
MX1	Double bal. mixer	Mini-ccts. type SRA-1	509/4/07375/001
	INDUCTORS		
L1,4,5, 11,12	47uH 10%	BS9751 N0001 PATT A	406/4/32161/033
L2,6	0.33uH 10%	BS9751 N0001 PATT A	406/4/32161/007
L3	100uH 10%	BS9751 N0001 PATT A	406/4/32161/037
L7-9	3.3uH 10%	BS9751 N0001 PATT A	406/4/32161/019
L10	1uH 10%	BS9751 N0001 PATT A	406/4/32161/013
L14	15uH 10%	BS9751 N0001 PATT A	406/4/32161/027
	MISCELLANEOUS		
FL1	USB filter 1.4MHz	STC/CATHODEON	422/9/07789
FL2	BP filter 38MHz ± 4kHz	STC/CATHODEON	422/9/07788
D1	Diode	1N4148	415/4/98869
T1-3	Transformer assy.	Plessey	406/1/31850
RLA,RLB	Reed relay 1750 ohms	Astralux type 1210-5	507/4/38446/007
Pins 1-6	Plug 6-way	Type 75160-110-6	508/9/24125/006
Pins 7-10	Plug 4-way	Type 75160-109-4	508/9/25124/004
Pins 11-15	Plug 5-way	Type 75160-108-15	508/9/25290/005
LK1	Socket 2-way	Berg type 65474-004	508/4/22197/004
LK2	Cable assy. RF	Plessey	630/1/38928
LK3	Cable assy. RF	Plessey	630/1/38929
LK4	Cable assy. RF	Plessey	630/1/43056

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. STATIC SENSITIVE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-SIATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.

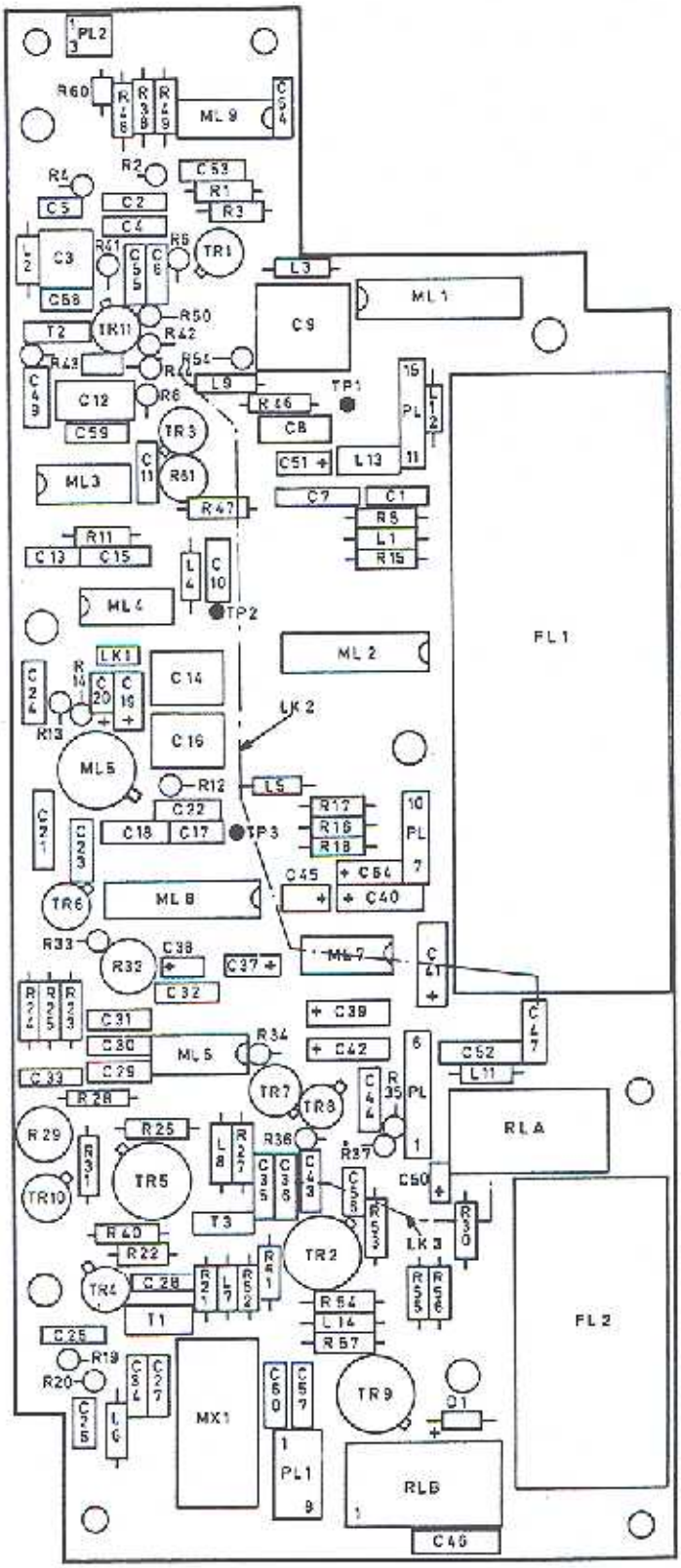

Fig 2 I.F board – component location

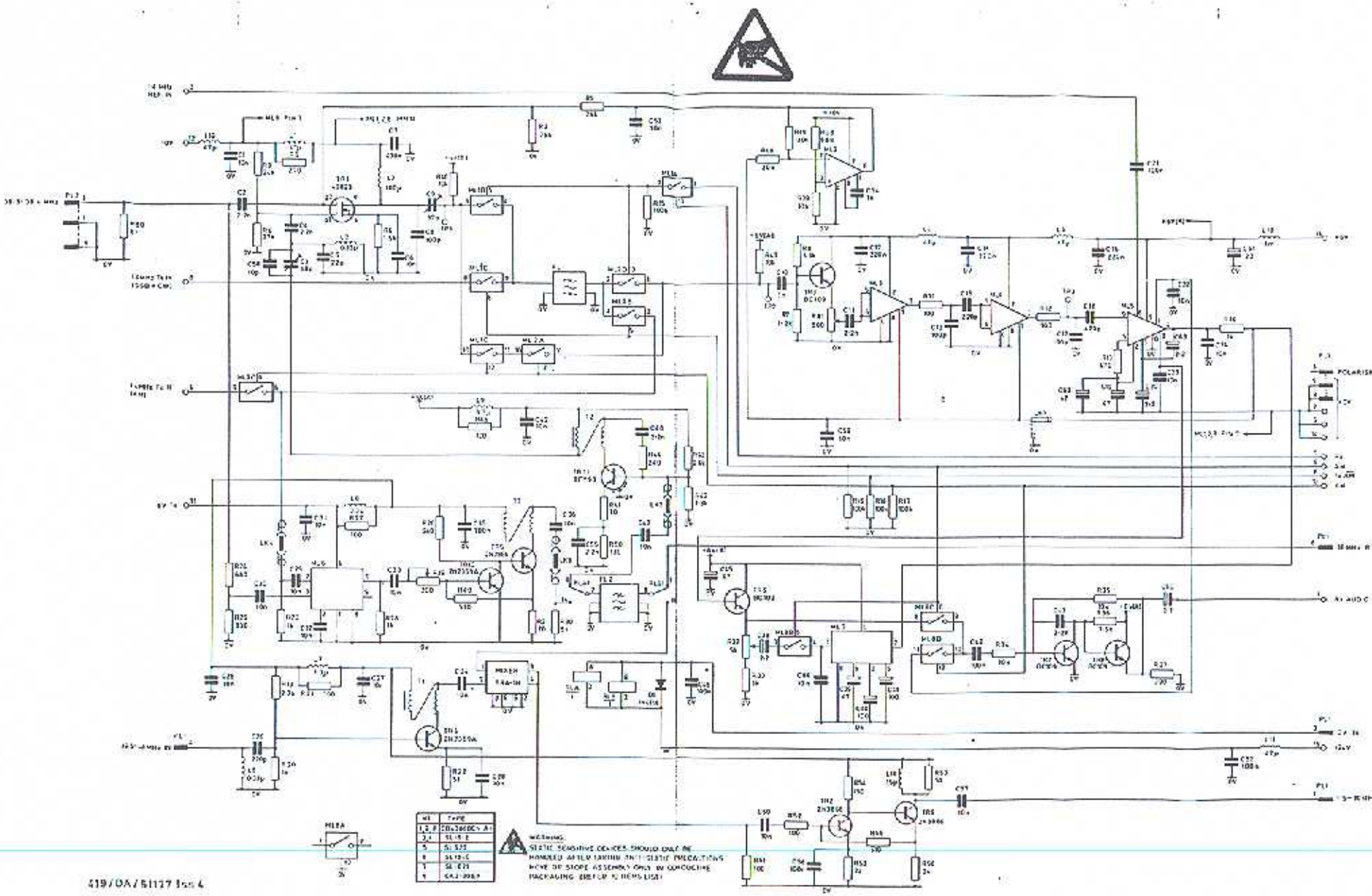

Fig 1 IF board circuit diagram

THIRD LINE SERVICING

OF

DISPLAY MODULE 630/1/39070

(DISPLAY BOARD 419/1/51210)

(DISPLAY DRIVER BOARD 419/1/51213)

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ILLUSTRATIONS

Fig.

1 Display board : circuit diagram
2 Display driver board : circuit diagram
3 Display board : component layout
4 Display driver board : component layout

TECHNICAL DESCRIPTION

Introduction

1. The Display Module comprises two printed circuit boards assembled together as a unit and interconnected by board mounted pins and sockets. One of the boards houses the decoding and display driver circuitry (419/1/51213), and the other board the seven-digit, seven-segment, visual display (419/1/51210).

2. The module receives address and data information on its inputs which enable successive digits in the display to be driven sequentially with the appropriate data. A strobe rate of approximately 250 Hz produces a normal bright display, and 100 Hz a dim display.

Circuit description

3. Circuit diagrams of the two boards forming the module are given in Figures 1 and 2. The circuits of the two boards are treated separately in the following description.

Display board (Figure 1)

4. The Display Board mounts seven 7-segment display units ML1 to ML7. Units ML1 to ML6 share a common seven-line bus from the driver board (board pins 9-15), which is used to energise the segments required to form each numerical digit of the frequency display. The digits forming the display are enabled sequentially over six address lines on board pins 16 to 21. Board pin 8 is used to illuminate the decimal point segment on unit ML2 thus providing a decimal display in megahertz.

5. Display unit ML7 is used to display a letter indicating the mode of ~~transmission~~ operation being used. The segments of this unit are brought out to board pins 1 to 7, and the unit is enabled over board pin 22.

Display driver board (Figure 2)

6. The incoming address lines, designated ADDRESS 1 to ADDRESS 6, are strobed high (logic 1) sequentially by an external control (eg. microprocessor) to enable each of the six display units on the Display Board in turn. As each unit of the display is enabled the relevant BCD bits representing the numeric digit to be displayed are presented at the data inputs to the board on PL1/2, 13, 1 and 14; designated DATA 0 to DATA 3 respectively. The BCD input is decoded at ML14 to form the seven-bit code required to drive the relevant segments of the display digit. This process is illustrated in Table 1. Decoder ML14 is enabled by the DISPLAY ENABLE input on PL1/7.

Table 1 - BCD to 7-segment numerical code

Data bits					Display segements						
D3	D2	D1	D0	Numerical	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	1	0	1	1	0	0	0	0
0	0	1	0	2	1	1	0	1	1	0	1
0	0	1	1	3	1	1	1	1	0	0	1
0	1	0	0	4	0	1	1	0	0	1	1
0	1	0	1	5	1	0	1	1	0	1	1
0	1	1	0	6	1	0	1	1	1	1	1
0	1	1	1	7	1	1	1	0	0	0	0
1	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	9	1	1	1	1	0	1	1

7. Only two BCD data bits are required to code the four transmission mode letters U, L, C, and A. The ADDRESS 1 input (PL1/12) enables the 10 MHz display digit and, as this digit will never be higher than numeric 2, only two bits (D0 and D1) are required on the data input lines; the other two bits (D2 and D3) are used to carry the mode bits. These are clocked into latch ML11 when the ADDRESS 1 line goes to logic 1. The two bit output of ML11 is processed by gates ML9A, ML10A, B, C and D and routed via driver ML12 and resistors ML13 to the seven input sockets (1 to 7) serving the mode display unit segments. Two of these outputs (sockets 5 and 6) are set continuously at +10V by ML12; these form the e and f segments which are illuminated for all four mode display letters. The other five outputs are set to complete the letter display required. The mode display digit (ML7) is enabled by the logic 1 condition on ML9D/11 when ADDRESS 2 input (PL1/3) goes high.

8. To prevent the mode data bits D2 and D3 corrupting the frequency data presented to the numeric display during an ADDRESS 1 input, AND gates ML9B and C are disabled by a complimentary ADDRESS 1 input (0V) on PL1/6.

9. When the LAMP TEST input on PL3/1 goes to logic 0, all the outputs of ML14 go to 0V to illuminate all seven segments on each of the six numerical display digits.

10. Power for the module is supplied from an externally mounted regulator connected to PL3/3. Capacitors C1 and C4 provide filtering for the regulator output, and potential divider R5/R6 provides the reference voltage for the regulator on PL3/2.

Testing

11. Testing information for the Display Module is given in Part 4 of this manual.

COMPONENTS LIST

12. The principal component parts of Display Module 630/1/39070 are Display Printed Circuit Board 419/1/51210 and Display Driver Board 419/1/51213.

13. The principal component parts of the two boards are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	DISPLAY BOARD		(419/1/51210)
ML1-ML7	Seven segment LED display	Hewlett Packard HDSP3733	520/4/97671/011
	DISPLAY DRIVER BOARD CAPACITORS		
C1,3	10 nF 20% 100V	Wima Type FKS2	435/4/90821/007
C2	100 nF 5% 100V	Siemens B32560-01104J	435/4/90137/014
C4	10 uF 10% 20V	CECC 30201-003	402/4/56272/100
	RESISTORS		
R1,2	100k 2% 0.25W	Metal oxide film	403/4/05525/100
R3	56k 2% 0.25W	Metal oxide film	403/4/05524/560
R4	300 ohm 2% 0.25W	Metal oxide film	403/4/05522/300
R5	150 ohm 2% 0.25W	Metal oxide film	403/4/05512/150
R6	1.1k 1% 0.25W	Metal oxide film	403/4/05510/110
	INTEGRATED CIRCUITS		
ML8	Transistor array	ULN2004ABU	445/9/03262
ML9	Quad 2-input AND gate	CD4081BCN	445/4/03234/081
ML10	Quad 2-input NORI gate	CD4001BCN	445/4/03234/001
ML11	Dual D-type flip-flop	CD4013BCN	445/4/03234/013

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
ML12	High current driver	UDN2984ABU	445/9/03266
ML13	Resistor network 7 x 100 ohm	Beckman 899-3-100R	403/4/04319/017
ML14	BCD to 7 segment decoder	CD4511BCN	445/4/03234/511
ML15	Resistor network 7 x 330 ohm	Beckman 899-3-330R	453/4/10976/331
ML16	Resistor network 5 x 220k ohm	Bourns 4306R-101-224	403/4/07113/001
	MISCELLANEOUS		
D1	Diode Volt. reg. 3V 0.4W	BZX79-C3V0	415/4/05830/003
TR1	Transistor N-P-N	BC109	417/4/02028/000
PL3 (Upper)	2-way Rt. angle	Berg 75168-109-02	508/4/22212/002
PL3 (Lower)	2-way Rt. angle	Berg 75168-103-02	508/4/22211/002

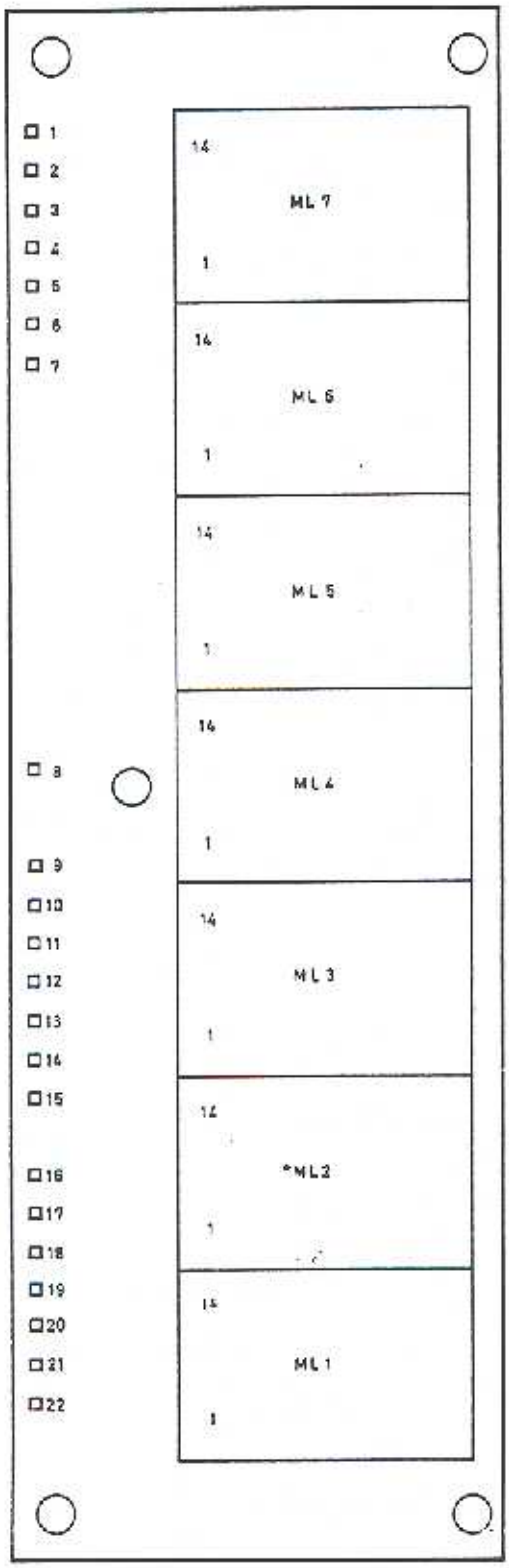


Fig 3 Display — component layout

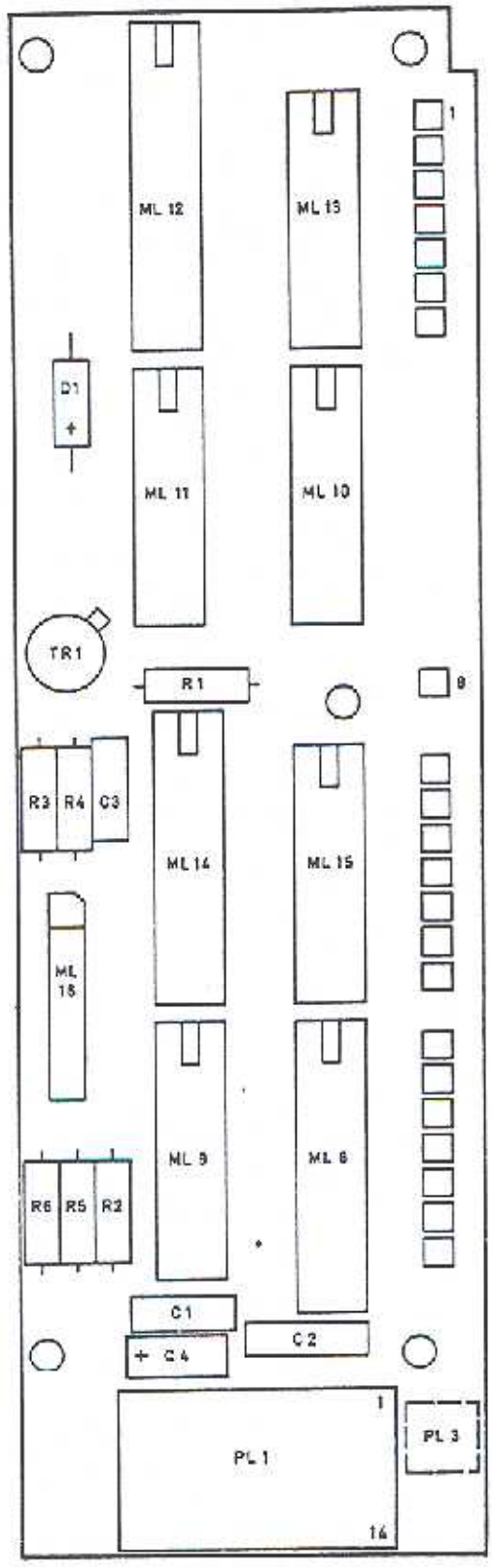
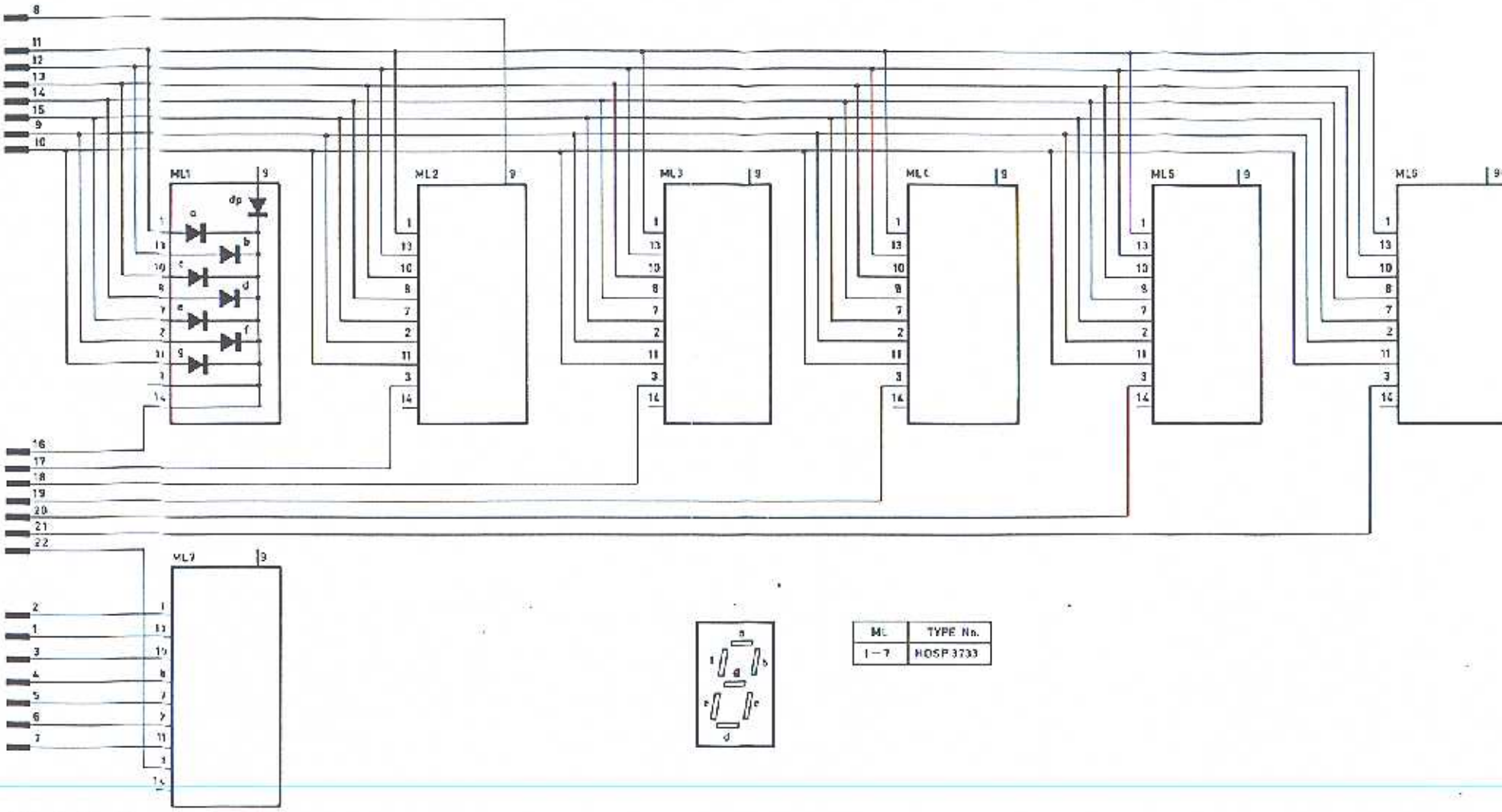


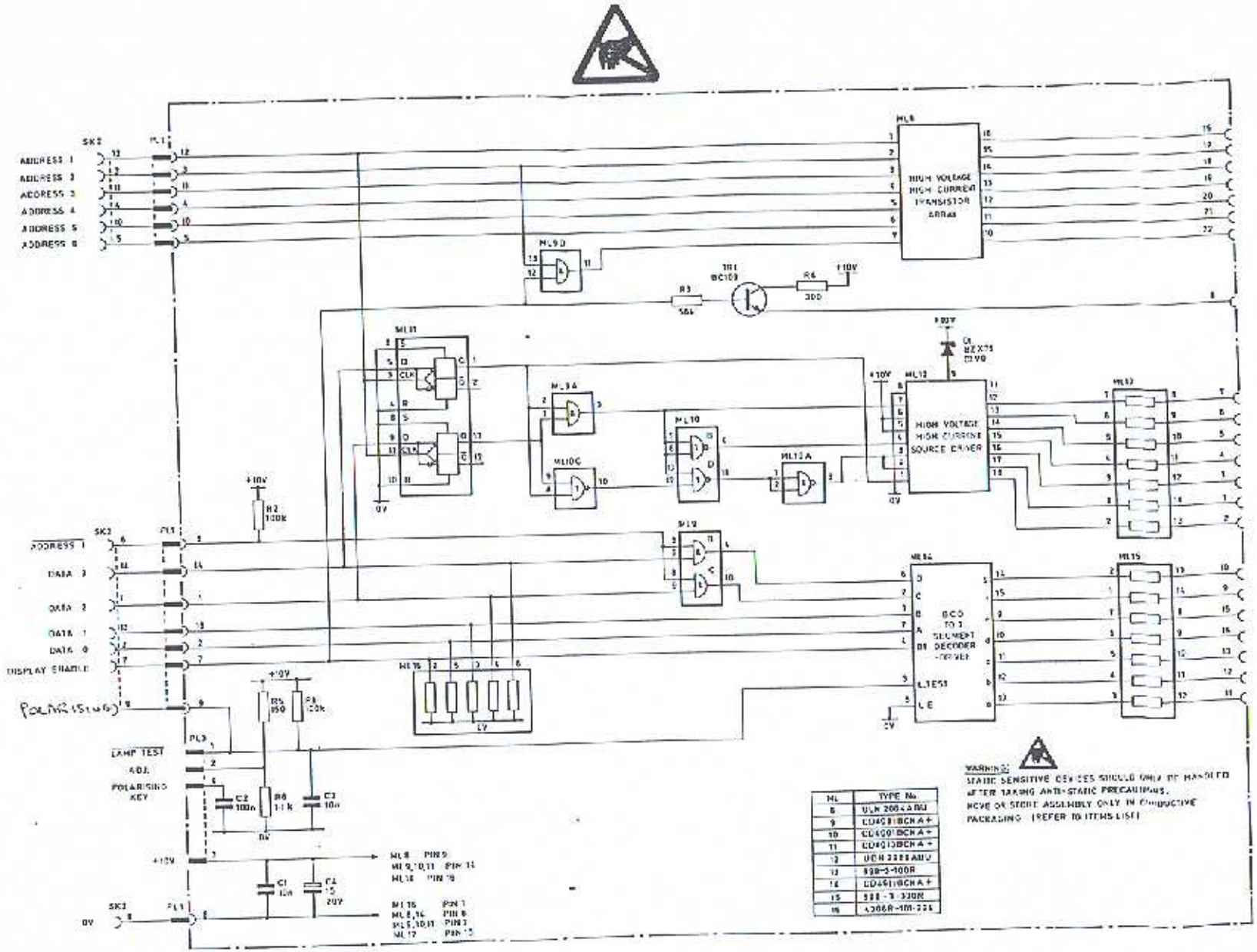
Fig 4 Display decode and drive board – component layout



ML	TYPE No.
1 – 7	HDSP 3733

619/DA/51210 Ins 1

Fig. 1 Display board : circuit diagram



ML	TYPE No.
8	ULN 2064A/BU
9	CD4081BCN A+
10	CD4001BCN A+
11	CD4013BCN A+
12	UCN 2283A/U
13	330-3-100R
14	CD4511BCN A+
15	330 - 3 - 330R
16	A266R-1M-224

419/DA/51213 Iss 3

Fig 2 Display driver board : circuit diagram

THIRD LINE SERVICING

OF

SYNTHESISER MODULE 630/1/38185

(SYNTHESISER BOARD 1 - 419/1/51216)

(SYNTHESISER BOARD 2 - 419/1/51219)

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TECHNICAL DESCRIPTION

INTRODUCTION

1. The Synthesiser module comprises two printed circuit boards designated Synthesiser Board 1 (419/1/51216), and Synthesiser Board 2 (419/1/51219) respectively. The two boards are assembled together as a unit, and are electrically connected by board mounted plugs and sockets as follows:

Board 1	Board 2
PL6 (12-way) mates with	SK8
PL7 (5-way) mates with	SK9

2. The Synthesiser module circuitry is disposed over the two boards as follows:

Board 2 (upper board in the module): On this board is mounted the control loop for the main Synthesiser (1st Local Oscillator) which produces an output frequency between 39.5 MHz and 68 MHz (fi + 38 MHz), and is adjustable in steps of 100 Hz. It is addressed by serial frequency control data from the micro- processor, which also determines which one of the two voltage controlled oscillators (VCO) on the lower board (Board 1), is to be selected. These digital loop components, loop filters, and phase comparators which are used in the main Synthesiser are also mounted on this board, together with the following control logic circuits:

(a) Warning tones selection and gating.

(b) Pressel control, including relay drive and delay.

(c) Reset pulse generator and ATU tune control.

(d) Mode decoder for Synthesiser and transmitted power level control.

(e) Battery voltage monitor.

(f) Receiver mute and VOGAD control.

(g) Transmitter inhibit.

Board 1 (lower board in the module): On this board is mounted a second local oscillator Synthesiser producing either 36.6 MHz or 39.4 MHz phase locked to a reference frequency and selected by data from the microprocessor received on Board 2. Board 1 also houses the following circuits:

(a) A crystal oscillator (5.6 MHz) from which are derived reference frequencies of 2.8 MHz, 1.4 MHz and 20 kHz.

(b) A voltage controlled crystal oscillator (6 MHz).

(c) Two VHF voltage controlled oscillators (VCO's) producing frequencies in the ranges 39.5 MHz to 52 MHz, and 52 MHz to 68 MHz respectively. An electronic switching circuit is provided to select one or other of the two VCO's.

(d) A monostable circuit for generating a pulse to initiate a 'poor VSWR' warning tone.

CIRCUIT DESCRIPTION

General

3. Circuit diagrams of Synthesiser Boards 1 and 2 are given in Figs.3 and 4 respectively. As far as is possible the circuits of the two boards are described separately to reduce the amount of cross-reference the reader has to make between Figures 3 and 4.

Board 1 : 2nd LO (Fig.3a/b)

4. The second local oscillator circuit (2nd LO) is mounted on this board, the block diagram in Figure 5 shows the functional relationships of the main components in the 2nd LO Synthesiser which has to generate a frequency of 36.6 MHz when the radio is using LSB or AM transmission; or a frequency of 39.4 MHz when using USB or CW transmission. The selection is determined by a logic 1 (high) condition from the control logic on Board 2 to either variable divider ML7/11 for LSB/AM, or ML7/13 for USB/CW. The output of the VCO (TR14) is divided by ten at ML6 and applied to the variable divider where it is divided by 183 (36.6 MHz) or 197 (39.4 MHz) to derive a 20 kHz loop frequency for the phase detector ML9. The phase detector compares this frequency with a 20 kHz reference frequency derived from the 5.6 MHz crystal oscillator TCXO1 via ML18 (divide by 2) and ML3 (divide by 140).

5. The output from the phase detector (ML9/13) is a high (1) level when the frequency derived from the VCO output is above the 20 kHz reference frequency, and at a low (0), level when the VCO derived frequency is below the reference frequency. Initially, when say the mode of operation is changed from LSB to USB, the frequency derived from the VCO will be considerably lower than 20 kHz (about 18.6 kHz) and the output from the phase detector ML9/13 will be low (0V). This is connected to the inverting input of the loop filter ML10/2, whose output (ML10/6) goes high. The voltage at the output of the phase filter is applied to varactor diode D13 which controls the frequency of the VCO (TR14); any increase in voltage from ML10 producing a proportional increase of the VCO output frequency, hence the full high on its output will produce a rapid rise in the VCO frequency. When the VCO frequency is close to the selected transmission frequency the output from phase detector (ML9) takes the form of pulses; negative going if the leading edge of the variable divider output

lags the leading edge of the reference frequency, and positive going for the opposite case. Loop filter ML9 now acts as an integrator to produce an analogue increase or decrease of the voltage on varactor D13. This causes an increase or decrease of the VCO frequency until phase lock is achieved at which point the output of the phase detector becomes in effect an open circuit. The charged voltage of D13 is then held with occasional 'topping-up' with a pulse or two from the phase detector when the VCO frequency falls due to any leakage of charge from D13 for instance. The output of the VCO is routed via a buffer amplifier stage TR13, TR15, and TR16, to board output PL3/4 (Refer to Fig.3b).

Board 1 : reference frequencies (Fig.3a)

6. Crystal oscillator TCXO1 produces a 5.6 MHz output at TXCO1/3 (Fig.3a) from which is derived various reference frequencies. Latches ML2A and ML2B form a quadrature divider to produce two 1.4 MEz outputs in phase quadrature (90° phase difference). These are routed from the board via pins PL2/3 and PL2/4, to the AM/AF/SSB Board.

7. The 5.6 MHz output from TCXO1 is also divided by two at ML1B to produce a 2.8 MHz reference for the main Synthesiser on Board 1, and for output to the microprocessor at PL2/2. The 2.8 MHz is also used to drive variable divider ML3 whose address is preset to produce a division by 140. The 20 kHz output from ML3/1 is used as the reference frequency for the 2nd LO phase detector described in para.4.

Board 1 : voltage controlled crystal oscillator (VCXO) (Fig.3b)

8. The 6 MHz crystal XTAL 1 with transistor TR17 and associated components form a voltage controlled oscillator, the frequency of which is variable about the mean 6 MHz and controlled by the magnitude of the voltage on the varactor diode D14. This voltage is dependent on the analogue voltage produced at the slow loop phase comparator output (ML24/8) of the main Synthesiser on Board 2.

Board 1 : VCO1 (39.5 MHz - 52 MHz) and VCO2 (52 MHz - 68 MHz)

9. The active device in VCO1 is transistor TR9; in VCO2 is transistor TR3. The VCO range required for the transmission frequency in use is selected by the logic level on PL6/7 from the MODE/VCO latch (ML22/6) on Board 2. A high on this line turns on transistor TR8 and TR11 to connect +10V to VCO1 (TR9). A low condition on the same line switches on transistor TR1 to connect the +10V supply to VCO2 (TR3). The frequency control voltage for oscillators VCO1 and VCO2 is applied to varactor diodes D12 or D11 respectively via PL6/6, resistors R41, R13, and then R20 or R16.

10. Transistor TR12 is switched on by a high on the VCO SELECT A input on PL6/9. When TR12 is turned on, resistor R44 is grounded and the control voltage presented to the varactor diodes (D11 and D12) is attenuated. Attenuation is switched into circuit at the lower end of the frequency ranges of both VCO1 and VCO2 as follows:

Transmission frequency (MHz)	VCO frequency (MEz)	VCO	Attenuator (IN/OUT)
1.5 - 7	39.5 - 45	1	IN
7 - 14	45 - 52	1	OUT
14 - 22	52 - 60	2	IN
22 - 30	60 - 68	2	OUT

11. Overall control of the attenuator is exercised by the programme of the associated microprocessor module in the radio. Attenuating the frequency control voltage at the lower end of the VCO ranges improves the loop gain performance of the Synthesiser, and produces a better overall signal to noise ratio at the output of the Synthesiser.

12. When the 2nd LO Synthesiser has achieved a phase lock. The phase detector ML9 generates a constant high on ML9/1. From here it is routed to the control logic on Board 2. (Fig.4b: ML32/1).

13. The D18, C95, R14 circuit ensures a minimum voltage of about 1.1V is maintained at the varactor diodes, and also provides some protection against fluctuations on the +6V supply line.

Board 1 : miscellaneous (Fig.3a)

14. Monostable ML8 is positive edge triggered when the output condition from a VSWR detector mounted elsewhere in the radio is between 10.5 and 14.5 volts. It generates a negative going pulse of approximately 200 milliseconds when triggered; this masks any rapid fluctuations which would be produced by a poor VSWR in an SSB mode creating a changing state between 'acceptable' and 'poor' due to the RF power output following the speech waveform. The low from ML8 is connected via PL3/3 to the control logic on Board 2 to switch on a 250 Hz tone giving audible warning of a poor VSWR. When the radio is in the Rx mode, or during a TUNE sequence a logic 1 condition on PL3/2 (from Board 2 PL1/13) holds ML8 in the reset condition and thus inhibits initiation of the VSWR warning tone.

Board 2 : main synthesiser (Fig.4a)

15. The block diagram of Fig.6 illustrates the relationship of the principal components in the main Synthesiser circuit. The output (fo) from the main Synthesiser VCO on Board 1 is the transmission frequency + the IF frequency of 38 MHz. This VCO output is connected as an input to the two phase locked loops on Board 1 via buffer amplifier TR7.

16. Consider first the operation of one of these loops; the FAST LOOP in Fig.6. Phase comparator ML19/9 is supplied with a reference frequency of approximately 3 MHz derived from the 6 MHz output of VCXO by latch ML18A (divide by 2). This 3 MHz reference frequency is subjected to further division inside the device to produce a basic reference frequency of approximately 10 kHz. The input from the VCO is divided by 10 or 11 in the prescaler ML27, further divided in the programmed universal divider ML14, to produce a frequency close to 10 kHz which is applied to phase comparator ML19/14. The phase comparator operates in similar fashion to that of the 2nd LO Synthesiser described in para.4; the output is integrated in loop filter ML12 and the analogue voltage out of the filter (ML12/6) is used to control the frequency of the VCO in use (para.9).

17. The division ratio of prescaler ML27 is controlled by inputs PE1 and PE2; the device will divide by ten when either input is high, and by eleven when both inputs are low. The divide by 10/11 stage extends the range of variable division to permit unit steps, instead of minimum steps of ten, in the divider ratios. This is achieved by varying the ratio between divide by 10 and divide by 11 in a regular manner during each output cycle of the divider chain, the control being derived from the universal divider (ML14) as logic levels. The

change from divide by 10 to divide by 11 once in an output cycle for one count of eleven, implies that one more input count is required to achieve the same output cycle length. In this way the division ratio is increased by a unit step, and by causing the change to occur a number of times during a single output cycle, the appropriate units figure may be selected.

18. The action of the fast loop may be described as a coarse tuning of the VCO to within 10 kHz of the wanted output frequency.

19. The SLOW LOOP acts in a similar manner to the fast loop. The reference frequency of 2.8 MHz (from Fig.5) is further divided in phase comparator ML24, to obtain a 10 kHz reference frequency. The VCO output frequency is routed through prescaler ML26 to the two universal dividers ML15 and ML23. Divider ML15 operates like the universal divider (ML14) in the fast loop, but an additional decade of division is applied. In the locked condition this produces an output of 1 kHz on ML15/25. This signal is applied to the strobe input of the sample and hold phase comparator ML24, where it is compared with the 10 kHz reference frequency, to produce an analogue output (3.5V to 5.5V) at ML24/8. Using ML23 in cascade with ML15 extends the division ratio by a further decade as follows.

20. Setting a unit step on ML23 will cause the division ratio of ML26/ML15 to rise by 'one' in one output cycle only, in every ten complete output cycles of ML15. In this way the 'average' division ratio has been raised by a fractional amount of one tenth. As an example, if the divider ratio of ML26/ML15 is 39500, the output frequency when this ratio is increased by one tenth would be 39500.1 x 1 kHz = 39.5001 MHz, an extra step of 100 Hz. Setting steps in the range 0-9 on ML23 will select the addition of 0 to 900 Hz in 100 Hz steps.

21. The action of the phase comparator (ML24) and the loop filter (ML12) causes the analogue voltage to be 'averaged' to the correct value to control the frequency generated by the nominal 6 MHz VCXO on Board 1 (see para.8) and hence varies the reference frequency used in the FAST LOOP. The overall effect is to 'fine tune' the VCO to within $\pm$ 1 Hz of the selected transmission frequency. The overall range of division is from 39500.0 to 67999.9 for 39.5000 MHz to 67.9999 MHz respectively.

22. Once the Synthesiser has achieved a phase lock, ML24/4 is maintained at logic 0. If the phase comparator in ML24 detects a phase difference for whatever reason (eg. change of channel and frequency) this output goes high as an out of lock signal to the control logic of Fig.4b (ML28/13).

23. If the FAST LOOP is unlocked by a change of 10 kHz or more, the phase comparator (ML19) puts out a low condition (0V) on ML19/12 to initiate a tune sequence via the control logic (ML39/11) on Fig.4b.

24. The divisor of the universal dividers is determined by the four data bits from the microprocessor control on PL4/1, 2, 6 and 7. The programme information is presented to the address lines A0 to A3 of the dividers via AND/OR gates ML16, ML17, and ML21.

Board 2 : universal dividers (Fig.4a)

25. The AND/OR gates ML16, ML17, and ML21 provide a data management stage, directing the incoming data stream from the microprocessor control to relevant dividers. The incoming data is connected to the 'B' inputs to these gates and

is only switched through to the 'D' outputs when input KB is high. This in turn is controlled by the count reached in the associated universal dividers.

26. The division ratio to obtain the transmission frequency required is selected by the programme presented to the dividers ML14, ML15, and ML23. The programme is in series/parallel form, defining one decimal digit at a time on the 4 data lines PLA/2, 7, 1 and 6. A double sequence is employed in the programme; first ML14 and ML15 are addressed together, and then ML23 is addressed.

27. During the first sequence, the PE2 input on PL4/9 goes to logic 1 and programme clock (PC) pulses appear on PL4/5. Successive rising edges of PC select each internal latch of the divider to be filled in the sequence illustrated in Figure 1. The data on the bus is latched in by the following falling edge of PC.

28. The relevant 8's, 4's, 2's, or 1's digit is marked by a logic 0. For example, if the selected frequency was 12.481 MHz the data latched into ML14 and ML15 would be as follows:

Clock Pulse	ML14 Pin No. 1	2	3	4		ML15 Pin No. 1	2	3	4	
1	1	1	1	0		0	1	0	1	
2	1	1	1	1		1	1	1	1	
3	1	1	1	1		1	1	1	0	(1 x 1 kHz)
4	0	1	1	1	(8 x 10 kHz)	0	1	1	1	
5	1	0	1	1	(4 x 100 kHz)	1	0	1	1	
6	1	1	0	1	(2 x 1 MHz)	1	1	0	1	
7	1	1	1	0	(1 x 10 MHz)	1	1	1	0	
8	1	1	1	0		1	1	1	0	

29. The first sequence ends with PE2 going to logic 0, and the second sequence commences when PE3 goes to logic 1 and ML23 is programmed as illustrated in Figure 2. Note that the only variable data loaded in is the number of 100 Hz steps.

30. As each latch in the dividers is addressed during the two sequences just described, a logic 0 condition appears on the relevant divider pins 5 to 11 as follows:

CLOCK PULSE	1	2	3	4	5	6	7	8
ML14, 15, or 23 Pin No.	5	-	11	10	9	8	7	6

At all other times these pins are at logic 1, except for pin 5 which goes to, and remains at, logic 0 when the sequence has ended.

Board 2 : miscellaneous

31. Capacitor C128 is the HOLD capacitor for the sample and hold circuit of frequency Synthesiser ML24, and capacitor C127 with R145 set the gain of the internal comparator of that device.

Board 2 : control logic (Fig.4b)

32. Logic levels are marked against devices shown in the main circuit diagram Fig.4b. These indicate the levels existing when operating AM transmissions on full power (HP), and when the radio is in the Rx mode (pressel not operated).

33. The conditions indicated by the various warning tones provided by the module are:

TONE	INDICATION
1 kHz (continuous)	Call or ATU tuning
1 kHz (keyed by pressel)	CW sidetone
250 Hz (continuous)	Poor VSWR on Tx (keydown) or External ATU fault
250 Hz (interrupted at 1.4 Hz)	Low battery/supply voltage
1 kHz/250 Hz (alternating at 1.4 Hz rate)	Synthesiser out of lock

34. The inputs to, and outputs from the control logic on the Synthesiser Board 2 are given in Table 1.

Table 1 - Control logic : inputs and outputs

Designation	Connector	Indication
Inputs		
EXT.ATU FAULT	PL10/12	Fault = 1
INT/EXT.ATU READY	PL10/3:PL10/11	Ready = 1
EXT.ATU PRESENT	PL10/5	Present = 1
VSWR	PL1/21	VSWR GT 3:1 = 0
CALL	PL1/9:PL1/22	Call tone required = 1
IC	PL1/8	Intercom required = 1
HP (Power)	PL1/7	HP = 0, LP = 1
PA PRESENT I/P	PL1/4	Present = 1
PRESSEL	PL10/10:PL1/12	Pressel operated = 0V
Outputs		
TRANSMIT (Tx)	PL1/19	Tx = 1
TRANSMIT (Tx DELAYED)	PL1/6	(Tx = 1 held for 0.25-0.75 secs. (after release of key on CW
RELAY DRIVE	PL1/5:PL1/16	0V for Tx: delayed for CW
RELAY DRIVE (NOT TUNE)	PL1/14	0V for Tx: delayed for CW except during ATU tune
Rx/Tx INDICATION	PL1/3	Tx = 0
TUNE	PL1/10	ATU tune commence = 0
CW/USB	SK9/3	CW/USB = 1 for either CW or USB
LSB/AM	SK9/2	LSB/AM = 1 for either LSB or AM
$\overline{AM}$	PL10/9	$\overline{AM}$ = 0 for AM only
Rx MUTE	PL1/20	Mute = 0 (when IC = 1)
+6V VOGAD	PL10/2	Supplies VOGAD w/+6V when IC = 1 or $\overline{CW}$ Tx = 1
POWER (HP)	PL1/18	HP = 1, LP = 0 (output to Module 11)

continued ...

Table 1 continued ...

Designation	Connector	Indication
1 kHz CW	PL1/11	1 kHz selected for Tx = 1. CW = 1 when pressl is operated or ATU tune in progress
RESET	PL1/17	RESET = 1 for 10 milliseconds min. if fast loop loses lock
RESET (EXT)	PL1/15	RESET = LOW
Rx + TUNE	PL1/13	At logic 1 when in Rx mode or during tune sequence. Inhibits initiation of VSWR warning tone.

Pressel

35. Operation of pressel puts low volt condition (OV) on the incoming pressel lead, switching off TR24 making one input of ML29B and ML43B high. ML43B output goes high making ML30B output low switching on TR26 and connecting the +6V supply (via PL10/2), to the VOGAD on the AF/AM/SSB board (unless 'CW' mode has been selected when ML43B is inhibited by a low on pin 5); also, with both inputs at 1, ML29B output goes low enabling the fault tone activate gate ML28C/9, and changing the output state of ML37A to generate a Tx = 1 output on PL1/19.

External ATU fault

36 When an external ATU is connected a logic 1 condition is incoming on PL10/5 and as long as no fault condition is signalled from the ATU on PL10/12 (ie. disconnection, or logic 1 state), ML28B/6 is held at logic 0. But if a fault condition is signalled ML26B/6 goes to logic 1 and its output goes low; this low enables ML28C/8 so that when the pressel is next operated ML28C output goes to logic 1 and switches the 3-input, 250 Hz activate gate (ML42B/6) to logic 0. This is connected to the A1 input of channel selector ML34 to switch D1 (250 Hz) through to the WARNING TONES output PL1/1.

VSWR fault

37. IF the VSWR is worse than 3:1 a logic 0 condition is connected via input PL1/21 to gate input ML28A/2. The output of ML28A goes to logic 0 causing the output of ML28B and input ML28C/8 to follow. When the pressel is next operated and the other input to ML28C/(9) goes tp 0, ML28C/10 output goes to logic 1 and activates the 250 Hz gate ML42B to make ML34/A1 low (0) which connects 250 Hz to the warning tone output.

Battery voltage monitor

38. The +24V supply to the board enters via PL10/1 (Fig.4a) and is connected to a voltage monitor circuit via resistor R111 (Fig.4b). The monitor circuit comprises transistors TR21 and TR22 and their associated components which act as a Schmitt trigger level detector. When the supply voltage is normal TR22 base is held at +12V by the regulator diode D22. When the supply voltage falls below +18V, D22 is no longer conducting and TR22 base is at approximately +9.4V; TR22 is turned on and its collector goes to logic 1. With one output high, the output of the 250 Hz activate gate ML42B/6 puts a logic 0 on address A1 of channel selector ML34, and the 250 Hz tone is connected to the WARNING TONE output (PL1/1). The logic 1 from the monitor circuit is also

connected to ML33B/5 and the output of this gate goes low, enabling the 1.4 Hz oscillator formed by ML33A, and ML32B, C, and D. The 1.4 Hz square wave on the A0 address of selector ML34, switches the 250 Hz tone on and off to give audible warning of a low supply voltage.

Synthesiser out of lock

39. Provided that the main Synthesiser (Fig.4a ML24/4) and the 2nd LO Synthesiser (Fig.3b ML9/1) have achieved phase lock both inputs to gate ML28D are kept at logic 0. If either or both go out of lock, ML28D/11 will change state to logic 0, triggering a 125 millisecond logic 0 pulse from $\overline{Q}$ of monostable ML44A/7, and making the output of ML29C/10 high. This high output is maintained on the output of ML29C for a minimum duration of 125 milliseconds by the logic 0 pulse from $\overline{Q}$. This ensures that any marginal out of lock condition does not corrupt the quality of the out of lock warning tone.

40. The high on ML29C/10; (a) changes the output states of ML33C/10 and ML11C/10 to make ML34/13 (A2) high; (b) changes the output state of ML42B/6 to make ML34/12 (A1) low; and (c) changes the output state of ML33B to switch on the 1.4 Hz generator supply to ML34/11 (A0). These conditions on the address lines to ML34 produce a warning tone alternating between 250 Hz and 1 kHz every 700 millisecond.

Call

41. If a CALL input (PL1/9 or PL1/22) goes high, the output of ML30C/10 goes low, and after inversion at ML31D, changes one input of the 1 kHz activate gate ML33C. This initiates an A2 (1 kHz) address to ML34B to produce a 1 kHz call tone at the WARNING TONES output PL1/1. A CALL signal on PL1/22 also makes ML42/9 low to disable ML29B and inhibit the Tx=1 signal when the pressel is operated.

Tune

42. The output of phase comparator ML19/12 (Fig.4a) goes low if a frequency shift of 10 kHz or more is detected. This triggers monostable ML39B/11 (Fig. 4b) to produce a 40 millisecond RESET pulse from Q on output PL1/17; this is used to reset the external control (eg. microprocessor). The complimentary low on $\overline{Q}$ of ML39B sets latch ML40A/13 low, and this is passed via ML35C, ML38C, and ML40C to produce a high on latch ML40B/9 which

(a) turns on transistor TR23 which simulates operation of the pressel and turns off TR24 producing a high on the output of ML37A. This leaves the board as the Tx signal on PL1/19, and also enables the continuous 1 kHz gate ML36C for the 1 kHz CW output on PL1/11.

(b) changes the output state of ML35A/3 to low to override any HP selection on PL1/7 and ensure tuning is carried out on low power.

(c) disables the VSWR fault gate ML28A/1.

(d) is inverted at ML38B to send a low on the TUNE = 0 output on PL1/10.

Mode logic and CW delay (Fig.7)

43. The two data bits carrying the mode selection information are latched into ML22 by the positive edge of a VCO/MODE LATCH ENABLE signal on PL4/8

(Fig.4a). The two bits, designated A and B in the circuit, are routed from the latch into the logic control circuitry (Fig.4b). The logic elements associated with mode selection have been extracted from Fig.4b to form Fig.7; the table in Fig.7 shows the mode selection code.

44. A feature of this part of the logic circuit is the Tx DELAY signal when operating on CW. The logic levels marked on Fig.4b are true when CW has been signalled on the A and B connections and before operation of the signalling key (pressel) for a mark, and provided a TUNE sequence has not been initiated. The selection of CW has enabled NAND gate ML37D with a high on pin 13. When the pressel (signalling key) is operated the change of state at the output of ML37D will gate the 1 kHz continuous tone through ML36C to provide a 1 kHz CW output at PL1/11. When the key is operated it also triggers monostable ML39A and $\overline{Q}$ goes low for the duration of its time out period (0.5 seconds approx.). The relay drive is activated for this period so that under normal CW operating conditions the relays will not be released during spaces in the keying (eg. morse or FSK signalling). This prevents the various Tx/Rx relays in the radio from attempting to follow the mark-space sequence in the signalling.

45. A TUNE condition on ML37C/9 will inhibit this gate and cancel the external RELAY DRIVE (NOT TUNE) during a tune sequence. The TUNE condition on ML35D/13 enables the 1 kHz tone used for modulation during a tune sequence.

Low power (LP)/high power (HP) selection

46. The signal to the power amplifier stage of the radio to indicate selection of low or high power working is routed through the Synthesiser control logic so that a HP selection can be overridden when a tune sequence is in progress, or when an external 100W power amplifier (PA) is connected to the radio. Operation of the HP override has been described in para.42. When an external PA is connected PL1/4 is marked high, and ML33D/11 goes low to produce a low on output PL1/18 (HP = 1).

Intercom (IC)

47. When the radio intercom circuit is being used PL1/8 goes high. This

(a) changes the output state of ML30B to a low; TR26 is turned on to connect +6V to the VOGAD via PL10/2.

(b) is inverted by ML31C to put a low on PL1/20 which is used to mute received signals in the radio.

(c) changes the output state of ML35B to low, which, at ML29B/5 inhibits the Tx = 1 signal (PL1/19) when the pressel is operated (ie. ML29B is disabled). This ensures antenna transmission does not take place during intercom.

ATU tune control

48. The following sequence occurs if the operating frequency changes by more than 10 kHz:

(a) Phase pulses from fast loop of Synthesiser set latch ML39B/11, and a reset is output to Module 5 on PL1/17, or an external unit on PL1/15. A READY = 0 is returned on PL10/3 from Module 5, or PL10/11 from an external unit.

(b) When next the pressel is operated (even momentarily) the control logic overrides other instructions and selects the following operating modes:

(i) CW

(ii) Low power

(iii) Transmit

(iv) ATU tune

(c) This condition is held until a 'READY' input is received (PL10/3 or 11).

(d) Pressel operation is then normal Tx/Rx until phase pulses are again received from the fast loop.

Transmitter inhibit

49. The Tx output (PL1/19) is held at logic 0 under the following conditions:

(a) Phase lock not achieved by Synthesiser.

(b) During intercom (IC).

TESTING AND ALIGNMENT

50. Testing and alignment information for this module is given in Part 4 of this manual.

COMPONENTS LIST

51. The principal components of the Synthesiser module are Synthesiser Board 1 (419/1/51226) and Synthesiser Board 2 (419/1/51219).

52. The principal component parts on the two boards are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
BOARD 1			419/1/51216
	CAPACITORS		
C1,2, 4-7, 12,14, 16-22, 24,25 30,31, 33-36, 40,42, 46-48, 50,60, 63 67,68, 80 83,87, 90 100, 142, 143	2.2nF		435/4/90821/012
C3,73, 92	Electrolytic - solid, 68uF 20% 16V		402/4/55746/018
C8,29, 44,51, 53-55, 57,66, 76,95	10nF 5% 63V	Wima Mk S2 or Arcotronics 1-68	435/4/90829/023
C9,28	10pF 2% 100V	Mullard 632-10129	400/4/20674/010
C10,27, 86	47pF 2% 100V	Mullard 632-34479	400/4/20674/018
C11,13, 26,45, 61	2.2pF 100V	Mullard 632-09228	400/4/20674/002
C15,85	100pF 2% 100V	Mullard 632-34101	400/4/20674/022
C37	1nF		435/4/90821/011
C38	220nF 5% 100V	Siemens 32561-B1224J	435/4/90827/001
C39,52, 64,89	2.2uF 10% 20V	CECC 30201-001	402/4/56311/220
C41	22pF 5% 400V	ITT 454-49-400-22-1PF	438/4/25904/009
C43	3.9pF	Mullard 632-09398	400/4/20674/005
C56,97	100nF 10% 50V	Wima Mk S2	435/4/90829/027
C75,78, 81	68nF 10% 63V	Wima Mk S2	435/4/90829/015
C77	82pF 2% 100V	Mullard 632-34829	400/4/20674/021
C82	22uF 10% 16V	CECC 30201-003	402/4/56132/220
C84,88	22nF 10% 63V	Wima Mk 52	435/4/90829/012
C96	22pF 2% 100V	Mullard 632-34229	400/4/20674/014
C98,99	68uF 20% 10V	BS9073 F002 or F005	402/4/55745/018
C144	1.5uF 10% 16V	ITT TAH	402/4/56131/150

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	RESISTORS		
R1	27 ohms 2% 0.25W	Metal oxide film	403/4/05521/270
R2,4,89	68 ohms 2% 0.25W	Metal oxide film	403/4/05521/680
R3,48, 52	47k 2% 0.125W	Metal oxide film	403/4/07181/473
R5,16	68k 2% 0.25W	Metal oxide film	403/4/05524/680
R6,20, 35,76, 81	470 ohms 2% 0.125W	Metal oxide film	403/4/07181/471
R7,21, 50,59, 74,79, 83	39k 2% 0.125W	Metal oxide film	403/4/07181/393
R8,22, 60	56k 2% 0.125W	Metal oxide film	403/4/07181/563
R9,23, 40,45, 61,65, 207	10k 2% 0.125W	Metal oxide film	403/4/07181/103
R10,55	20 ohms 2% 0.125W	Metal oxide film	403/4/07181/200
R11,27, 34	82 ohms 2% 0.125W	Metal oxide film	403/4/07181/820
R12,25, 64	1k 2% 0.125W	Metal oxide film	403/4/07181/102
R13	15k 2% 0.125W	Metal oxide film	403/4/07181/153
R14,56	3.9k 2% 0.125W	Metal oxide film	403/4/07181/392
R15,19, 39,41, 44,46, 63,86, 94,208	8.2k 2% 0.125W	Metal oxide film	403/4/07181/822
R17,18, 57,201	100k 2% 0.125W	Metal oxide film	403/4/07181/104
R24	39 ohms 2% 0.125W	Metal oxide film	403/4/07181/390
R26,28, 29	390 ohms 2% 0.125W	Metal oxide film	403/4/07181/391
R30,31, 68,72, 206, 209	270 ohms 2% 0.125W	Metal oxide film	403/4/07181/271
R32,99	2.7k 2% 0.125W	Metal oxide film	403/4/07181/272
R33,71	3.3k 2% 0.125W	Metal oxide film	403/4/07181/332
R42,69	47 ohms 2% 0.125W	Metal oxide film	403/4/07181/470
R43	180 ohms 2% 0.125W	Metal oxide film	403/4/07181/181
R47	22 ohms 2% 0.125W	Metal oxide film	403/4/07181/220
R51,75, 78	4.7k 2% 0.125W	Metal oxide film	403/4/07181/172
R53	36k 2% 0.25W	Metal oxide film	403/4/05524/360
R54,58	20k 2% 0.125W	Metal oxide film	403/4/07181/203

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R62,211	220 ohms 2% 0.125W	Metal oxide film	403/4/07181/221
R66,90,	68 ohms 2% 0.125W	Metal oxide film	403/4/07181/680
97,98,			
R67	560 ohms 2% 0.125W	Metal oxide film	403/4/07181/561
R70	16 ohms 2% 0.125W	Metal oxide film	403/4/07181/161
R73,204	27 ohms 2% 0.125W	Metal oxide film	403/4/07181/270
R77	120k 2% 0.125W	Metal oxide film	403/4/07181/124
R80	5.6k 2% 0.125W	Metal oxide film	403/4/07181/562
R82,96	150k 2% 0.125W	Metal oxide film	403/4/07181/154
R84	82k 2% 0.125W	Metal oxide film	403/4/07181/823
R85	820k 5% 0.33W	Metal film	403/4/07177/820
R88	12k 2% 0.25W	Metal oxide film	403/4/05524/120
R91,213	220k 2% 0.25W	Metal oxide film	403/4/05525/220
R92	330 ohms 2% 0.25W	Metal oxide film	403/4/05522/330
R93	22k 2% 0.25W	Metal oxide film	403/4/05524/220
R95	820 ohms 2% 0.125W	Metal oxide film	403/4/07181/821
R200	Variable pot., 5k 10% 0.5W	Non-wirewound	404/9/05032/005
R202, 203	10 ohms 2% 0.125W	Metal oxide film	403/4/07181/100
R210	100 ohms 2% 0.125W	Metal oxide film	403/4/07181/101
R212	560k 2% 0.25W	Metal oxide film	403/4/05525/560
	DIODES		
D1,18	75V rev. max. IF (AV) 0.075A	IN4148	415/4/98869
D11	Varactor 68pF/4V	Ferranti ZC712	415/4/05833/013
D12	Varactor 100pF/4V 30V VRM	Ferranti ZC714	415/4/05833/015
D13,14	Varactor 18pF/4V 30V VRM	Ferranti ZC705	415/4/05833/006
	TRANSISTORS		
TR1,11	P-N-P	BCY71	417/4/01721/002
TR3,9, 14*	FET	BFR84	417/4/04370
TR4-7, 13,15, 16,20	N-P-N	Texas BF357K	417/4/02162
TR8,12, 19	N-P-N	BC109C	417/4/02028/009
TR17,18	N-P-N	2N2369A	417/4/01881/001
	INTEGRATED CIRCUITS		
ML1,2*	Dual D-type flip-flop	HEF40138D	445/4/03272/013
ML3,7*	Dual prog. BCD/binary counter	Motorola MC14569BCPD	445/4/10806/569

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
ML6	Prescaler divider (divide by 10)	Plessey SP8660A	445/4/03155/004
ML8*	Mono/Astable multi-vibrator	National CD4047BCN-A	445/4/03234/047
ML9*	Phase locked loop	National CD4046BCN-A	445/4/03234/046
ML10*	Operational amplifier	RCA CA3130EX	445/4/03193/003
	MISCELLANEOUS		
XTAL1	Quartz crystal 6.0040 MHz		428/9/05034
TCXO1	RF oscillator 5.6 MHz	OSC87-22	612/9/42981
T1	Transformer RF		405/1/14486
T2,3,4	Transformer RF		405/1/14464
L1,3,8, 14,15	Inductor RF, 47uH 10%	BS9751 N0001 Patt. A	406/4/32161/033
L2,11	Inductor RF, 100uH 10%	BS9751 N0001 Patt. A	406/4/32161/037
L4	Inductor RF		406/1/32236/003
L5	Inductor RF		406/1/32236/002
L6	Inductor RF		406/1/32236/001
L10	Inductor RF, 56-82uH 10%	Cambion 558-1192-18-00-00	406/4/31754/018
L16	Inductor RF, 0.39-0.56uH	Cambion 558-1192-05-00-00	406/4/31751/005
L17	Inductor RF	Mullard FX4001 Bead	905/4/11801/001
BOARD 2			419/1/51219
	CAPACITORS		
C101, 106	47uF 10% 6V	CECC 30201-003/016 PT E	402/4/56122/470
C102	2.2nF 10% 100V	Mullard 630-18-222	400/4/21414/014
C103	6.8uF 10% 35V		402/4/56321/680
C104, 108, 109, 128, 135, 136, 138	10nF 5% 63V	Wima Mk S2	435/4/90829/023
C105, 137	220nF 5% 100V	Siemens B32561-B1224-J	435/4/90827/001
C107	10uF 10% 20V	CECC 30201-003/016 PT D	402/4/56272/100
C110	22nF 5% 63V	Wima Mk S2	435/4/90829/012
C111, 118, 130, 139, 141	2.2nF 5% 100V	Wima FKS2	435/4/90821/003
C112	18pF 2% 100V	Mullard 632-10189	400/4/20674/013

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C113, 127, 132	68nF 5% 63V	Wima Mk S2	435/4/90829/015
C114	220pF 2% 100V	Mullard 632-58221	400/4/20674/026
C115, 131	470nF 5% 100V	Siemens B32561-D1474J	435/4/90827/003
C116, 117, 119	100nF 10% 50V	Wima Mk S2	435/4/90829/027
C120	22uF 10% 16V	CECC 30201-003/016 PT E	402/4/56132/220
C121	5.6pF 100V	Mullard 632-09568	400/4/20674/007
C122-125	12pF 2% 100V	Mullard 632-10129	400/4/20674/011
C126	4.7nF 5% 100V	Wima FSK2	435/4/90821/005
C129	100pF 2% 100V	Mullard 632-34101	400/4/20674/022
C133, 134	390pF 15% 100V	Mullard 630-02391	400/4/19430/008
C140	10nF 10% 100V		400/4/20673/002
	RESISTORS		
R101	5.6k 2% 0.125W	Metal oxide film	403/4/07181/562
R102	68k 2% 0.125W	Metal oxide film	403/4/05521/680
R103	10 ohms 2% 0.125W	Metal oxide film	403/4/07181/100
R104	68 ohms 2% 0.125W	Metal oxide film	403/4/07081/680
R105, 114	10k 2% 0.125W	Metal oxide film	403/4/07181/103
R106, 113, 146	3.6k 2% 0.125W	Metal oxide film	403/4/07181/362
R107, 118	27k 2% 0.125W	Metal oxide film	403/4/07181/273
R108, 139	47k 2% 0.125W	Metal oxide film	403/4/07181/473
R109, 112, 122,	220k 2% 0.15W	Metal oxide film	403/4/05525/220
R110, 119, 120	22k 2% 0.125W	Metal oxide film	403/4/07181/223
R111, 141, 142	20k 2% 0.125W	Metal oxide film	403/4/07181/203
R115, 116	27 ohms 2% 0.125W	Metal oxide film	403/4/07181/270
R117	120k 2% 0.125W	Metal oxide film	403/4/07181/120
R121, 149	150k 2% 0.125W	Metal oxide film	403/4/07181/154
R123, 154	2.2k 2% 0.125W	Metal oxide film	403/4/07181/222

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R124	470k 2% 0.25W	Metal oxide film	403/4/07149/470
R126	56k 2% 0.125W	Metal oxide film	403/4/07181/563
R127, 164	5.6M 5% 0.25W	Metal oxide film	403/4/07118/010
R128	560k 2% 0.25W	Metal oxide film	403/4/07149/560
R129, 161, 162	820 ohms 2% 0.125W	Metal oxide film	403/4/07181/821
R130, 131	1M 5% 0.25W	Metal oxide film	403/4/07118/001
R133	2.7k		403/4/07181/272
R137, 138, 144, 148	10M 5% 0.25W	Metal oxide film	403/4/07118/013
R140	7.5k 2% 0.125W	Metal oxide film	403/4/07181/752
R143	18k 2% 0.125W	Metal oxide film	403/4/07181/183
R145	68k 2% 0.25W	Metal oxide film	403/4/05524/680
R147, 160	18k 2% 0.25W	Metal oxide film	403/4/05524/180
R150	100k 2% 0.125W	Metal oxide film	403/4/07181/104
R151	1.5k 2% 0.125W	Metal oxide film	403/4/07181/152
R152, 153, 155	2.2k 2% 0.25W	Metal oxide film	403/4/05523/220
R156-159,	3.3k 2% 0.125W	Metal oxide film	403/4/07181/332
R165	15k 2% 0.125W	Metal oxide film	403/4/07181/153
	DIODES		
D21,23, 27	V reg. 10V 5% 400mW	BZX79-C10	415/4/05830/016
D22	V reg. 12V 5% 400mW	BZX79-C12	415/4/05830/018
D24-26, 28-31, 32	75V rev. max. IF(AV) 0.075A	1N4148	415/4/98869
	TRANSISTORS		
TR21,23, 24	N-P-N	BC107	417/4/02028/001
TR22,26	P-N-P	BCY70	417/4/01721/001
TR25	N-P-N	BC109	417/4/02028/000
	INTEGRATED CIRCUITS		
ML11,29, 37*	Quad 2-input NAND gates	HEF4011BD	445/4/03272/011
ML12*	Linear operational amp.	CA3140EX	445/4/03193/008

continued ...

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. STATIC SENSITIVE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.

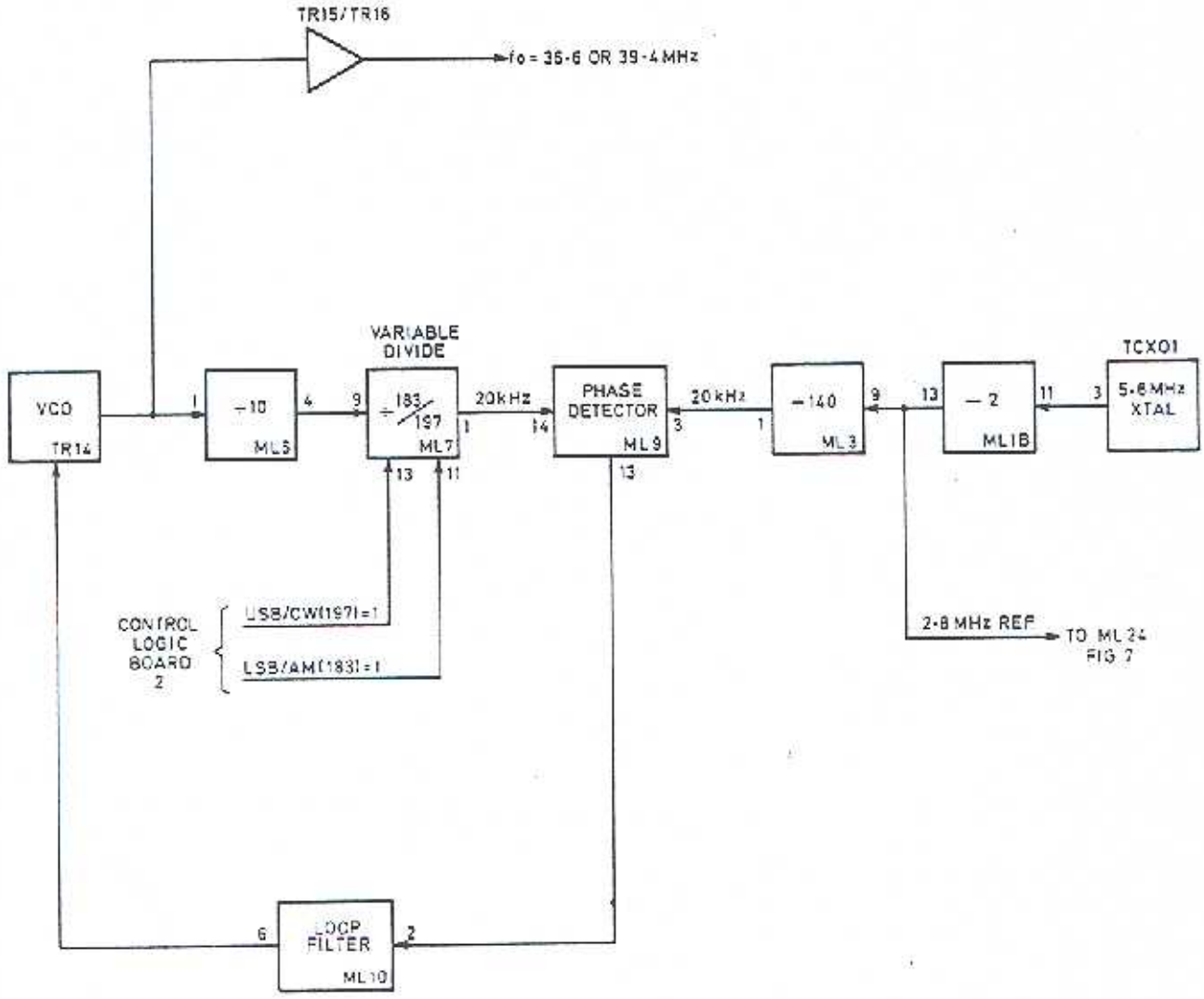


Fig 5 2nd L.O. Synthesiser — block diagram

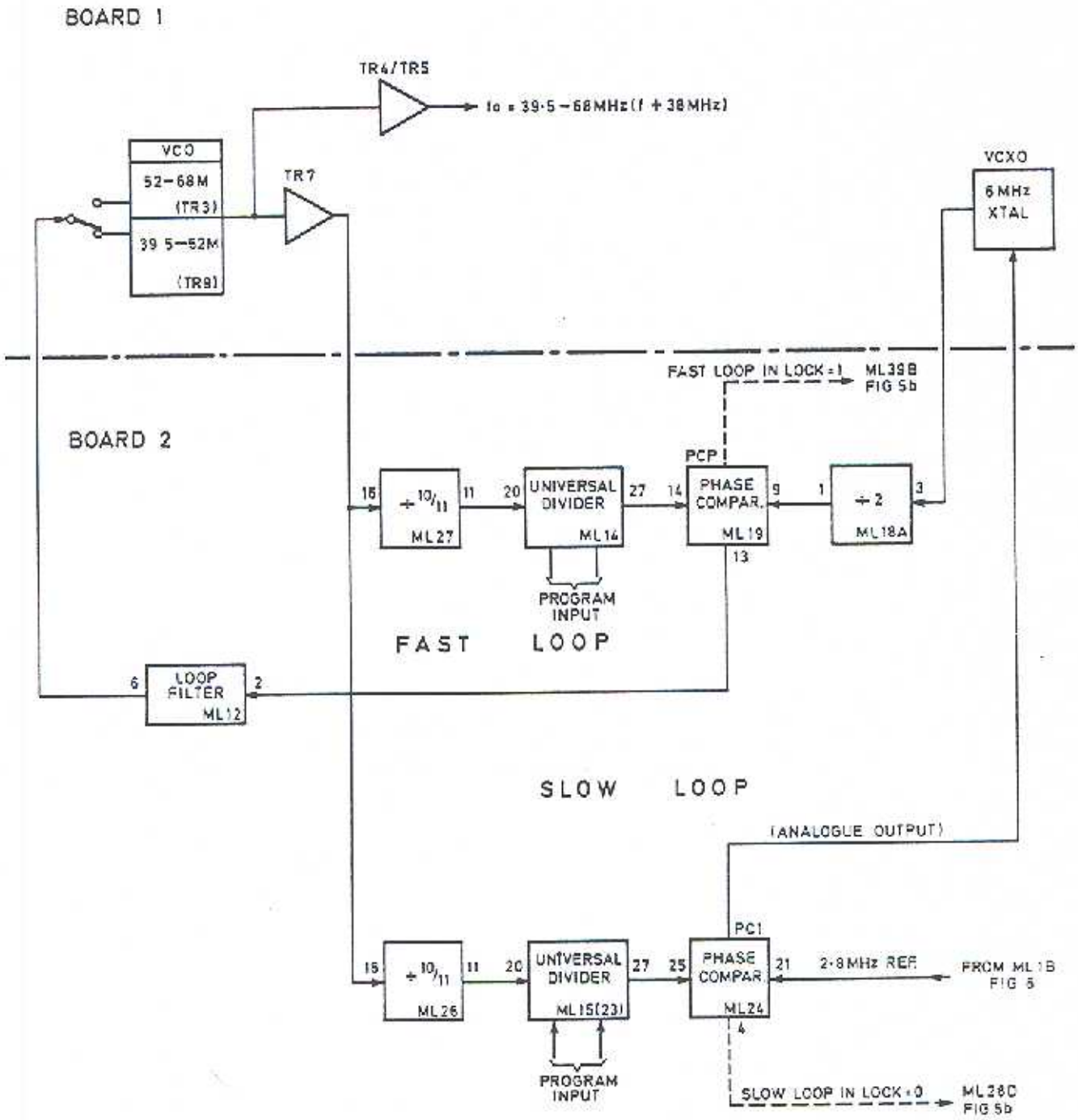


Fig 6 Main synthesiser– block diagram

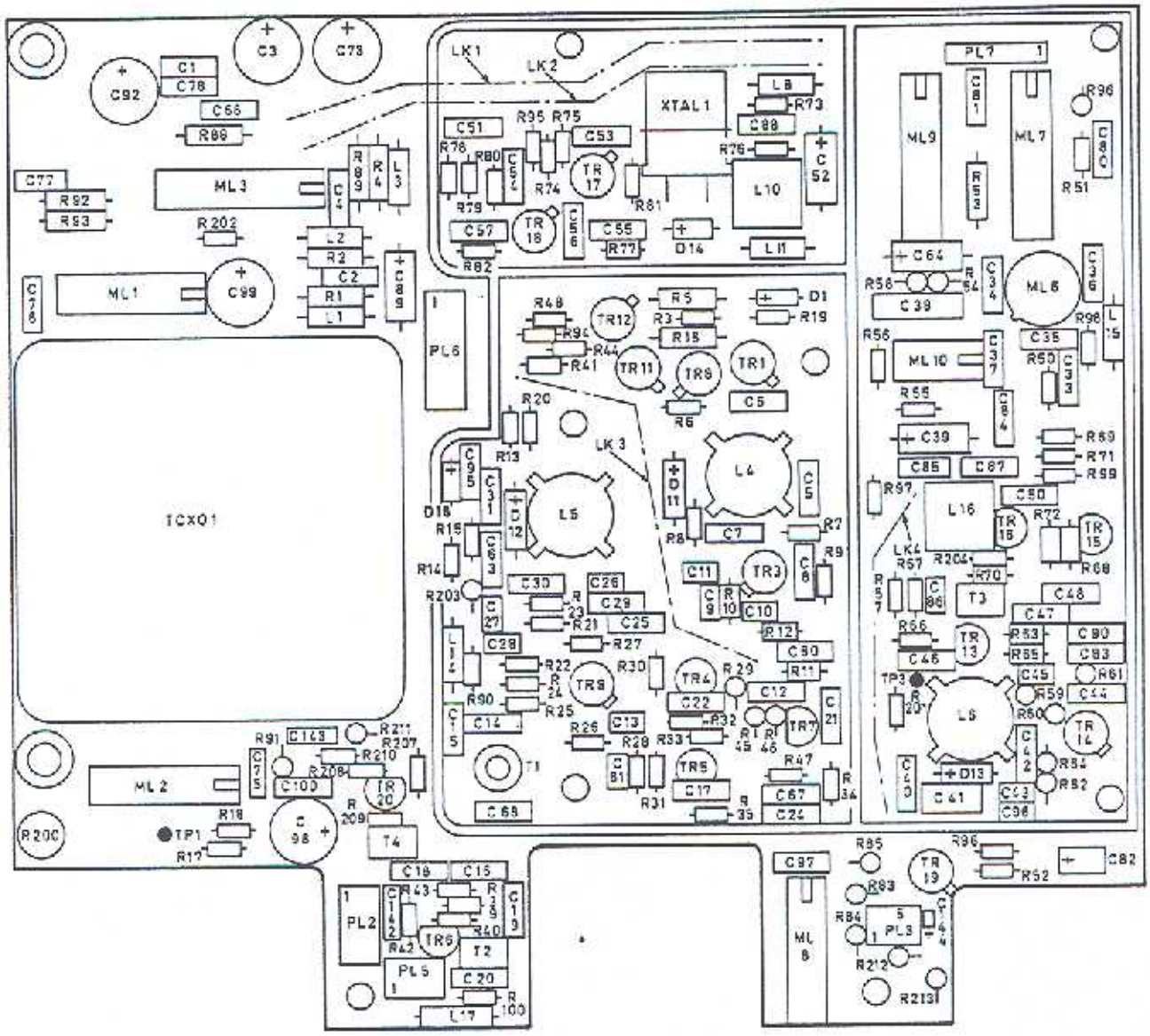
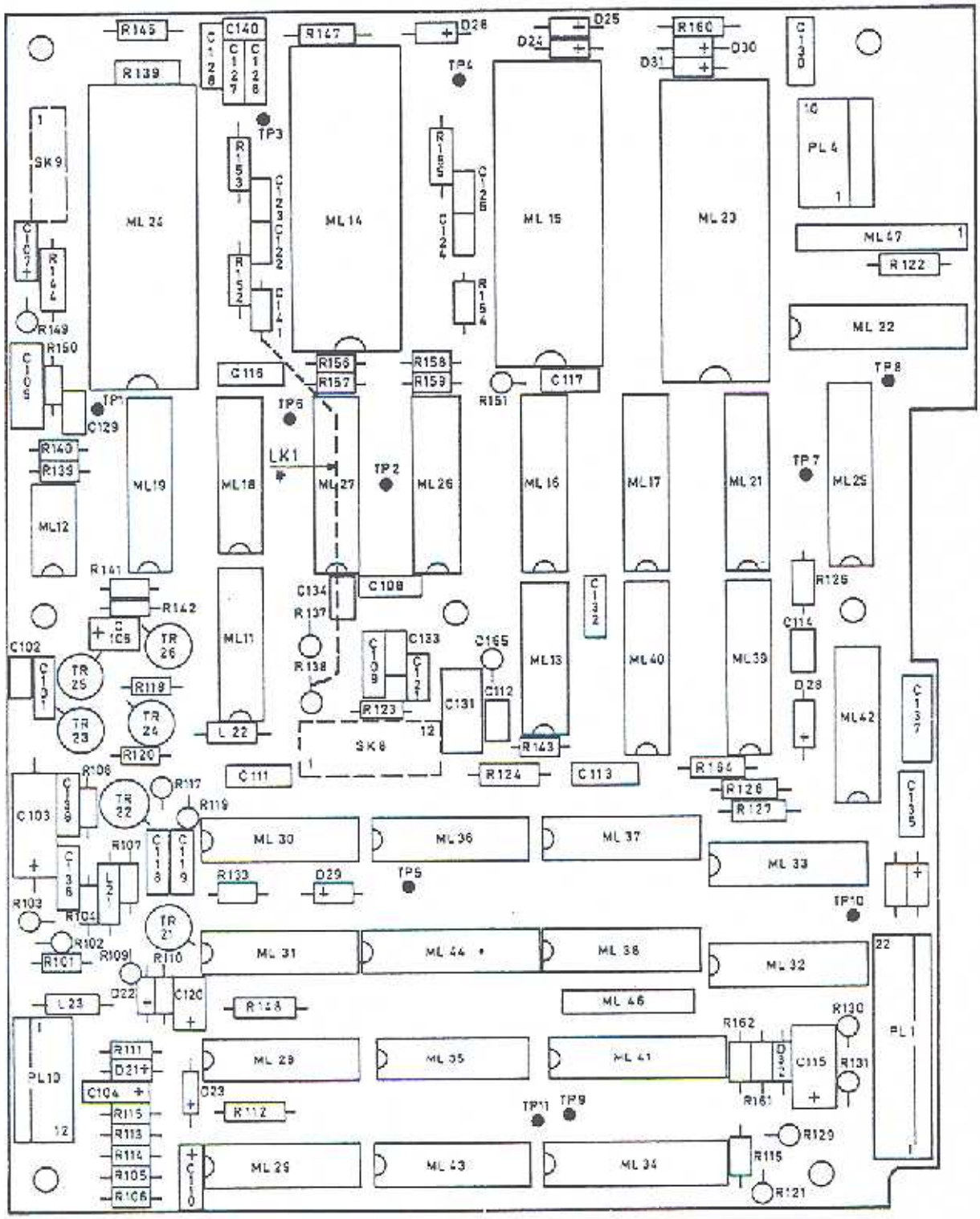
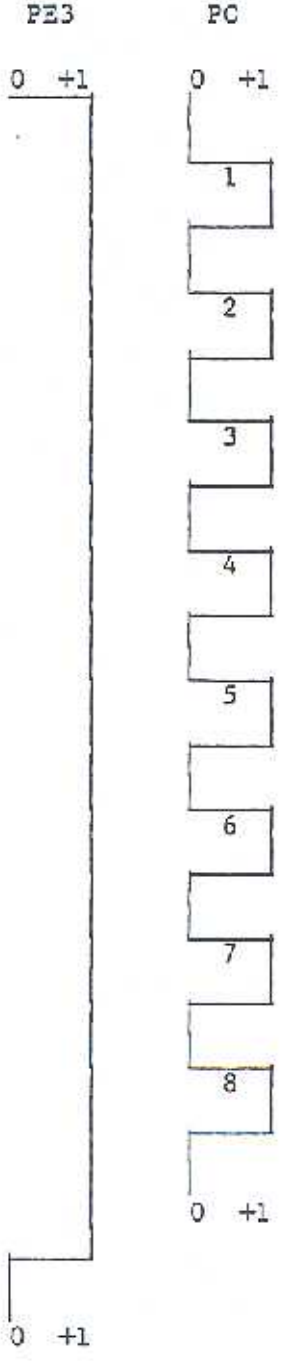


Fig 8 Synthesiser board 1 - component layout



419/1/51219 Iss 3 *NOTE. IT IS IMPORTANT THAT LK1 IS ROUTED AS SHOWN AND SECURED TO ML 27 BY A DAB OF INSULATING VARNISH.

Fig 9 Synthesiser board 2 – component layout

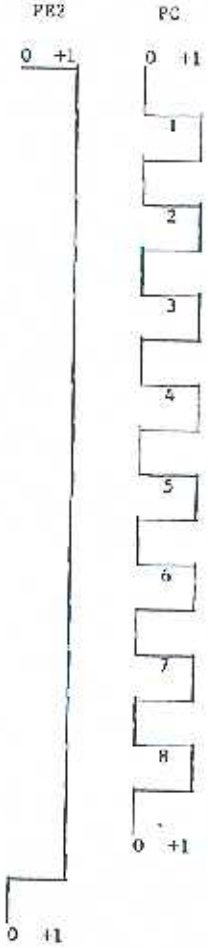


ML23 Pin No.				
1	2	3	4	
1	1	1	0	(FIXED BY ML21)
1	1	1	1	(DON'T CARE)
1	1	1	1	(FIXED)
8's	4's	2's	1's	(Nos. of 100 Hz)
0	1	0	0	(FIXED)
1	1	1	1	(FIXED)
1	1	1	1	(FIXED)
1	1	1	1	(FIXED)
1	1	1	0	(UNTIL PE3 = 1 AGAIN)

Fig.2 Programming of Main Synthesiser Dividers ML23

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
ML13,31, 38*	Hex. inverter	CD4069CN	445/4/03234/469
ML14,15, 23*	Universal divider	HEF4751VD	445/4/03272/751
ML16,17, 21*	Quad AND/OR select gate	CD4019BCNA	445/4/03234/019
ML18*	Dual D-type flip-flop	HEF4013BD	445/4/03272/013
ML19*	Phase comparator and prog. counter	MC14568BCPD	445/4/02383/568
ML22*	Quad D-type flip-flop	CD40175BCN	445/4/03234/175
ML24*	Frequency synthesiser	HEF4750VD	445/4/03277
ML25*	Dual BCD counter	CD4518BCN	445/4/03234/518
ML26,27	Divide by 10/11 prescaler	SP8690A (DC)	445/4/03155/013
ML28,30, 33,35, 36*	Quad 2-input NOR gate	CD4001BCNA	445/4/03234/001
ML32*	Hex Schmitt trigger/ inverter	CD40106BCNA	445/4/03234/106
ML34*	8-chan. data selector	CD4512CN	445/4/03234/512
ML39,44*	Dual mono. multi-vibrator	CD4098BEX	445/4/03234/098
ML40*	Quad tri-state NAND R/S latch	CD4044BCNA	445/4/03234/044
ML41*	Transistor array	ULN2004ABU	445/9/03262
ML42*	Triple 3-input pos. NOR gate	CD4025BCN	445/4/03234/025
ML43*	Quad 2-input AND gate	CD4081BCN	445/4/03234/081
ML46	220k resistor network 5%	Bourns 4306R-101-224	403/4/07113/001
ML47	220k resistor network 2%	Bourns 4308R-101-224	403/4/07075/220
	MISCELLANEOUS		
L21	Inductor RF 47uH 10%		406/4/32161/033
L22,23	Inductor RF	Ferrite bead FX4001	905/4/32161/035
PL4 (Lower)	Plug 5-way	Berg 75168-103-05	508/4/22211/005
PL4 (Upper)	Plug 5-way	Berg 85168-109-05	508/4/22212/005
PL1 (Lower)	Plug 11-way	Berg 75168-103-11	508/4/22211/011
PL1 (Upper)	Plug 11-way	Berg 75168-109-11	508/4/22212/011
PL10 (Lower)	PCB connector 6 male	Berg 75168-103-06	508/4/22211/006
PL10 (Upper)	PCB connector 6 male	Berg 75168-109-06	508/4/22212/006
SK8	PCB connector 12 female	Berg 76325-206	508/4/24138/006
SK9	PCB connector 12 female	Berg 76323-205	508/4/24189/005



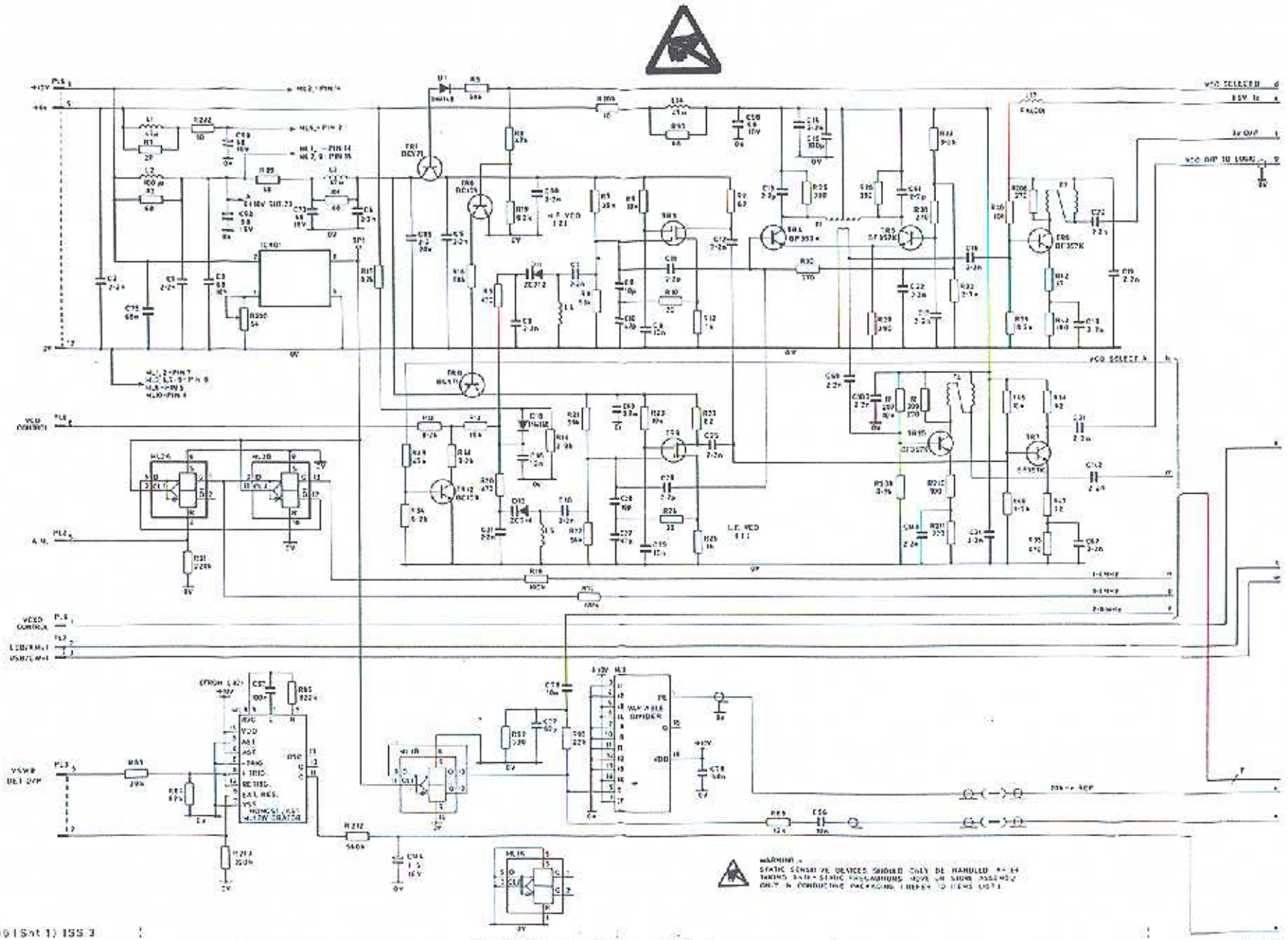
	ML14 Pin No.					ML15 Pin No.				
	1	2	3	4		1	2	3	4	
1	1	1	1	0	(FIXED BY ML16)	0	1	0	0	(FIXED BY ML17)
2	1	1	1	1	(DON'T CARE)	1	1	1	1	(DON'T CARE)
3	1	1	1	1	(FIXED BY ML16)	8's	4's	2's	1's	(Nos. of 1 kHz)
4	8's	4's	2's	1's	(Nos. of 10 kHz)	8's	4's	2's	1's	(Nos. of 10 kHz)
5	8's	4's	2's	1's	(Nos. of 100 kHz)	8's	4's	2's	1's	(Nos. of 100 kHz)
6	8's	4's	2's	1's	(Nos. of 1 MHz)	8's	4's	2's	1's	(Nos. of 1 MHz)
7	8's	4's	2's	1's	(Nos. of 10 MHz)	8's	4's	2's	1's	(Nos. of 10 MHz)
8	1	1	1	0	(FIXED)	1	1	1	0	(FIXED)
0 +1	1	1	1	0	(UNTIL PE2 = 1 AGAIN)	0	1	0	1	(UNTIL PE2 = 1 AGAIN)

Fig.1

Oct.82

Programming of Main Synthesiser Dividers ML14 and ML15

Fig.



419/DA/5121(Sht 1) ISS 3

Fig 3a

Synthesiser board 1 circuit board

Fig 3a

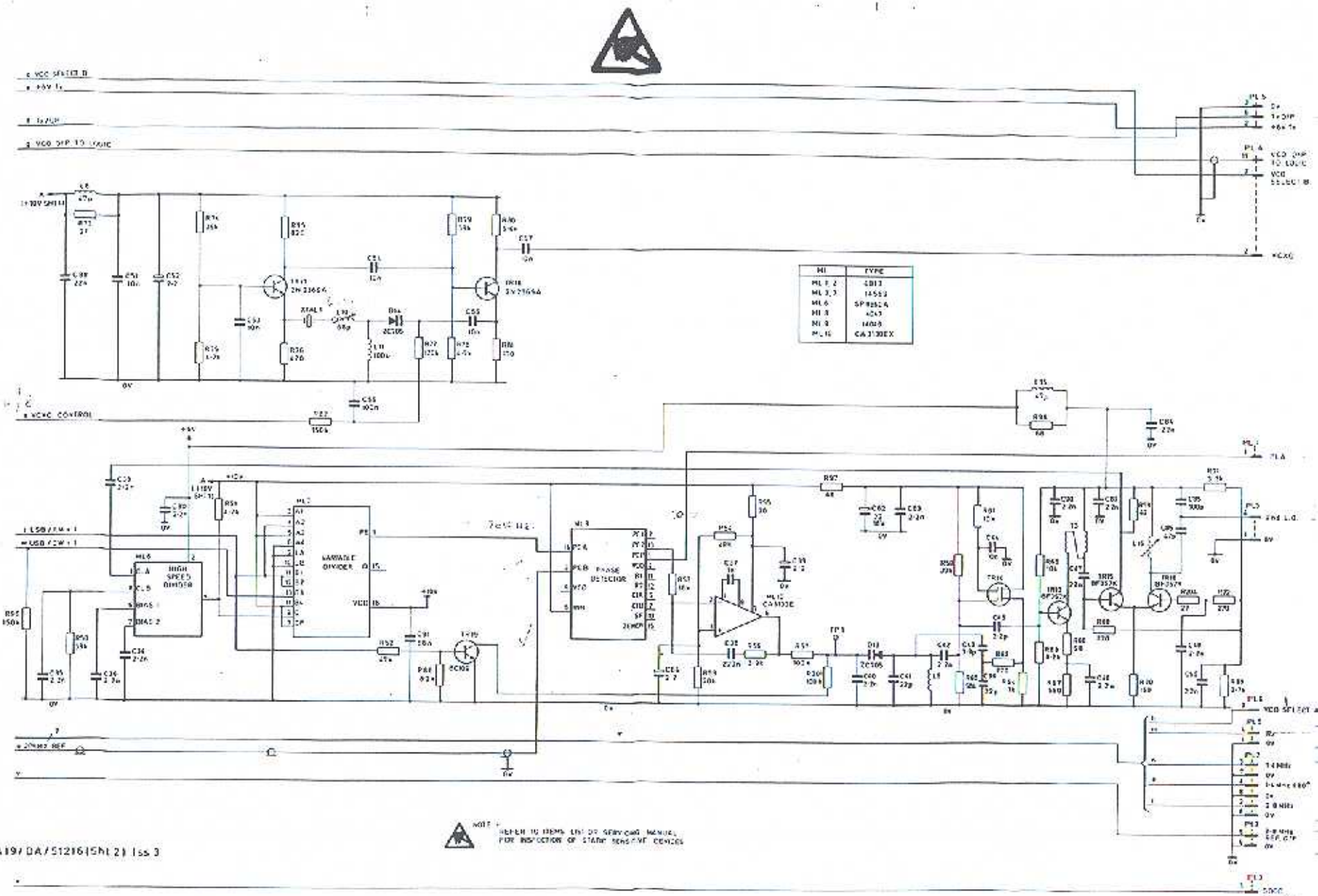


Fig 35 Synthesiser board 1 circuit diagram Fig

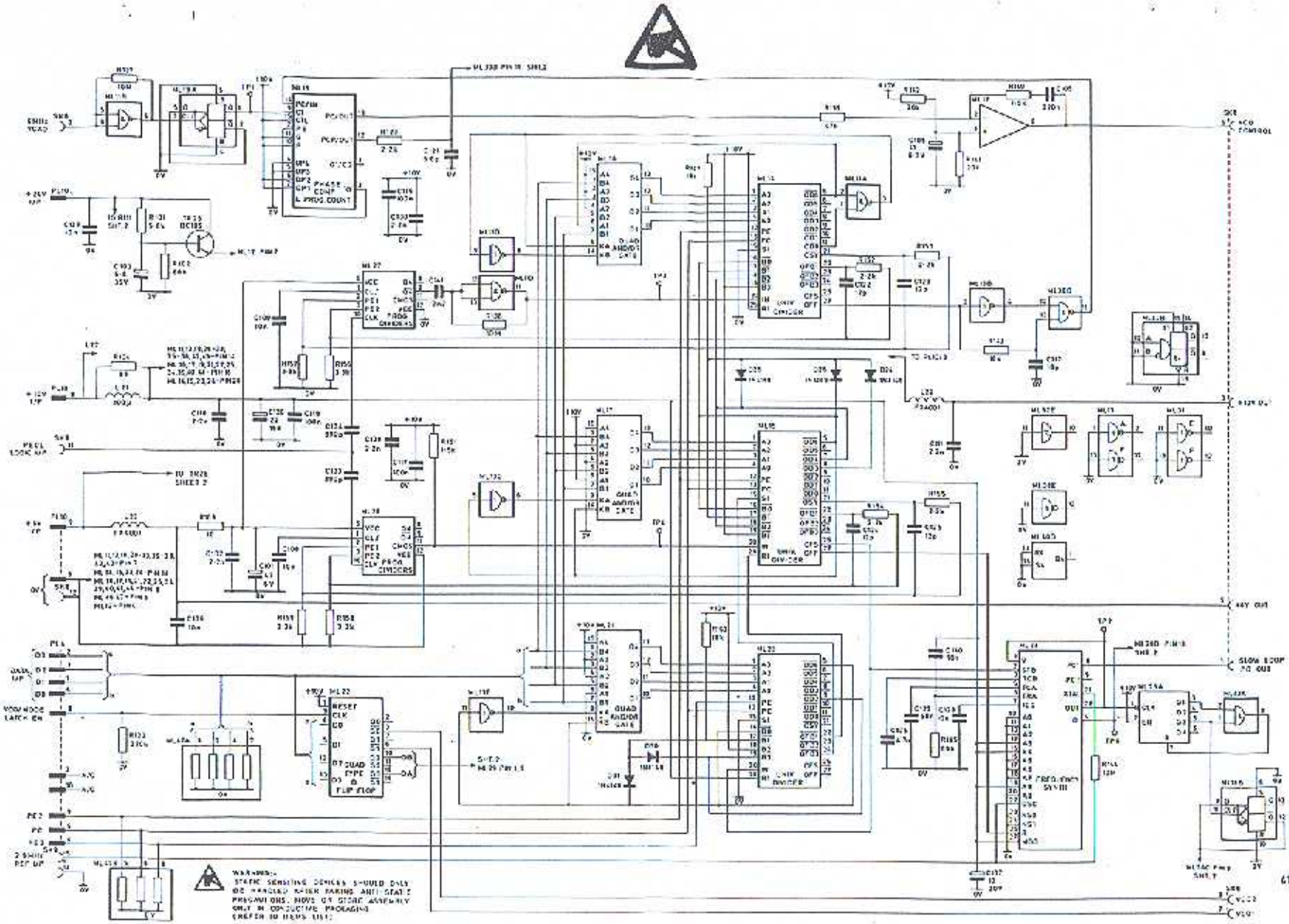
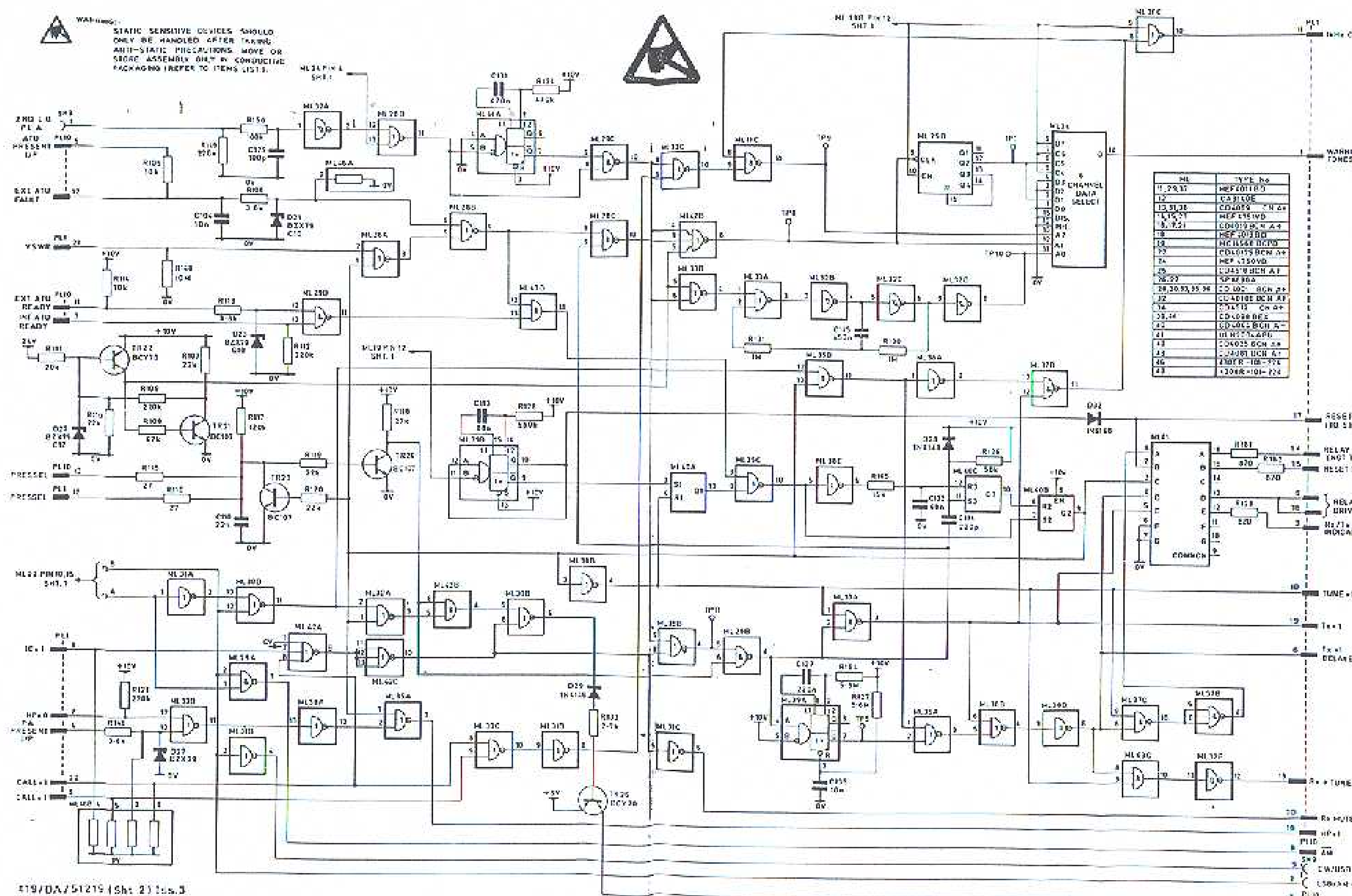


Fig 4a

Synthesiser board 2 : circuit diagram

630/HA/



ML	TYPE No
11,29,37	HEF4011BD
12	CA3130E
13,31,38	CD4069 CN A+
14,15,21	HEF4551VD
16,17,21	CD4013 BCN A+
18	HEF4013BD
19	MC14568 BCPD
23	CD4015 BCN A+
24	HEF4150VD
25	CD4518 BCN A+
26,27	SP8790A
28,30,33,35,36	CD4001 BCN A+
32	CD40108E BCN AF
34	CD4518 CN A+
39,44	CD4098 BEX
40	CD4053 BCN A+
41	HI1 672 APL
43	CD4025 BCN A+
44	CD4081 BCN A+
46	4308 R-101-226
48	4308 R-101-224

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Fig 4b

Synthesiser board 2 : circuit diagram

Jan 84

THIRD LINE SERVICING

OF

BANDPASS FILTER MODULE 630/1/38186

(BPF BOARD 1 - 419/1/51222)

(BPF BOARD 2 - 419/1/51225)

CONTENTS

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Circuit description	3
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ILLUSTRATIONS

Fig.

1 RF path between boards 1 and 2
2 BPF board 1 : circuit diagram
3 BPF board 2 : circuit diagram
4 BPF board 1 : component layout
5 BPF board 2 : component layout

TECHNICAL DESCRIPTION

Introduction

1. The Bandpass Filter (BPF) module comprises two printed circuit boards. Interconnection between the boards is by board mounted pins and sockets connected as follows:

Board 1 (Lower)		Board 2 (Upper)
SK6	connected to	SK4
SK9	connected to	SK2

ie. SK6/1 connected to SK4/1 etc.

2. The two boards provide the circuitry for:

(1) Eight bandpass filters, any one of which can be individually inserted in the RF transmission path by the operation of reed relays.

(2) A low pass filter network at the output of the bandpass filter stage.

(3) A receiver first intermediate frequency (1st IF) mixer stage and a 38 MHz band-stop filter.

Circuit description

3. Circuit diagrams of the two boards forming the BPF module are given in Figures 2 and 3. The mixer circuit and the BPF's are not associated in any way and are treated separately in the following description.

Bandpass filters (Figs.2 and 3)

4. Four of the eight BPF's are located on each board and the RF path between the boards is illustrated in Figure 1.

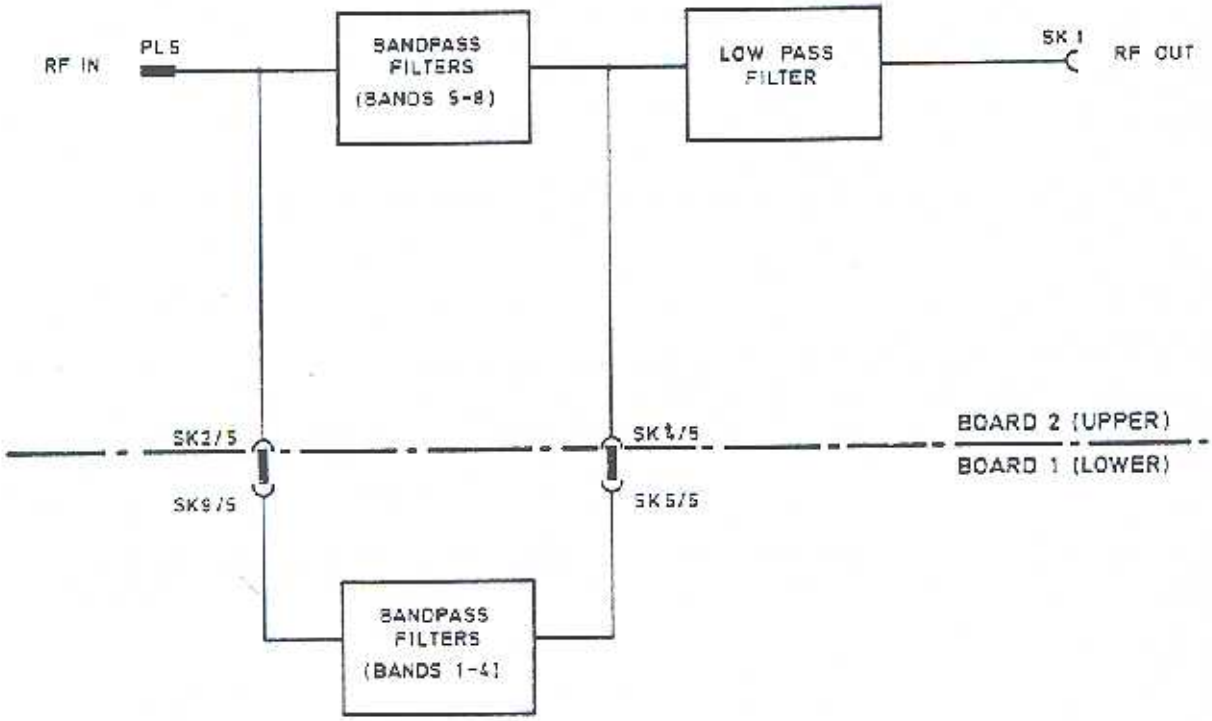


Fig.1 RF path between boards 1 and 2

5. The frequency bands are shown in Table 1 which also shows which relays are set to select the filter for each band.

Table 1 - Frequency bands and connecting relays

Band	Frequency range (MHz)	Relays
1	1.5 - 2.19	RLK/RLO)
2	2.2 - 3.19	RLL/RLP) Board 1
3	3.2 - 4.56	RLM/RLQ) (Lower)
4	4.6 - 6.59	RLJ/RLN)
5	6.6 - 9.59	RLD/RLH)
6	9.6 - 13.89	RLC/RLG) Board 2
7	13.9 - 20.19	RLB/RLF) (Upper)
8	20.2 - 29.99	RLA/RLE)

6. The reed relays are bistable; each pair of relays has its own SET line but all the relays (8 pairs) share a common RESET line which enters the module at PL3/6.

7. Consider the operation of the module for a frequency in the band 1.5 - 2.19 MHz. The external control circuitry (eg. microprocessor) will generate a short OV pulse on the BAND 1 SET line connected to PL1/3 on board 2. This is routed via R4 and SK4/3 to SK6/2 on Board 1. Resistor R1 and capacitor C40 suppress transient voltages produced when the OV condition is disconnected from the relay coils. The OV on SK6/2 of Board 1 energises coil 2-3 of RLO which makes contacts RLO/1 and RLO/4, connecting the incoming RF signal to the Band 1 filter network. The same pulse on coil 5-6 of RLK makes contacts RLK/4 and RLK/7, connecting the output of the Band 1 filter via SK6/5 (Board 1) and SK4/5 (Board 2) to a low pass filter. The three sections of this filter (L1, L2 and L3) are tuned for maximum insertion loss at 38 MHz, 51.20 MHz, and 87.96 MHz respectively. After filtering the RF leaves the module at SK1.

8. When the operating frequency in use is changed to one in another band, an OV RELAY RESET pulse from the external control circuit resets relays RLO and RLK and connects the input and output of the Band 1 filter to ground via contacts RLO4/7 and RLK1/4. The filter appropriate to the new working frequency is then connected in the RF path by an OV pulse on the appropriate BAND SET line.

9. Filter FL1 provides a harmonic trap on the PA side of the filter serving Band 6.

10. Grounding the inputs and outputs of all the filters not in use prevents any mutual coupling interference with the working filter.

Receiver first IF mixer circuit (Fig.2)

11. Signals received by the radio in the range 1.5 - 30 MHz are connected to the first IF mixer stage on Board 1 at Rx INPUT, PL7/6. The Rx signal is then routed through a low pass filter network which is tuned (L20) to reject frequencies of 38 MHz $\pm$ 100 kHz. After filtering the signal is transformer coupled by T1 to a balanced modulator ML1 where it is mixed with the local oscillator frequency in the range 39.5 - 68 MHz which will yield a 38 MHz difference with the incoming signal carrier frequency. The output from the mixer into

the primary of T2 is the first IF frequency of 38 MHz modulated by the audio frequency components carried by the received RF. The 1st IF signal leaves the board at PL8/4.

Testing and alignment

12. Testing and alignment information for the BPF module is given in Part 4 of this manual.

COMPONENTS LIST

13. The principal component parts of Bandpass Filter Module 630/1/38186 are BPF Board 1 - 419/1/51222 and BPF Board 2 - 419/1/51225.

14. The principal component parts of the two boards are:

Circuit ref.	Description & Tolerance			Manufacturer & Ref.	Plessey Part No.
BOARD 1					(419/1/51222)
	CAPACITORS				
C50	82pF	2%	100V	Mullard 632-34829	400/4/20674/021
C51	136pF	1%	400V	ITT 454-49/MS89	438/4/25904/072
C52	150pF	2%	100V	Mullard 682-34151	400/4/21413/024
C53	66pF ± 1pF		400V	ITT 454-49-66-1pF-400V	438/4/25904/094
C54	26pF ± 1pF		400V	ITT 454-49-26-1pF-400V	438/4/25904/087
C55	15pF	2%	100V	Mullard 632-10159	400/4/20674/012
C56,57	100nF	10%	63V	Wima MKS2	435/4/90829/016
C58-61	10nF	10%	63V	Wima MKS2	435/4/90829/023
C62	100nF	5%	100V	Siemens B32560-D1104J	435/4/90317/014
C63,64, 72,73	168pF	1%	400V	ITT 454-49 400-168-1%MS89	438/4/25904/069
C65,66, 76,77	460pF	1%	400V	ITT 454-52 400-460-1%MS139	438/4/25907/059
C67,68, 80,81	306pF	1%	400V	ITT 454-52 400-306-1%MS139	438/4/25907/060
C69,70, 84,85	243pF	1%	400V	IFF 454-89 400-243-1%MS89	438/4/25904/070
C71	712pF	1%	400V	ITT 454-52 400-712-1%MS139	438/4/25907/063
C74,75	879pF	1%	400V	ITT 454-52 400-879-1%MS139	438/4/25907/065
C78,79	2.166nF	1%	125V	ITT 454-52 125-2166-1%MS139	438/4/25907/061
C82,83	1.750nF	1%	400V	ITT 454-52 400-1750-1%MS139	438/4/25907/062
C86,87	1.264nF	1%	400V	ITT 454-52 400-1264-1%MS139	438/4/25907/064
C88,89	250pF	1%	400V	ITT 454-49 400-250-1%MS89	438/4/25904/071
C90	1.336nF	1%	400V	ITT 454-52 400-1336-1%MS139	438/4/25907/066
C91,92	507pF	1%	400V	ITT 454-52 400-507-1%MS139	438/4/25907/067

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C93	33pF 2% 100V	Mullard 632-34339	400/4/20674/016
C94,95	12pF 2% 100V	Mullard 632-10129	400/4/20674/011
	RESISTORS		
R12	1.3k 2% 0.25W	Metal oxide film	403/4/05523/130
R13	390 ohm 2% 0.25W	Metal oxide film	403/4/05522/390
R14	470 ohm 2% 0.25W	Metal oxide film	403/4/05522/470
R15	200 ohm (variable) 10% 0.5W	Wire-wound	404/9/05032/009
R16	51 ohm 2% 0.25W	Metal oxide film	403/4/05521/510
	INDUCTORS		
L20		Cambion 558-1192-02-00-00	406/4/31715/002
L21,25	47 uH ± 10%		406/4/32161/033
L22	0.22 uH ± 10%		406/4/32161/005
L23	0.33 uH ± 10%		406/4/32161/007
L24	0.47 uH ± 10%		406/4/32161/009
L26,34, 41			406/4/31844/015
L27,36			406/1/31844/016
L28,38			406/1/31844/017
L29,32, 40			406/1/31844/018
L30			406/1/31844/019
L31			406/1/31844/020
L33			406/1/31844/022
L35			406/1/31844/023
L37			406/1/31844/024
L39			406/1/31844/025
	MISCELLANEOUS		
ML1	Integrated cct. Mixer	Plessey SL6440CDP	445/4/03382
RLJ,K, L,M,N, O,P,Q	Relay 2700 ohm 24V	Thorn RSL2-24	507/4/05183/003
D1,D2	Diode - switching	IN4148	415/4/98869
D3	Diode - 3.3V regulator	BZX79-C3V3	415/4/05830/004
T1	Transformer RF		406/1/32253
T2	Transformer RF		406/1/32254
SK6,9	Socket 6-way	76323-206	508/4/24189/006
BOARD 2			(419/1/51225)
	CAPACITORS		
C1	12pF 5% 400V	ITT CD08	400/4/21282/002
C2,3,15	82pF ± 1pF 400V	ITT 454-60 or Stability MS89	438/4/25913/007

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance			Manufacturer & Ref.	Plessey Part No.
C4,5	57pF ± 1pF		400V	ITT 454-60 or Stability MS89	438/4/25913/004
C6	37pF ± 1pF		400V	ITT 454-60 or Stability MS89	438/4/25913/002
C7,8	61pF ± 1pF		400V	ITT 454-60 or Stability MS89	438/4/25913/005
C9	15pF	5%	100V		400/4/19301/150
C11	63pF ± 1pF		400V	ITT 454-60 or Stability ML89	438/4/25913/006
C12	1nF	10%	100V		435/4/90821/011
C13	160pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/030
C14	52pF ± 1pF		400V	ITT 454-60 or Stability MS89	438/4/25913/003
C16,17	86pF ± 1pF		400V	ITT 454-49-86-1pF-400V	438/4/25904/095
C18,19	128pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/098
C20,21	138pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/099
C22,23	244pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/077
C24	297pF	1%	400V	ITT 454-52 or Stability MS139	438/4/25907/068
C25,35	297pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/078
C26,27	133pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/079
C28	45pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/097
C29	149pF	1%	400V	ITT 454-49 or Stability MS89	438/4/25904/081
C30	60pF ± 1pF		400V		438/4/25904/092
C31,32	95pF ± 1pF		400V	ITT 454-49 or Stability MS89	438/4/25904/055
C33,34	168pF ± 1pF		400V	ITT 454-49 400-168-1%MS89	438/4/25904/069
C36	331pF	1%	400V	ITT 454-52 or Stability MS89	438/4/25907/069
C37-45	100nF	5%	100V	Siemens B32560-D1104J	435/4/90317/014
C46	350pF	1%	125V	ITT 454-49-125-350-1%	438/4/25904/085
	RESISTORS				
R1-8	120 ohm	2%	0.25W	Metal oxide film	403/4/05522/120
R9	18 ohm	2%	0.25W	Metal oxide film	403/4/05521/180
	INDUCTORS				
L1	0.107 uH				406/1/31843/001
L2	0.247 uH				406/1/31844/001

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
L3	0.227 uH		406/1/31849/001
L4,14	0.134 uH		406/1/32158/001
L5,15	0.357 uH		406/1/31844/002
L6	0.568 uH		406/1/31844/007
L7,17	0.598 uH		406/1/31844/009
L8	0.342 uH		406/1/31844/003
L9	1.89 uH		406/1/31844/006
L10	2.67 uH		406/1/31844/010
L11	1.09 uH		406/1/31844/004
L12	0.439 uH		406/1/31844/005
L13	0.816 uH		406/1/31844/011
L16	0.439 uH		406/1/31844/008
	MISCELLANEOUS		
RLA to RLH	Reed relay 2700 ohm 24V		507/4/05183/003
PL3 (Lower)	Plug 5-way	Berg 75168-103-05	508/4/22211/005
PL3 (Upper)	Plug 19-way Rt. Angle	Berg 75168-109-05	508/4/22212/005
SK1	Socket 50 ohm Rt. Angle	Radiall R115.666	508/4/22110
SK2,SK4	Socket	Berg 75302-001	508/4/22131
FL1	Filter		422/1/07829

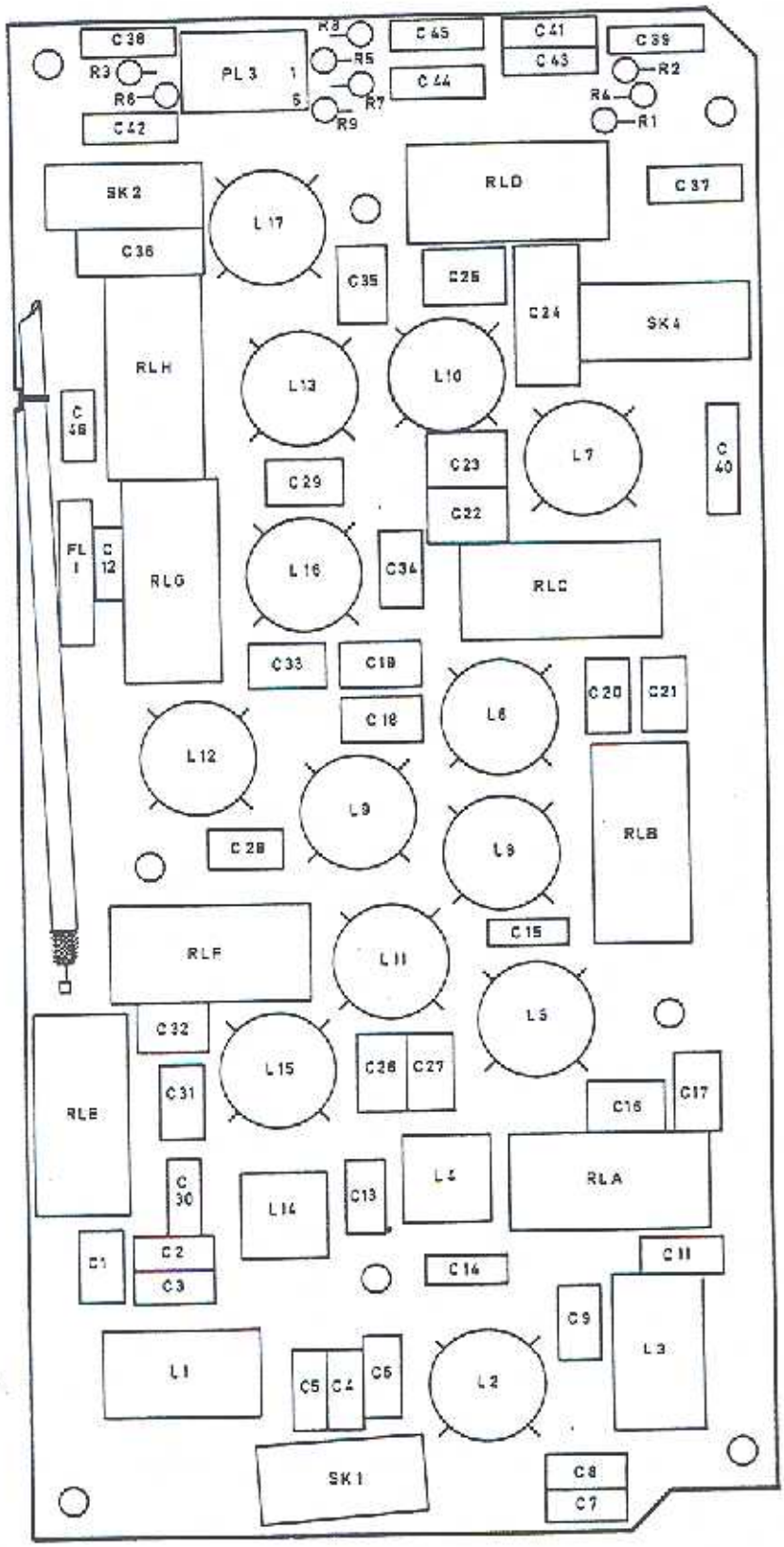


Fig 5 Bandpass filter board 2 – component layout

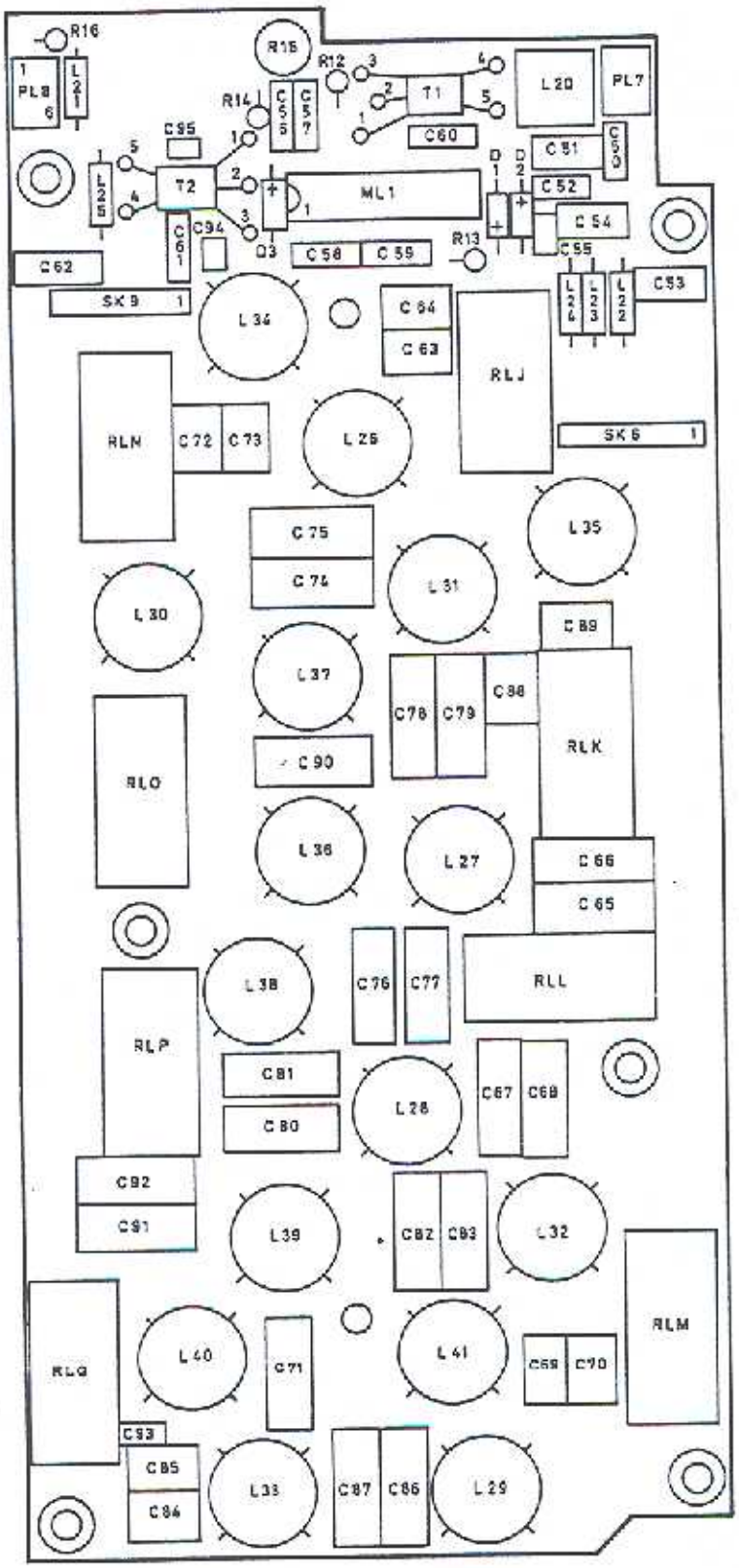
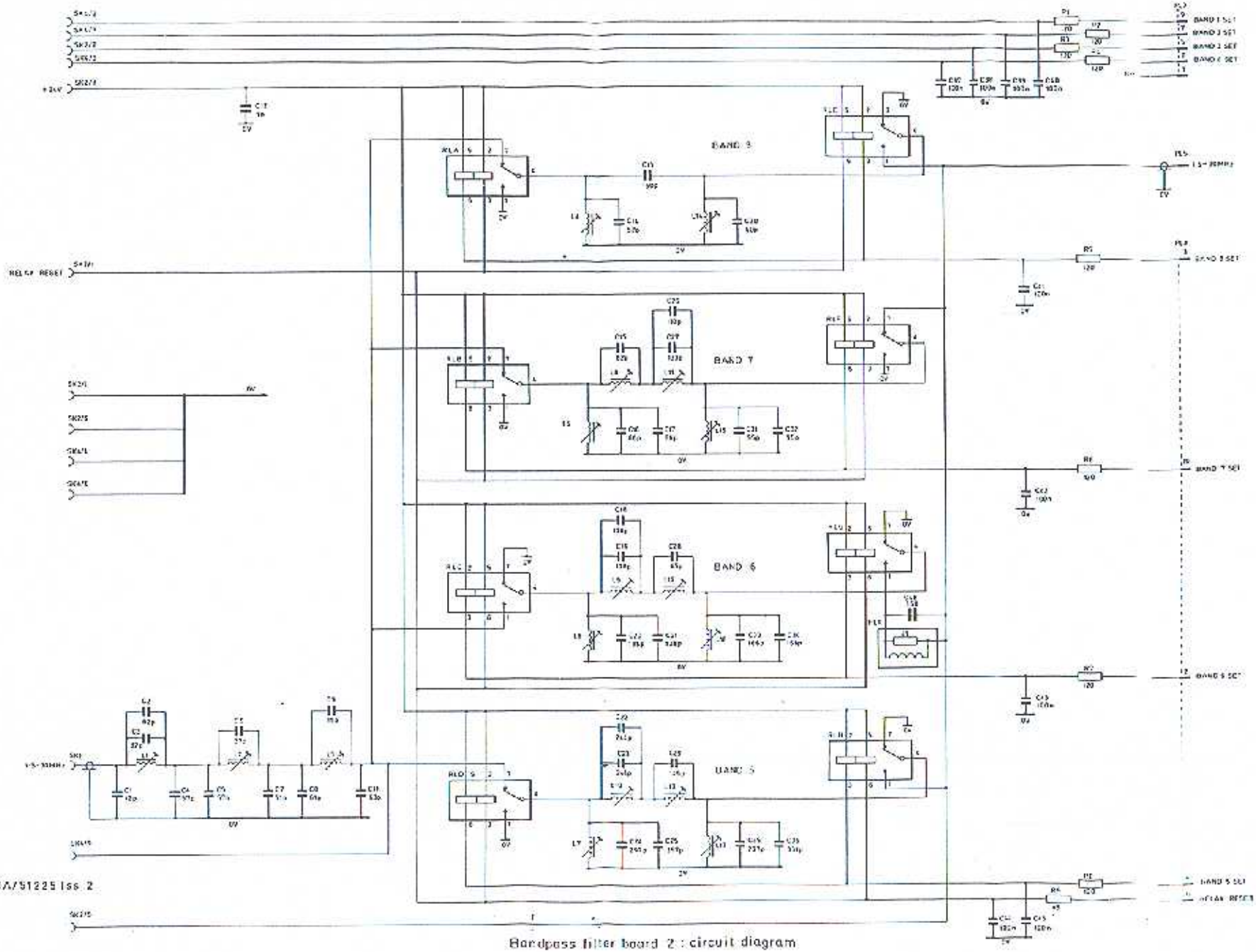


Fig 4 Bandpass filter board 1 — component layout



415/CA/91225 Iss 2

Fig 3 Bandpass filter board 2 : circuit diagram

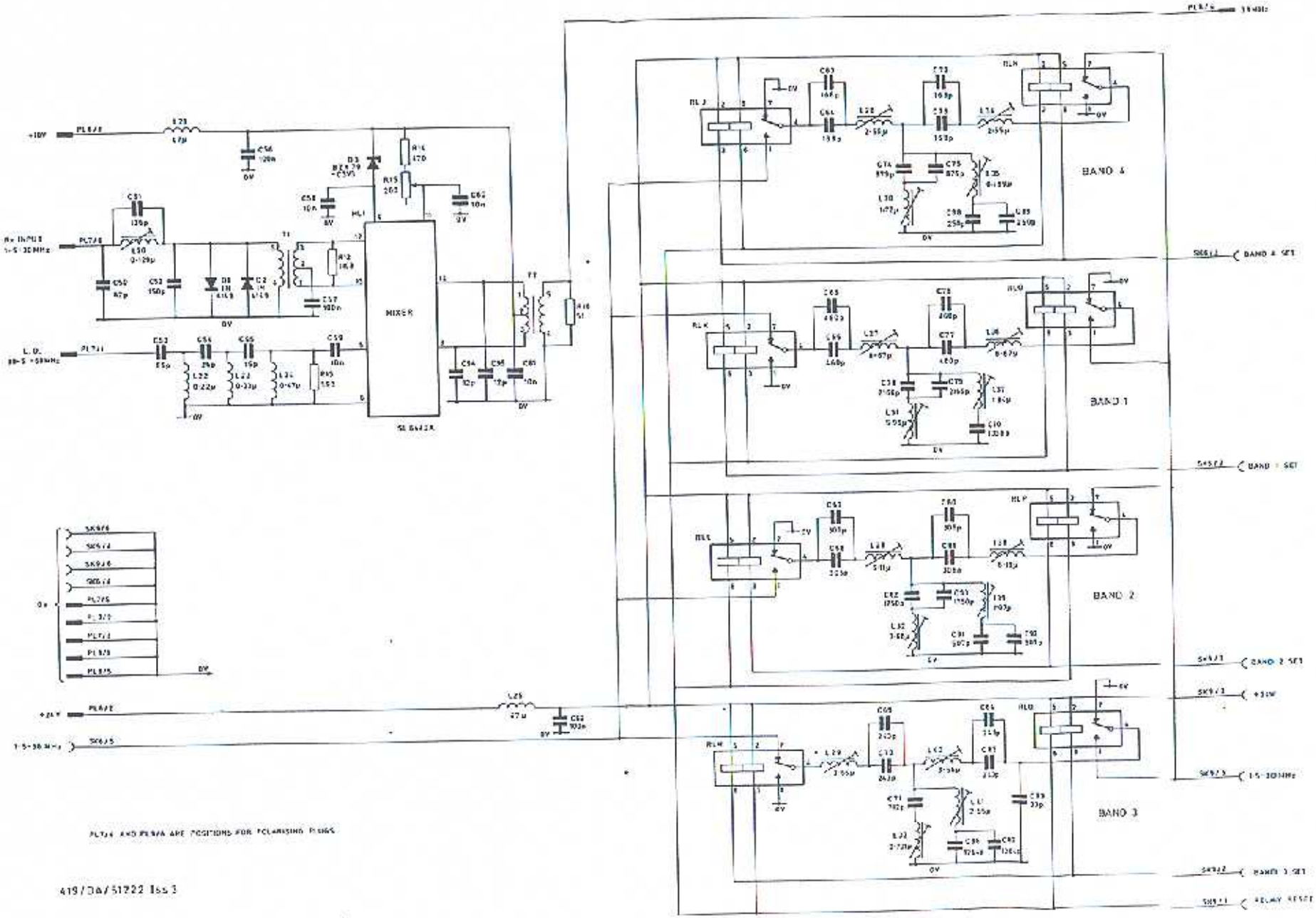


Fig 2 Bandpass filter board 1 : circuit diagram

THIRD LINE SERVICING

OF

POWER AMPLIFIER BOARD 419/1/51228

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ILLUSTRATIONS

Fig.
1 Power amplifier board : circuit diagram
2 Power amplifier board : component layout

TECHNICAL DESCRIPTION

General

1. The principal function of the Power Amplifier Board is to boost the rf output of the radio intermediate frequency (IF) stage and provide an output capability of 20W pep at the 50 ohm output socket of the radio. The amplifier circuit includes:

(1) A low-pass filter to suppress the image produced by the mixing process on the preceding IF Board.

(2) A three-stage power amplifier.

(3) An automatic level control circuit (ALC) to stabilise the output power and prevent damage to the output transistors if excessive input signals or external mismatches occur at the output.

2. The board also carries a VSWR comparator circuit which is not a functional part of the power amplifier circuit itself, but which operates in conjunction with a VSWR detector circuit on the antenna tuning unit (ATU) to produce a signal to the Synthesiser Board, if the VSWR is worse than 3:1.

Circuit description

3. The circuit of the Power Amplifier Board is given in Fig.1. The circuit description which follows is divided into four parts, namely:

(1) RF path.

(2) Bias circuits.

(3) Automatic level control (ALC).

(4) VSWR comparator.

RF path

4. RF input to the board from the preceding IF stages is at PL1/6. The incoming signal is routed through a low-pass filter comprised of two resonator circuits. The resonators are tuned to reject 54.84 MHz (L2/C6) and 39.03 MHz (L3/C8) respectively.

5. After the filter the RF path is through a gain control attenuator formed by the four PIN diodes D1 to D3, and D10. Attenuation is controlled by a dc voltage level generated by the automatic level control circuitry (ALC) which regulates the base drive of the first amplifier stage; the class A amplifier circuit of TR3.

6. The amplified signal on the collector of TR3 is transformer coupled to a class AB driver amplifier (TR4/TR5) which in turn is transformer coupled (T2) to the power output pair TR6 and TR7 which also operate in class AB. The amplified RF output is routed via the Tx/Rx relay RLA to leave the board at PL3.

Bias circuits

7. The bias for the Class A stage is fixed by resistors R9, R10 and R11 which sets the dc base voltage at about 4.3 volts.

8. Bias for the driver stage transistors TR4 and TR5 is controlled by the voltage across resistors R17 and R18 respectively. This voltage is controlled by the driver stage bias circuit which includes R59, R60, TR17, and TR18 which provide a constant voltage source for these resistors to the centre point of transformer T1 secondary. Potentiometer R59 provides an adjustment to set the bias, and TR17 acts as a thermal sensor to provide temperature compensation. When used for high power transmissions the R66 path is open circuit at transistor Q1, but when low power is selected Q3 is switched off and Q1 is turned on. Resistor R66 is then grounded and effectively in parallel with the resistance between R59 wiper and ground, increasing the bias voltage to the amplifier stage.

9. A similar circuit configuration is used for the output stage bias across R23 and R24. The output stage bias circuit includes R65, R67, TR19, TR20, and TR21. In this circuit TR19 acts as the thermal sensor.

Automatic level control

10. The forward and reverse power components are monitored at the output of the Power Amplifier Board by coupling networks which are connected to the output path by capacitors C26 and C30 and transformer T4. The capacitors provide a sample of the line voltage; the transformer a sample of the line current; to the coupler network where they are compared for phase and magnitude, rectified (D4 and D6) and produce a resultant dc voltage at the junction of R29/R30. As the forward power increases the value of the resultant dc voltage will follow proportionally. If the reverse power component increases sufficiently, due

perhaps to a mismatch on the outgoing line, D5 will no longer be reverse biased and the resultant standing voltage at R29/R30 will be dependent only on the reverse component of output power.

11. Thus any rise or fall in the peak envelope power at the output of the amplifier will be reflected by an increase or decrease in the resultant voltage appearing at the junction of R29/R30. This voltage is connected to the input of the ALC circuit at ML1A/3 where it is amplified and applied to the inverted input of ML1B. Hence any sudden increase in voltage at ML1A/3 will cause a proportionate reduction at ML1B/7. The emitter of TR13 must track this falling voltage (to maintain the 1.4V differential due to D14 and TR13 etc.) and in turn the emitter voltage of TR15 must follow suit. Hence the dc voltage connected via L4 to the PIN diodes is decreased causing an increase in attenuation of the incoming signal.

12. Conversely, if the output power level falls, the forward bias on the PIN diode attenuator will increase to produce a reduction in attenuation of the incoming signal. To prevent the ALC reacting to the reduced pep in the space between each word of a transmitted message, a 'fast attack' 'slow decay' feature is provided by capacitor C46 and resistor R53. The capacitor can discharge quickly when a sudden increase in pep is detected, but the 220 kilohm resistor (R53) in the charging circuit of C46 ensures a delayed reaction to a drop in the output pep level.

13. Potentiometer R46 allows the reference voltage on ML1A to be adjusted to set the operating threshold of the ALC circuit. When operating on low power (LP) the LOW LEVEL COMMAND input on PL1/4 is at logic 0 and transistor Q3 is turned off removing the 0V condition at the junction of R34/R43. This causes transistor Q4 to conduct, connecting the 2.7V zener diode D9 across potentiometer R46 to reduce the reference voltage on ML1A and the operating threshold of the ALC. Transistor Q5 is switched on when working LP to complete the R40, C38 path to ground. This increases the amount of attenuation introduced by the PIN diodes at the signal input to the amplifier.

14. Thermistor R42 has a positive temperature coefficient; when the temperature rises to 110°C its resistance increases rapidly to 1 kilohm and the consequent increase in the dc voltage on ML1B/6 lowers the operating threshold of the ALC to increase the amount of attenuation introduced by the PIN diodes. This effectively reduces the level of output power delivered by the amplifier.

15. A current monitor circuit in the ATU produces an analogue dc voltage output which is proportional to the current through part of the RF matching network. This voltage (normally about 1.5V) is connected to input PL2/8 on the PA Board and routed to the non-inverting input of ML2B. An increase in RF current in the ATU matching network will produce an increase in the voltage level into ML2B, and when this is greater than the reference voltage on the inverting input of ML2B, the output of the comparator (ML2B/7) will go positive, and transistor Q2 will be turned on. This grounds the LOW LEVEL COMMAND line and restricts the amplifier to a low power output.

VSWR comparator

16. The circuit formed by ML2A and its associated components acts as a comparator for the VF and VR inputs on PL2/7 and PL2/6 respectively. The voltage level on these two inputs is controlled by a VSWR detector in the ATU, and the comparator is set to produce a logic 1 output on PL2/5 if the VSWR detected is

worse than 3:1. The VSWR comparator circuit is located on the Power Amplifier Board, but plays no part in the operation of the amplifier circuit.

TESTING AND ALIGNMENT

17. Testing and alignment information for this board will be found in Part 4 of this manual.

COMPONENTS LIST

18. The principal component parts of Power Amplifier Board 419/1/51228 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	CAPACITORS		
C2,10-12,13,33,38,41,43,44,48,50,51,53,54,55,57,58	10nF 10% 63V	Wima MKS2	435/4/90829/023
C5	95pF ± 1pF 400V	BS9070 N002 C2AED-C	438/4/25351/950
C6	30pF ± 1pF 400V	BS9070 N002 C2AED-C	438/4/25351/300
C7	144pF 1% 100V	BS9070 N002 C2AED-C	438/4/25322/144
C8	102pF 1% 100V	BS9070 N002 C2AED-C	438/4/25322/102
C9	58pF ± 1pF 400V	BS9070 N002 C2AED-C	483/4/25351/580
C14,29,39,56	1nF 20% 100V	Wima FKS2	435/4/90821/001
C15,16,20-22,40	10nF 10% 100V	BS9075 N024 Patt.B	400/4/19314/100
C17,24,25,31,35,36	100nF 10% 100V	BS9075 N024 Patt.C	400/4/19495/100
C23	150pF 5% 100V	BS9075 N023 Patt.B	400/4/19302/150
C26,30	2-16pF variable 500V	Mullard 809-05003	401/9/98059/003
C27,32	82pF 2% 100V	Mullard 632-34829	400/4/20674/021
C28	33pF 2% 100V	Mullard 632-34339	400/4/20674/016
C34,45	10uF 20% 35V	BS9073 F002 or F005	402/4/55748/013
C37	150pF 2% 100V	Mullard 632-34151	400/4/20674/024
C42	22uF 20% 25V		402/4/55747/015
C46	4.7uF 20% 35V		402/4/55748/011
C47	2.2nF 20% 100V	Wima FKS2	435/4/90821/003
C49,52	470nF 20% 35V	BS9073 F002 or F005	402/4/55748/005
	RESISTORS		
R7,16	51 ohm 2% 0.25W	Metal oxide film	403/4/05521/510
R8,54	390 ohm 2% 0.25W	Metal oxide film	403/4/05522/390

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R9,10	3k 2% 0.25W	Metal oxide film	403/4/05523/300
R11	330 ohm 2% 0.25W	Metal oxide film	403/4/05522/330
R12	120 ohm 2% 1W	Metal oxide film	403/4/05222/120
R13,47, 50,56, 63	1k 2% 0.25W	Metal oxide film	403/4/05523/100
R14	10 ohm 2% 0.25W	Metal oxide film	403/4/05521/100
R15,40	47 ohm 2% 0.25W	Metal oxide film	403/4/05521/470
R17,18, 23,24, 52	100 ohm 2% 0.25W	Metal oxide film	403/4/05522/100
R19,20	3.3 ohm 2% 0.25W	Metal oxide film	403/4/07148/330
R21,22	91 ohm 2% 0.25W	Metal oxide film	403/4/05521/910
R25,26	150 ohm 2% 0.5W	Metal oxide film	403/4/05322/150
R27,28, 32,33	150 ohm 2% 0.25W	Metal oxide film	403/4/05522/150
R29,37, 49,81, 87	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R30	9.1k 2% 0.25W	Metal oxide film	403/4/05523/910
R31,38, 43	47k 2% 0.25W	Metal oxide film	403/4/05524/470
R34	15k 2% 0.25W	Metal oxide film	403/4/05524/150
R35,75, 76,78	100k 2% 0.25W	Metal oxide film	403/4/05525/100
R36	36k 2% 0.25W	Metal oxide film	403/4/05524/360
R39	5.1k 2% 0.25W	Metal oxide film	403/4/05523/510
R41	130 ohm 2% 0.25W	Metal oxide film	403/4/05522/130
R42	1000 ohm 0.69W (Thermistor)	ITT YC100TB	403/4/07179/004
R44,55	220 ohm 2% 0.25W	Metal oxide film	403/4/05522/220
R45,61, 84	2k 2% 0.25W	Metal oxide film	403/4/05523/200
R46	5k 10% 0.5W (Variable)	3329H/81E	404/9/05032/005
R48	22k 2% 0.25W	Metal oxide film	403/4/05524/220
R51	13k 2% 0.25W	Metal oxide film	403/4/05524/130
R53	220k 2% 0.25W	Metal oxide film	403/4/05525/220
R57	4.7k 2% 0.25W	Metal oxide film	403/4/05523/470
R58	56k 2% 0.25W	Metal oxide film	403/4/05524/560
R59,65	1k 10% 0.5W (Variable)	3329H/81E	404/9/05032/003
R60,83	360 ohm 2% 0.25W	Metal oxide film	403/4/05522/360
R62	510 ohm 2% 0.25W	Metal oxide film	403/4/05522/510
R64	8.2k 2% 0.25W	Metal oxide film	403/4/05523/820
R66	3.3k 2% 0.5W	Metal oxide film	403/4/05523/330
R68	300 ohm 2% 0.25W	Metal oxide film	403/4/05522/300
R67,70	820 ohm 2% 0.25W	Metal oxide film	403/4/05522/820
R69	120 ohm 5% 2.5W	Wire-wound	403/4/04522/120
R71	10 ohm 2% 0.25W	Metal oxide film	403/4/05321/100

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R73,79	10M 5% 0.25W	Mullard VR25 Metal glaze	403/4/07118/013
R77	27k 2% 0.25W	Metal oxide film	403/4/05524/270
R80	470 ohm 2% 0.25W	Metal oxide film	403/4/05522/470
R82,	33k 2% 0.25W	Metal oxide film	403/4/05524/330
R85	4.3k 2% 0.25W	Metal oxide film	403/4/05523/430
R86	560 ohm 2% 0.25W	Metal oxide film	403/4/05522/560
	DIODES		
D1-3,10	P-I-N switching 0.25W	AEI type DB2849E	415/4/05750
D4-7, 13,14	Switching	1N4148	415/4/98869
D9	2.7V regulator 0.4W	BZX79-C2V7	415/4/05830/002
D11,12, 16	5.1V regulator 0.4W	BZX79-C5V1	415/4/05830/009
D15	15V regulator 0.4W	BZX79-C15	415/4/05830/020
	TRANSISTOR		
TR3	N-P-N	2N3866	417/4/01775
TR4,5	N-P-N	2N3553	417/9/01814
TR6,7!!	N-P-N (BERYLLIA!!)	Mullard BLW83	417/4/04369/006
TR13	P-N-P	2TX500	417/4/02035/001
TR14,15	P-N-P	BCY70	417/4/01721/001
TR16,17, 19,20, 22	N-P-N	BC107B	417/4/02028/004
TR18,21	N-P-N	BFY51	417/4/01737/002
	INTEGRATED CIRCUITS		
ML1,ML2*	Operational amplifier (Dual)	RCA CA3240EX	445/4/03274/001
ML3	Transistor array	RCA CA3146E	445/4/03275/001
	INDUCTOR		
L2	Variable		406/1/32256/001
L3	Variable		406/1/32256/002
L4	47uH	BS9751 N0001 Patt.A	406/4/32161/033
L5-7	15uH	BS9751 N0001 Patt.A	406/4/32161/027
L10	1uH		406/4/31754/001
L11	Inductor, RF		406/1/32373
L12	1mH	BS9751 N0001 Patt.A	406/4/32161/049
L13	100uH	BS9751 N0001 Patt.A	406/4/32161/037
FL1,FL2	4uH/27 ohm		406/1/32257

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	MISCELLANEOUS		
T1	Transformer RF		405/1/14470
T2	Transformer RF		405/1/14471
T3	Transformer RF		405/1/14472
T4	Transformer RF		405/1/14473
	(Secondary)		
	Coaxial (T4 Primary)		630/1/42958
RLA	Relay 1250 ohm 24V		507/9/05097/003
PL1 (Lower)	Plug Rt. Angle	Berg 75168-103-03	508/4/22211/003
PL1 (Upper)	Plug Rt. Angle	Berg 75168-109-03	508/4/22212/003
PL3	Plug 50 ohm	Radiall R114.426	508/4/24190

WARNING ...

*DENOTES STATIC SENSITIVE DEVICE. THESE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING.

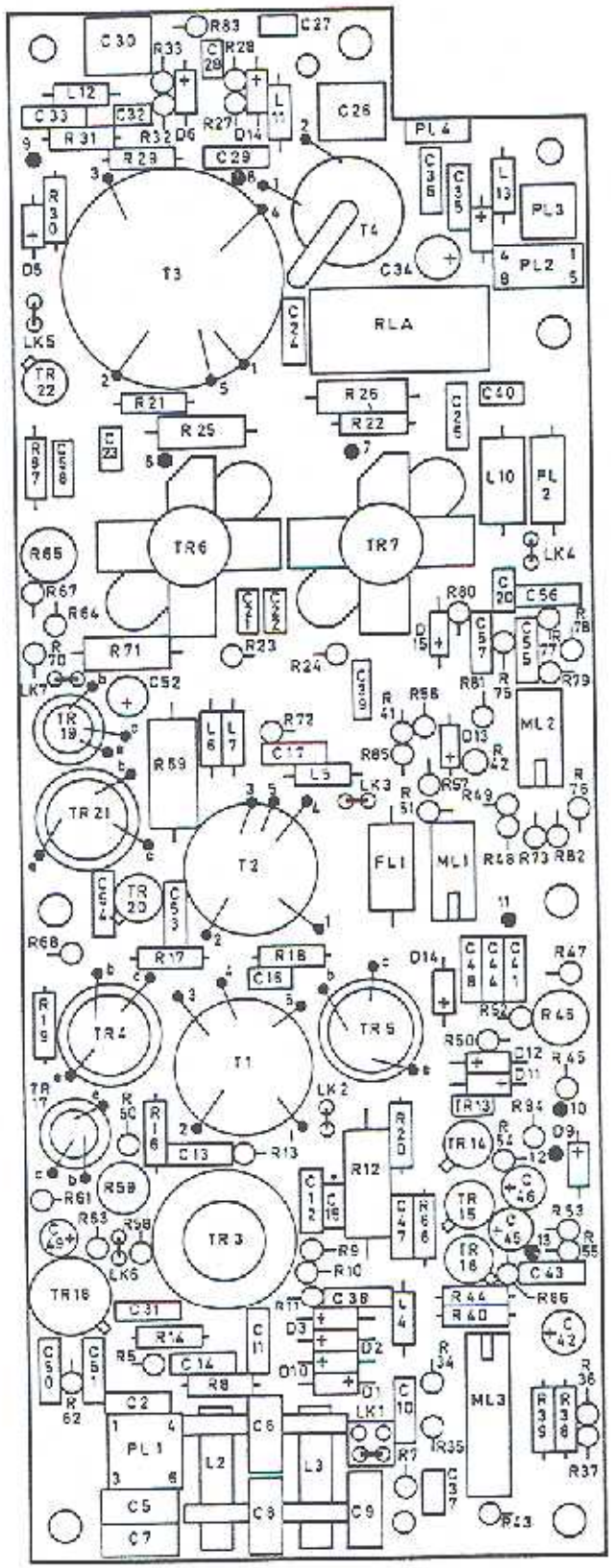
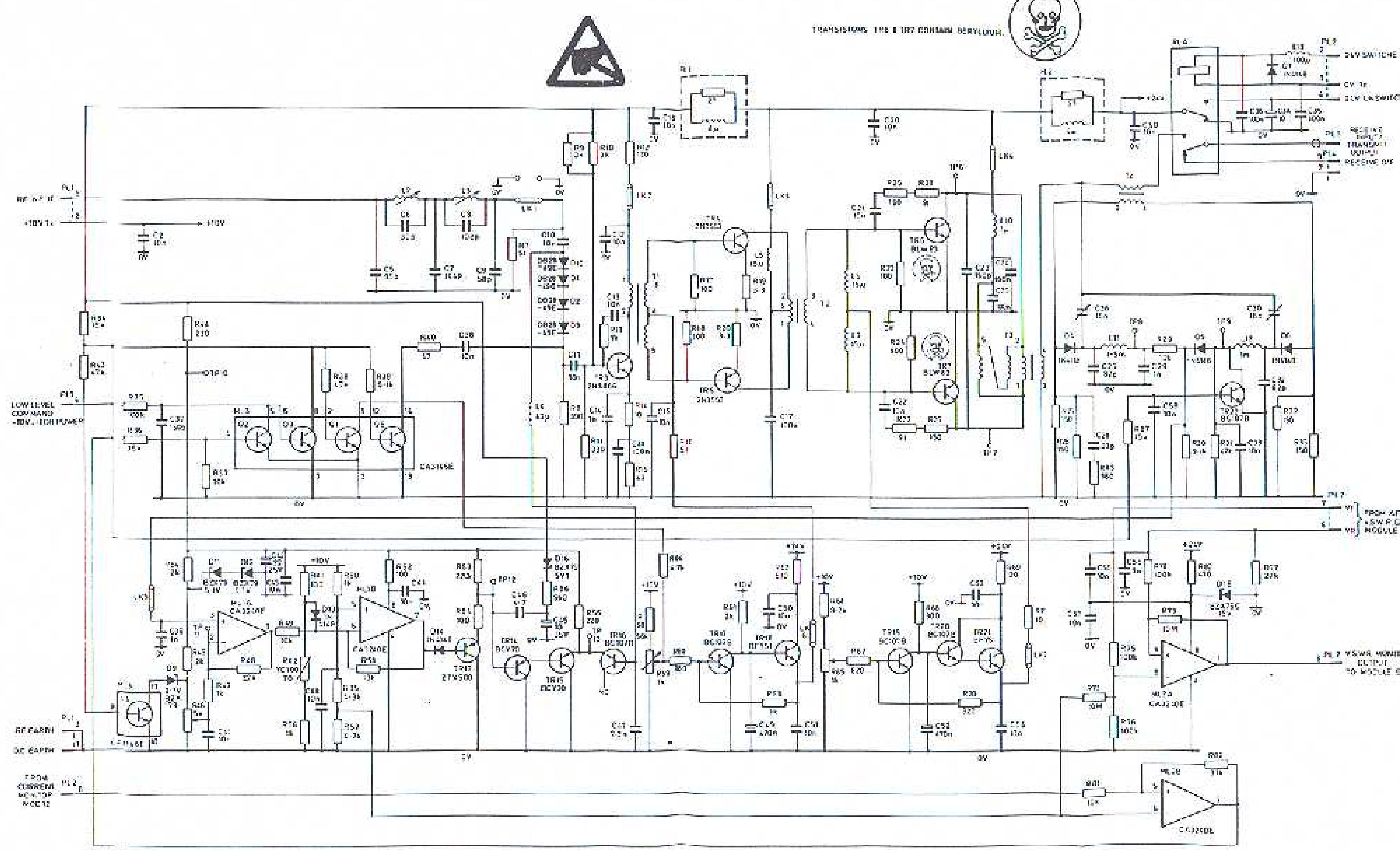


Fig 2 PA board – component layout



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WARNING: STATIC SENSITIVE DEVICES SHOULD ONLY BE HANDLED AFTER TAKING ANTI-STATIC PRECAUTIONS. MOVE OR STORE ASSEMBLY ONLY IN CONDUCTIVE PACKAGING. (REFER TO ITEMS LIST)

Fig. 1 Power amplifier board : circuit diagram

Oct 82

THIRD LINE SERVICING

OF

ANTENNA TUNING UNIT MODULE

(ATU BOARD 1 - 419/1/51231)

(ATU BOARD 2 - 419/1/69106)

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ILLUSTRATIONS

Fig.

1 ATU board 1 : circuit diagram
2 ATU board 2 : circuit diagram
3 ATU board 1 : component layout
4 ATU board 2 : component layout

TECHNICAL DESCRIPTION

Introduction

1. The Antenna Tuning Unit (ATU) module comprises two printed circuit boards designated ATU Board 1 and ATU Board 2 respectively. Electrical connection between the two boards is by board mounted six-way plug and socket connector (PL7 on Board 1 and SK10 on Board 2). The principal function of the ATU is to match the impedance of the radio antenna to 50 ohms at the transmission frequency in use.

2. Most of the circuitry is carried on the larger of the two boards, Board 1 and includes:

(a) an RF matching network which is tuned by switching bistable reed relays from an external microprocessor control,

(b) a phase detector,

(c) a conductance detector,

(d) a forward and reflected power monitor,

and (e) a current monitor.

3. On Board 2 is mounted a gas discharge overvoltage protection device and the board also carries an overflow of two additional capacitive matching elements and their switching relays.

Circuit description

4. Circuit diagrams for ATU Boards 1 and 2 are given in Figs.1 and 2 respectively.

Tuning

5. The principle of operation of the ATU circuit is as follows. At the start of a tune program all the inductance elements are switched into the RF path, and all the capacitive elements are disconnected. Inductive elements are then switched out of the RF path one at a time in accordance with the software program of an external microprocessor control. The inductors are removed in a sequence starting with the highest value of inductance, and this proceeds until a monitor circuit detects that the conductance of the RF path has fallen below 20 millimhos. The last inductor element removed is then reinserted, and the next smaller one removed, and so on until the conductance is as close to the 20 millimhos as the control switching can achieve. (NB. When conductance = 0.02 mhos, impedance (Z_o) = 50 ohms).

6. The next part of the tuning program is to tune out the inductive reactance of the circuit by inserting capacitance in parallel with the inductors. The capacitors are connected one at a time starting with the smallest values and this proceeds until the output of a phase detector circuit indicates to the external control that the phase relationship between voltage and current has changed from a positive value (inductive) to a negative value (capacitive). When this occurs the last capacitor element added is disconnected and the next smaller one is connected in its place, and the smaller capacitors are progressively added until an 'in phase' condition is achieved. The conductance detector and phase detector are set during manufacture with the RF path terminated by an impedance of 50 ohms to represent the antenna. Hence when 'tuning' is completed the characteristic impedance of the radio antenna is matched to this 'target' impedance of 50 ohms.

7. When the ANTENNA/50 ohm switch is set to 50 ohms the RF line is routed by RLA contacts 4 and 7 to the 50 ohm socket via PL2.

RF matching network (Figs.1 and 2)

8. Inductors L8 to L17 on ATU Board 1 can be switched in or out of the RF line by setting or resetting relays RLB to RLL respectively. Similarly capacitors C21 to C27, and C58 to C60 can be connected in parallel with the RF line to increase capacitance, or disconnected to reduce circuit capacitance, by setting or resetting relays RLM to RLV respectively.

9. Control of the relays is exercised over twenty SET and nineteen RESET lines from the external control (microprocessor). Only nineteen reset lines for the twenty relays because relays RLU and RLV on Board 2 share a common reset line. Relays are set or reset by an OV pulse on the relevant SET or

RESET line connected to PL6. Decoupling capacitors C28 to C45, C48 and C49 are necessary on the relays switching the inductor elements to counter any RF induced into the relay coils when the contacts are carrying, or breaking the RF current.

10. Capacitors C58 to C60 on Board 2 are connected to the RF line via SK10/6-PL7/6 and are only required in the following situations:

(a) at LOW frequencies, when the size of inductor required for loading to obtain a conductance less than 20 millimhos becomes too large to be accommodated in the space available. Capacitance is then introduced in parallel with the antenna load impedance to reduce the capacitive reactance of the load,

and (b) at MIDDLE frequencies where antenna resonant frequencies may be encountered.

11. Under the above conditions the external control first attempts to tune the antenna as described in paragraph 5, and if this is unsuccessful, the additional capacitance is switched into circuit, and the tuning program is repeated.

Conductance detector

12. The voltage developed across resistor R5 in the secondary circuit of transformer T2 is directly proportional to the RF line current in the primary winding; and the voltage appearing at the junction of capacitors C13, C14, and C51, with capacitor C9, is directly proportional to the RF line voltage. The circuit design is such that the relationship between the two voltages is 2Vpk(R5) = Vpk (C51/C9) for a terminating conductance of 20 mhos at PL5/1. The two ac voltages are summed and detected by D3 and D4 to produce a dc output voltage at the junction of R8/R9/R11 which will modify the standing voltage of +6V (from PL1/1) at this point.

13. The conductance detector circuit is preset (C13 and C14) to produce a zero change in the +6V dc level when the RF line is terminated by a load having an impedance of 50 ohms. (ie. conductance = 20 millimhos) when the load on the detector is the matching circuit plus the antenna the +6V will be modified by the dc voltage derived from the relative circuit conductance, in such a manner that the standing +6V decreases when the conductance is greater than 20 millimhos, and increases when the conductance is less than 20 millimhos. The resultant voltage is used to control the inverting input to comparator ML1A which refers it to a +6V reference voltage in its non-inverting input. The 680 kilohm feedback resistor R17 on ML1A makes the device very sensitive to any changes on the inverting input above or below the +6V reference level. Hence when the conductance is greater than 20 millimhos the output of ML1A goes to logic 1 (+10V) and conversely when the conductance is less than 20 millimhos, the output goes to logic 0 (0V). Inductance L5 provides phase correction to compensate for the phase shift introduced by the transformer windings.

Phase detector

14. The voltage developed across resistor R19 is directly proportional to the RF line current in the primary of transformer T4, and the voltage developed across R21 and L7 is proportional to, but in quadrature phase with, the line

voltage. These voltages are summed and detected in a bridge circuit which is preset (R22) to give a null change to the standing dc voltage of +6V when the line voltage and current are in phase.

15. When the line current is lagging line voltage, indicating an inductive load, the effect is to increase the standing dc voltage on the inverting input of comparator ML1B producing a negative swing in the output of this device. Conversely when the line current is leading line voltage (capacitive load) the effect is to decrease the standing voltage into the comparator, producing a positive swing in the output of same. The non-inverting input to ML1B is connected to a +6V reference voltage, and the 680 kilohm feedback resistor R18 makes ML1B very sensitive to changes in level occurring at the inverting input above or below the +6V reference level. Hence when the load is capacitive and the inverting input drops below +6V the output of the device goes to logic 1 (10V); and when the load is inductive and the inverting input rises over +6V the output of the device goes to logic 0 (0V).

16. Inductor L7 provides phase correction to compensate for phase shift introduced by the windings of transformer T1.

Forward and reflected power monitor

17. The incoming RF signal is coupled to the forward and reflected power monitor by transformer T1 and capacitors C2 and C4. The voltage developed across R1/R2 and R3/R4 is proportional to the line current sampled by T1, and the RF voltages developed across C3 in the 'reflected', and C5 in the 'forward' sections of the monitor, are directly proportional to the line voltage. The two coupled RF voltages are summed and rectified by D1 and D2 and the magnitude of the resultant dc voltages appearing at the junctions L1/C1 and L2/C6 are proportional to the reflected and forward powers respectively.

18. The dc voltage derived in the reflected coupler is preset by adjustment of capacitor C2 so that when the forward direction of transmission is correctly terminated by a 50 ohm impedance, the dc voltage at L1/C1 is a minimum. Similarly in the reverse direction of transmission, with the normal RF inputs (PL3) terminated on a 50 ohm impedance and RF injected at PL2, C4 is adjusted for a dc voltage minimum at L2/C6. Hence the relationship between the two dc voltage levels produced by the monitor circuit is analogous to the ratio between the levels of forward and reverse power. The outputs of the monitor are connected to board output pins PL1/10 and PL1/9 for connection to an external VSWR detector.

Current monitor

19. The outgoing RF line current to the antenna is routed through the primary of transformer T5. The RF voltage induced in the secondary circuit of T5 is detected by D7; the resultant dc voltage developed across R27 gives an analogue output on PL8/1 which is directly proportional to the peak value of line current flowing. This output is used to operate an externally connected CURRENT TRIP circuit if the line current is excessive.

Overvoltage protection (Fig.2)

20. The gas discharge surge arrestor on ATU Board 2 strikes at 3500V to protect the radio circuits from damage which could be caused by the high voltage induced by transmitting with an unmatched load or other fault condition.

Testing and alignment

21. Testing and alignment information for this board will be found in Part 4 in this volume.

COMPONENTS LIST

22. The principal component parts of the Antenna Tuning Unit module are ATU Board 1 (419/1/51231), and ATU Board 2 (419/1/69106). The principal component parts of the two boards are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
BOARD 1			(419/1/51231)
	CAPACITORS		
C1,6,17, 18,50	10nF 10% 100V	BS9075 F0034 type E2C1	400/4/20673/002
C2,4	3.5-16.5pF (Variable) 50V	BS9093 F016 CD5/20	401/4/14446/005
C3,5	150pF 10% 100V		400/4/21690/150
C7,11, 20,46, 47	68nF 10% 63V	Arcotronics 1-68	435/4/90829/015
C8	300pF 1% 125V	ITT 454-49-125-300-1%	438/4/25904/036
C9	180pF 1% 125V	ITT 454-49-125-180-1%	438/4/25904/031
C10,12, 15,19	10nF 10% 63V	Arcotronics 1-68	435/4/90829/023
C13	0.9-1.1pF (Variable) 100V	BS9093 F016 CD5/2	401/4/14446/001
C14	3.5-21.5pF (Variable) 50V	BS9093 F016 CD5/25	401/4/14446/006
C16	12pF 2% 400V	Resista RCL608P/630V	400/4/21281/003
C21	37pF ± 1pF 400V	BS9070 N002	438/4/25351/370
C22	18pF ± 1pF 400V	BS9070 N002 C2AED-C	438/4/25351/180
C23	79pF ± 1pF 400V	BS9070 N002 C2AED-C	438/4/25351/790
C24	171pF 1% 400V	BS9070 N002 C2AED-C	438/4/25352/171
C25	350pF 1% 125V	ITT 454-49-125-350-1%	438/4/25904/085
C26	813pF 1% 125V	ITT 454-49-125-813-1%	438/4/25904/068
C27	1.71nF 1% 400V	ITT 454-52-400-1N71-1%	438/4/25907/058
C28-43, 52,53	330pF 2% 100V	Mullard 632-58331	400/4/20674/028
C44,45, 48,49	2.2nF 20% 100V	Wima FKS2	435/4/90821/003
C51	15pF 2% 100V	Mullard 632-10159	400/4/20674/012
	RESISTORS		
R1-4	75 ohm 2% 0.25W	Metal oxide film	403/4/05521/750
R5	47 ohm 2% 0.5W	Metal oxide film	403/4/05321/470
R6	100 ohm 2% 0.25W	Metal oxide film	403/4/05522/100
R7,9	1k 2% 0.25W	Metal oxide film	403/4/05523/100
R8	4.7k 2% 0.25W	Metal oxide film	403/4/05523/470

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
R10,13-16	2k 2% 0.25W	Metal oxide film	403/4/05523/200
R11	2.7k 2% 0.25W	Metal oxide film	403/4/05523/270
R12,23	10k 2% 0.25W	Metal oxide film	403/4/05524/100
R17,18	680k 2% 0.25W	Metal oxide film	403/4/07149/680
R19	51 ohm 2% 0.25W	Metal oxide film	403/4/05521/510
R20,24	2.4k 2% 0.25W	Metal oxide film	403/4/05523/240
R21	330 ohm 2% 0.25W	Metal oxide film	403/4/05522/330
R22	5k 5% 0.75W (Variable)	Bourns 3290W	404/4/07943/500
R25	47 ohm 2% 1.00W	Metal oxide film	403/4/05221/470
R26	5.6 ohm 2% 0.25W	Metal oxide film	403/4/07148/560
R27	47k 2% 0.25W	Metal oxide film	403/4/05524/470
	INDUCTORS (RF)		
L1,2	1mH 10%	BS9751 N0001 Patt.A	406/4/32161/049
L3	15uH 10%	BS9751 N0001 Patt.A	406/4/32161/027
L4,6	47uH 10%	BS9751 N0001 Patt.A	406/4/32161/033
L5	Variable		406/1/32279
L7	0.68uH 10%	BS9751 N0001 Patt.A	406/4/32161/011
L8	Variable		406/1/32158/006
L9	Variable		406/1/32158/005
L10	Variable		406/1/31844/032
L11	Variable		406/1/31844/031
L12	Variable		406/1/31844/030
L13	Variable		406/1/32250/001
L14	Variable		406/1/32250/002
L15	Variable		406/1/32159/003
L16	Variable		406/1/32159/002
L17	Variable		406/1/32159/001
	MISCELLANEOUS		
ML1	Integrated circuit operational amplifier	SE532N (Burnt-In)	445/4/03279/002
D1-D7	Diode	IN4148	415/4/98869
RLA,B,C, D,E,F, G,H,J, M,N,P, Q,R,S, T	Reed relay 2700 ohm 24V	Thorn RSL2-24	507/4/05183/003
RLK,L	Reed relay 500 + 500 ohm	R09-0994	507/9/38464 406/4/32161/009
T1	Transformer RF		406/1/32276
T2,5	Transformer RF		406/1/31851
T3	Transformer RF		406/1/31853
T4	Transformer RF		406/1/31852

continued ...

COMPONENTS LIST continued ...

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
PL2	Plug 50 ohm	Radiall R114.426	508/4/24190
PL3	Cable RF assy. incl. plug		630/1/42961
PL6	Connector		508/9/24125/020
PL7	Connector	Type 75160-109-7	630/1/48818
BOARD 2			(419/1/69106)
	CAPACITORS		
C54	68nF 20% 50V	Wima MKS2	435/4/90829/015
C55-57	2.2nF 20% 100V	Wima MKS2	435/4/90821/003
C58,59	47pF 5% 500V	Vitramon VY81C390J	400/4/21318/017
C60	42pF ± 1pF 400V	ITT 454-49-400-42pF-1%	435/4/90829/015
	MISCELLANEOUS		
RLU,V	Relay 500 + 500 ohm	R09-0994	507/9/38464
SC1	Surge arrestor	Reynolds NLH2000L	516/4/00463/007
SK10	Socket	Berg 75302-001	508/4/22131

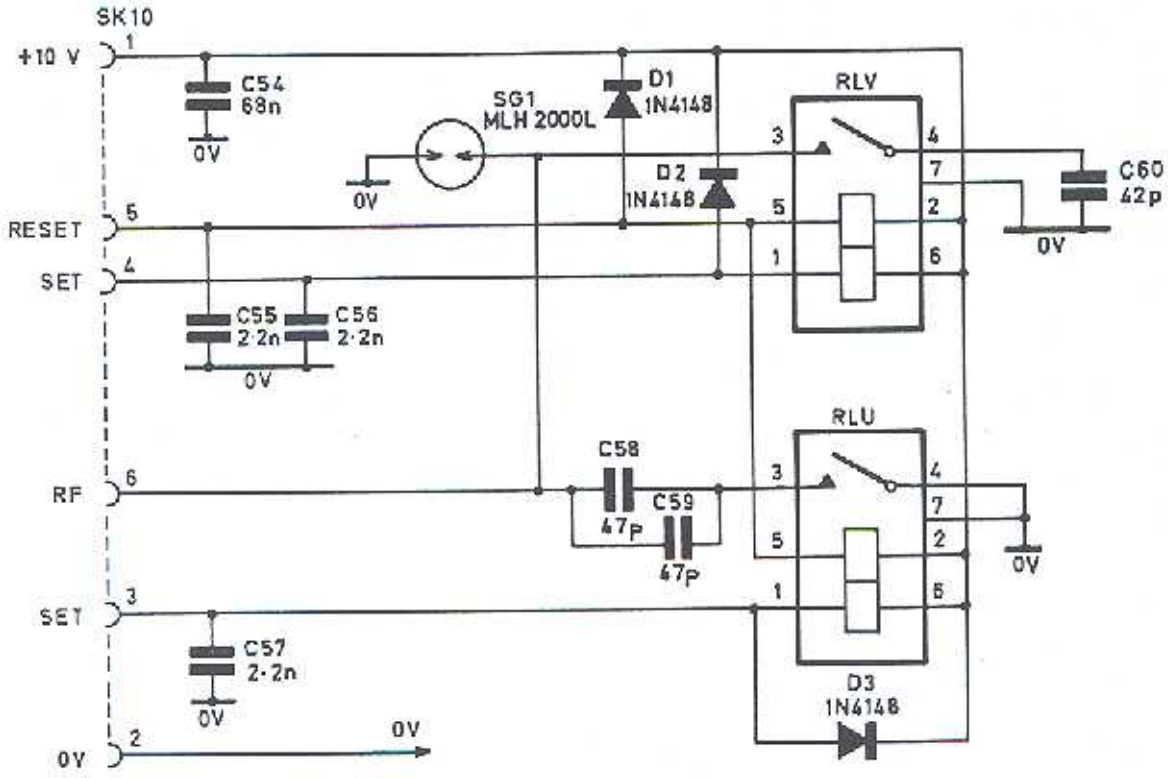

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Fig.2 ATU board 2 : circuit diagram

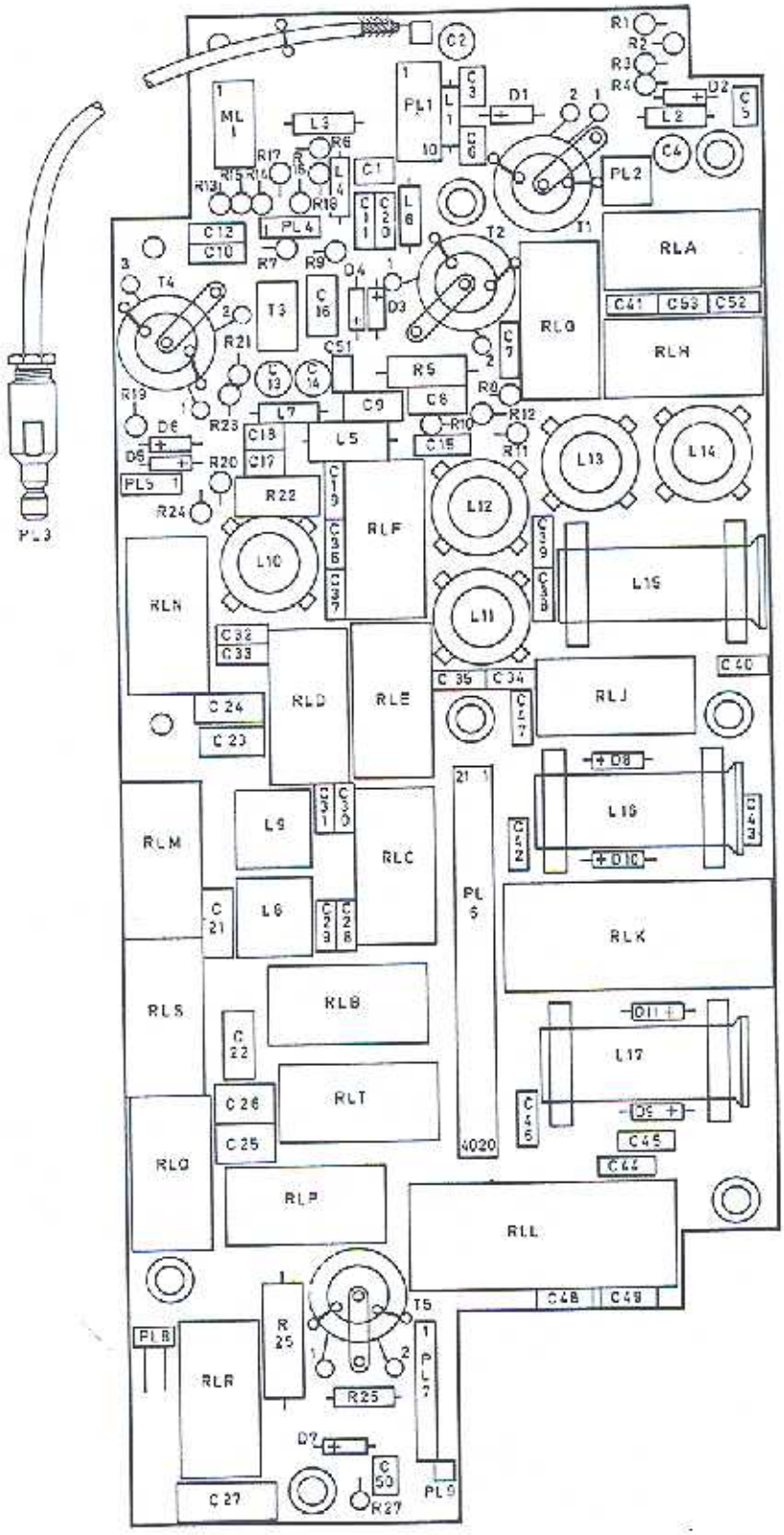

Fig 3 ATU board 1 – component layout

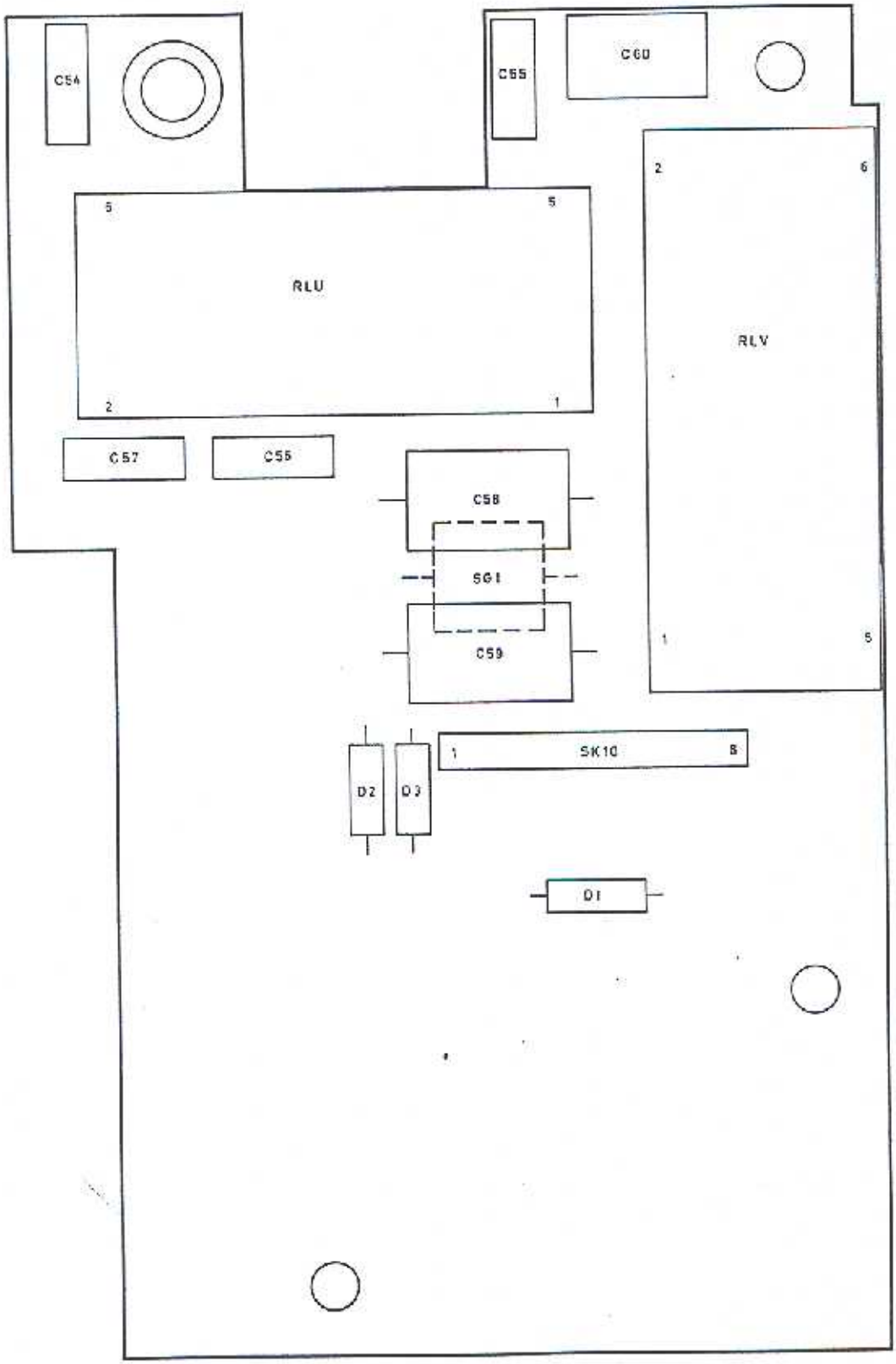

Fig 4 ATU board 2 – component layout

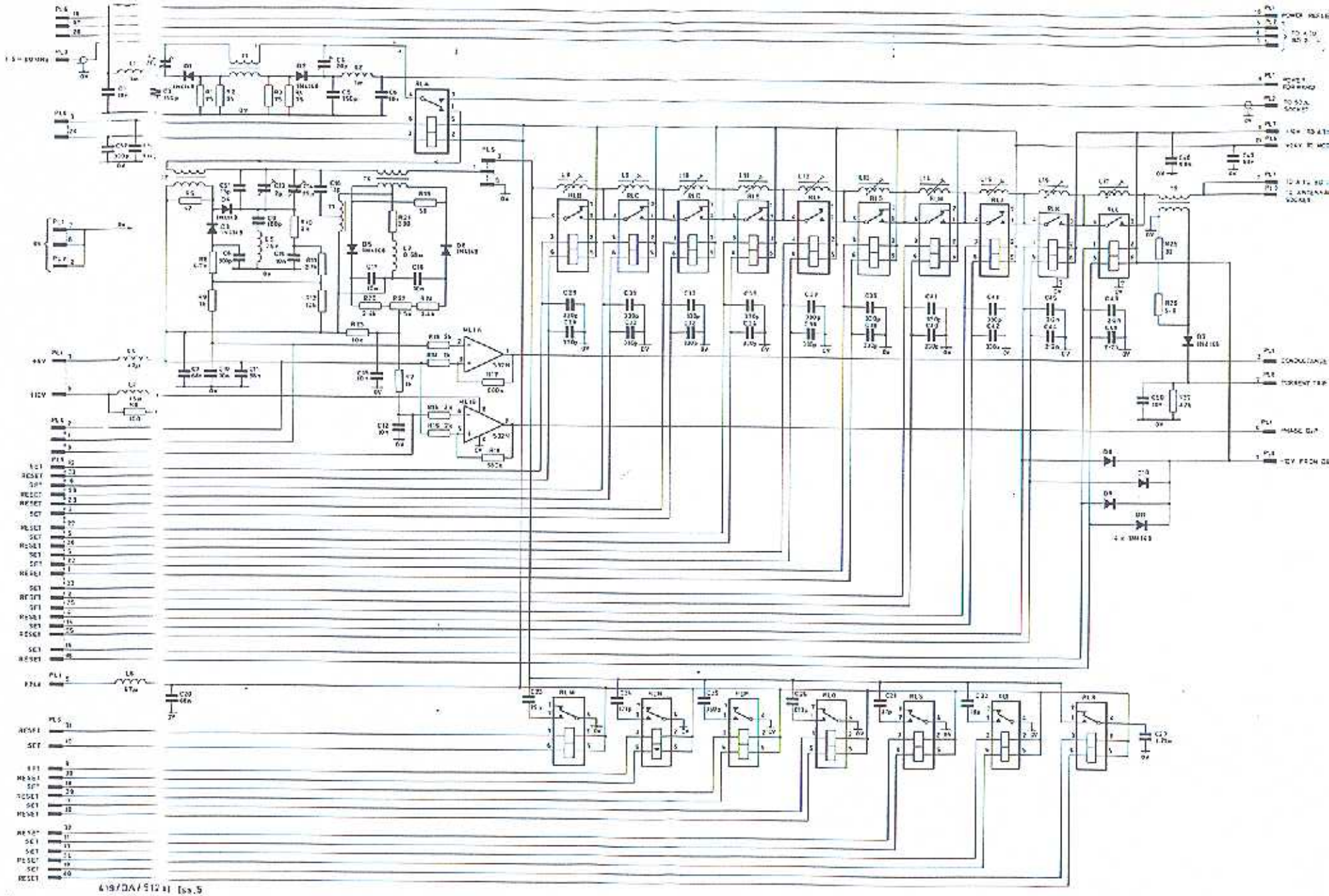

Fig. 1 ATU board 1 : circuit diagram

THIRD LINE SERVICING

OF

FILTER BOARD - FRONT 419/1/66402

CONTENTS

	Para.
Technical description	1
Testing and alignment	3
Components list	4

ILLUSTRATIONS

Fig.
1 Filter board - front : circuit diagram
2 Filter board - front : component layout

TECHNICAL DESCRIPTION

1. The Filter Board is equipped with bead ferrite inductors and ceramic capacitors to provide decoupling of ancillary equipment connected to the front panel connectors on the radio. A circuit diagram of the board is given in Figure 1.

2. Diode D1 limits the voltage at output PL1/3 (WRITE INPUT) to 10V and R1 limits the current drawn by that output to less than 3 mA.

TESTING AND ALIGNMENT

3. Testing of the Filter Board is covered in Part 4 of this manual. There are no alignment adjustments.

COMPONENTS LIST

4. The principal component parts of Filter Board 419/1/66402 are:

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
C1-6	Capacitor 10uF 20%	BS9075 (ceramic)	400/4/21712/100
L1-8, 10-12	Ferrite bead iductor	Mullard FX1115/A1	905/9/98000
D1	Diode V reg. 10V 5%	BZX79-C10	415/4/05830/016
R1	Resistor 3.9k 2% 0.125W	Metal oxide film	403/4/07181/392
F1	Fuse 0.75A	Littlefuse 275/0.75A	518/4/90467/006
SK2,3	Socket 7-way	Amphenol 62GB/5016/10/7SF	508/4/24131/001

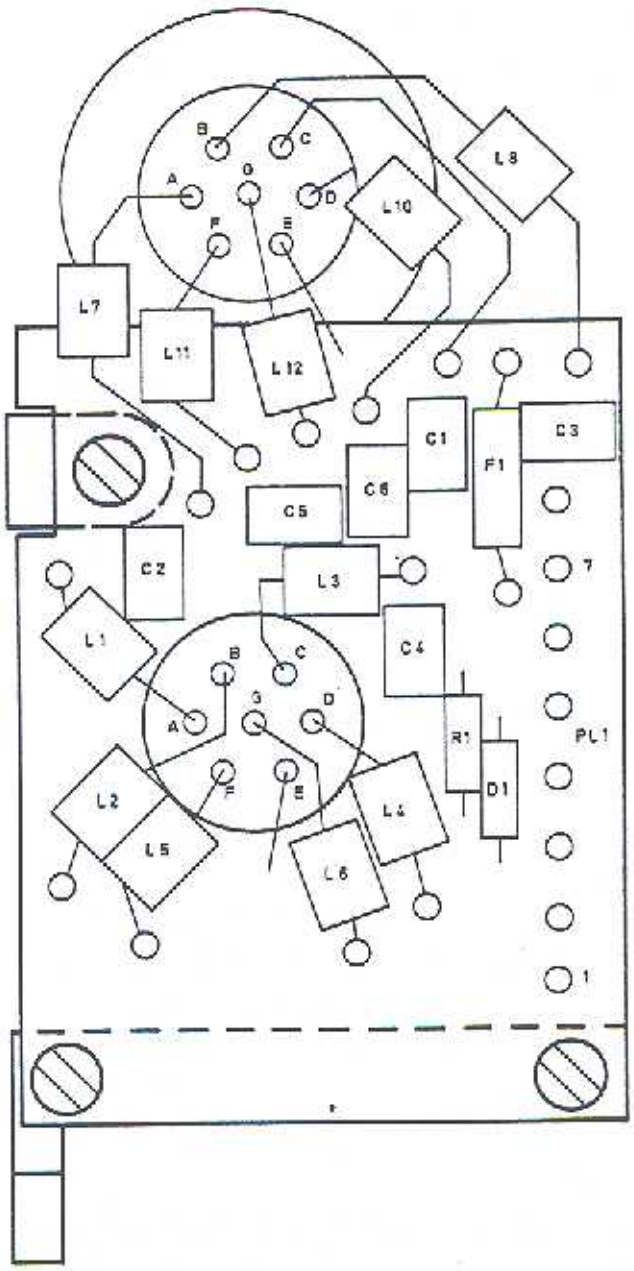

Fig 2 Filter board (front) – component layout

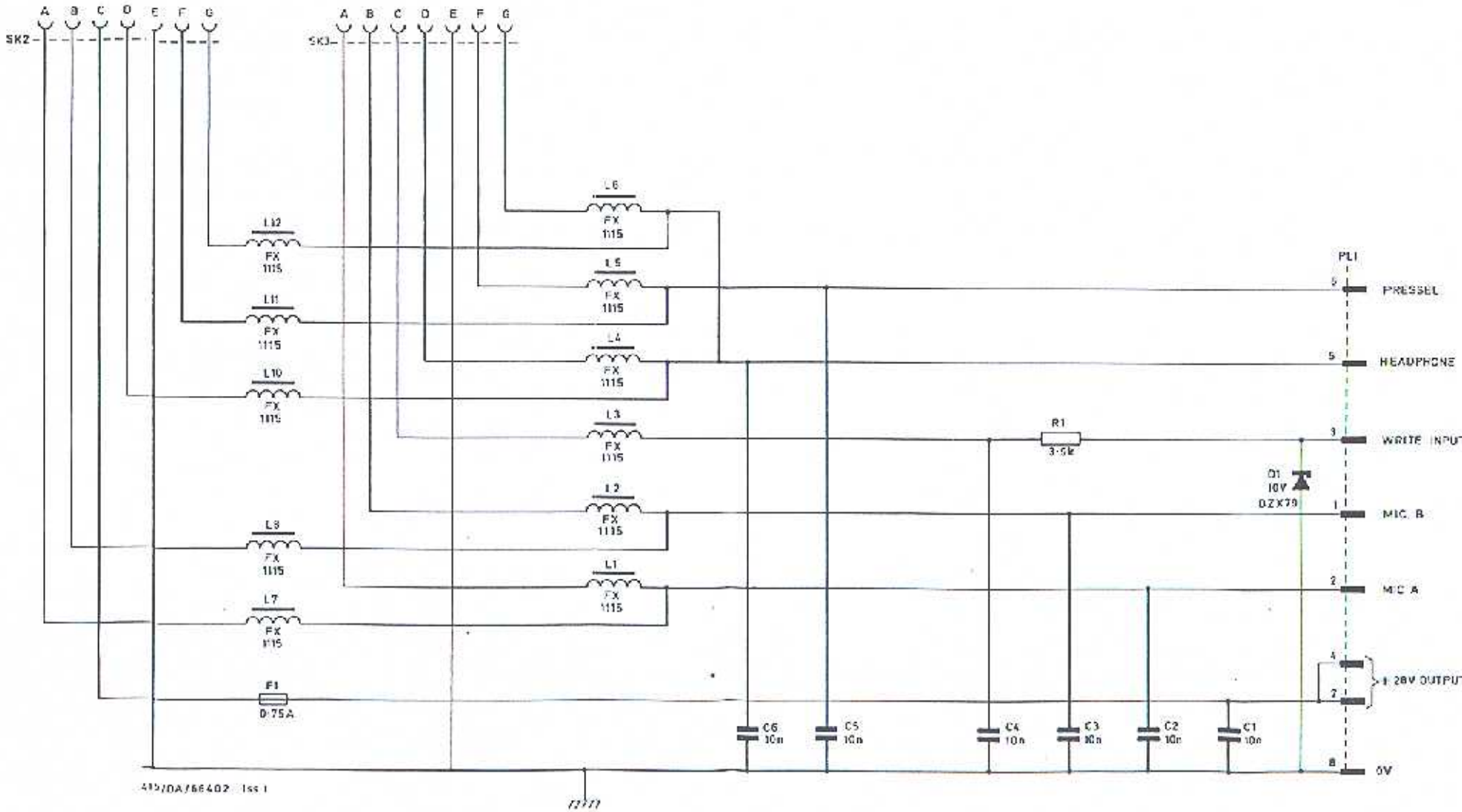

Fig 1

Filter board-front : circuit diagram

Fig

Oct. 82

THIRD LINE SERVICING

OF

PRC420 HF TRANSCEIVER

APPENDIX 1

HAND HELD CHANNEL SELECTOR PV2319

CONTENTS

	Para.
Introduction	1
Construction	2
Circuit description	3
Testing	
Test equipment required	7
Test procedure	8
Servicing and repair	10
Repainting	13
Components list	14

ILLUSTRATIONS

Fig.
A1/1 PV2319 hand held channel selector
A1/2 PV2319 hand held channel selector : circuit diagram
A1/3 PV2319 : wiring diagram

INTRODUCTION

1. The hand held channel selector permits an operator who is equipped with a PRC420 Transceiver in a manpack configuration to have remote control of channel selection, signal volume, and pressel operation. It is a sealed unit which can be hand held or fitted to a webbing harness. It plugs into the ANCILLARIES socket on the rear panel of the radio, and the unit has a seven-way socket for connection of a standard headset, handset, or telegraph key.

CONSTRUCTION

2. The unit consists of a cast aluminium alloy case on which are mounted two rotary switch controls (volume and channel selector), and a pushbutton switch which operates as a pressel. The case has a removable cover underneath, with a gasket fitted between cover and case to form an airtight seal. The physical layout of the unit is shown in Fig.A1/1.

CIRCUIT DESCRIPTION

3. A circuit diagram of the unit is given in Fig.A1/2.

4. Each setting of the nine-position channel select switch S2 connects the corresponding 4-bit BCD code for each channel to the REM CHANNEL outputs PL5/G, H, J and K as follows:-

Switch Position	Channel	Connector Terminal G (MSB)	H	J	K (LSB)
1	SYNTH	1	1	1	1
2	1	1	1	1	0
3	2	1	1	0	1
4	3	1	1	0	0
5	4	1	0	1	1
6	5	1	0	1	0
7	6	1	0	0	1
8	7	1	0	0	0
9	8	0	1	1	1

5. Having selected a channel the operator has the option of initiating a tune cycle in the transceiver by operating pushbutton PBS1, or operating the headset pressel in the usual manner. Use of the pushbutton allows transmission to be effected without use of a handset or pressel box.

6. Resistors R1 to R9 form a voltage divider between the receiver audio signal on PL5/D and ground. Wafer A of the volume control S1 taps an increasing level of audio signal voltage for the headset receiver as the control is rotated in a clockwise direction. As the volume is increased resistors R10 to R15 reduce the line current to the headset microphone, to limit the audio input to the transceiver.

TESTING

Test equipment required

7. One multimeter with resistance ranges 0-200 ohms; 0-2 kilohms; and 0-20 kilohms. Accuracy should be $\pm$ 1%.

Test procedure

8. Proceed as follows:

(1) Short circuit SK2/A and SK2/B with a wire link.

(2) Set the multimeter on the 20 kilohm range and measure the resistance between PL5A and PL5B is within the following limits:-

Volume Switch Position	Resistance (kilohms)
10 (max.) and 9	6.3 - 7.1
8, 7 and 6	2.16 - 2.44
5, 4 and 3	0.620 - 0.700
2 and 1 (min.)	0 (less than 1 ohm)

(3) Remove link from SK2A and SK2B.

(4) Connect the multimeter to SK2/D and PL5/D. Set the range to 0-2 kilohms.

(5) Check the resistance measured on the meter for each setting of the volume control is within the following limits:-

Volume Switch Position	Resistance (ohms)
10 (max.)	0 (less than 1 ohm)
9	63 - 72
8	177 - 199
7	384 - 432
6	553 - 623
5	630 - 710
4	661 - 745
3	675 - 761
2	681 - 768
1 (min.)	684 - 772

(6) Disconnect the multimeter.

9. To test the operation of the channel selector switch (S2), the unit under test should be plugged into the ANCILLARIES (SK5) connector of a PRC420 transceiver known to be in good working order. The frequency of each preset channel of the PRC420 should be noted by selecting each channel in turn using the controls on the front panel of the radio. Set the channel select switch on the front panel of the radio to EXTERNAL and, selecting each channel in turn on the hand held channel selector, operate pushbutton PBS1 and check that the correct frequency is displayed on the radio for each channel selected.

SERVICING AND REPAIR

10. The cover on the unit is secured by four M3 slotted screws. It should be noted that the sealing of the unit against the environment is jeopordised when the cover is removed.

11. The knobs on the rotary switches can be removed by undoing the 6BA hexagon grub screws securing them to the spindle.

12. After effecting any repairs necessary the unit should be retested in accordance with paras.7 to 9 before being passed as serviceable.

REPAINTING

13. Retouching of damaged surfaces may be carried out, but not the repainting of a complete unit, only the following paints should be used:

(1) Paint, priming, DTD5555.

(2) Paint, finishing, DTD5555, colour deep bronze green to BS381C No.224.

COMPONENTS LIST

14. The principle component parts of the Hand Held Channel Selector (630/1/42795) which may be required for repair are:-

Circuit ref.	Description & Tolerance	Manufacturer & Ref.	Plessey Part No.
	Base, insert assembly (case)		630/1/42797
	Cover		630/2/39036
	Screw, M3x8 (securing cover)		991/9/11854/002
	Knob (for rotary switches)		630/2/37208/001
	Knob, black (for PBS1)		418/9/44489/003
	Screw, grub (securing knobs)		999/4/31542/004
	Seal		630/2/39037
SK2	Socket, 7-way, 5A	Style CC1301-10-7SF	508/4/20931/035
PL5	Plug, 10-way, 5A (Note: Plug PL5 complete with 12-wire cable as an assembly is Plessey Part No. 705/1/14335)	Bendix PT08E-12-10P	508/4/22093/011
PBS1	Pushbutton switch, 2A	Honeywell 8P1-02-1-B	408/4/51526
S1	Switch, rotary, 3-pole	71AY231748	408/9/51536
S2	Switch, rotary, BCD, 9-position	71AY231747	408/9/51535
	RESISTORS		
R1	3.3 ohms 5% 0.33W	Carbon film	403/4/78482/014
R2	6.8 ohms 5% 0.33W	Carbon film	403/4/78482/069
R3	15 ohms 5% 0.2W	Carbon film	403/4/78596/002
R4	33 ohms 5% 0.2W	Carbon film	403/4/78596/006
R5	82 ohms 5% 0.2W	Carbon film	403/4/78596/011
R6	180 ohms 5% 0.2W	Carbon film	403/4/78596/015
R7	220 ohms 5% 0.2W	Carbon film	403/4/78596/016
R8	120 ohms 5% 0.2W	Carbon film	403/4/78596/013
R9	68 ohms 5% 0.2W	Carbon film	403/4/78596/010
R10,13	330 ohms 5% 0.2W	Carbon film	403/4/78596/018
R11,14	820 ohms 5% 0.2W	Carbon film	403/4/78596/023
R12,R15	2.2k ohms 5% 0.2W	Carbon film	403/4/78596/028

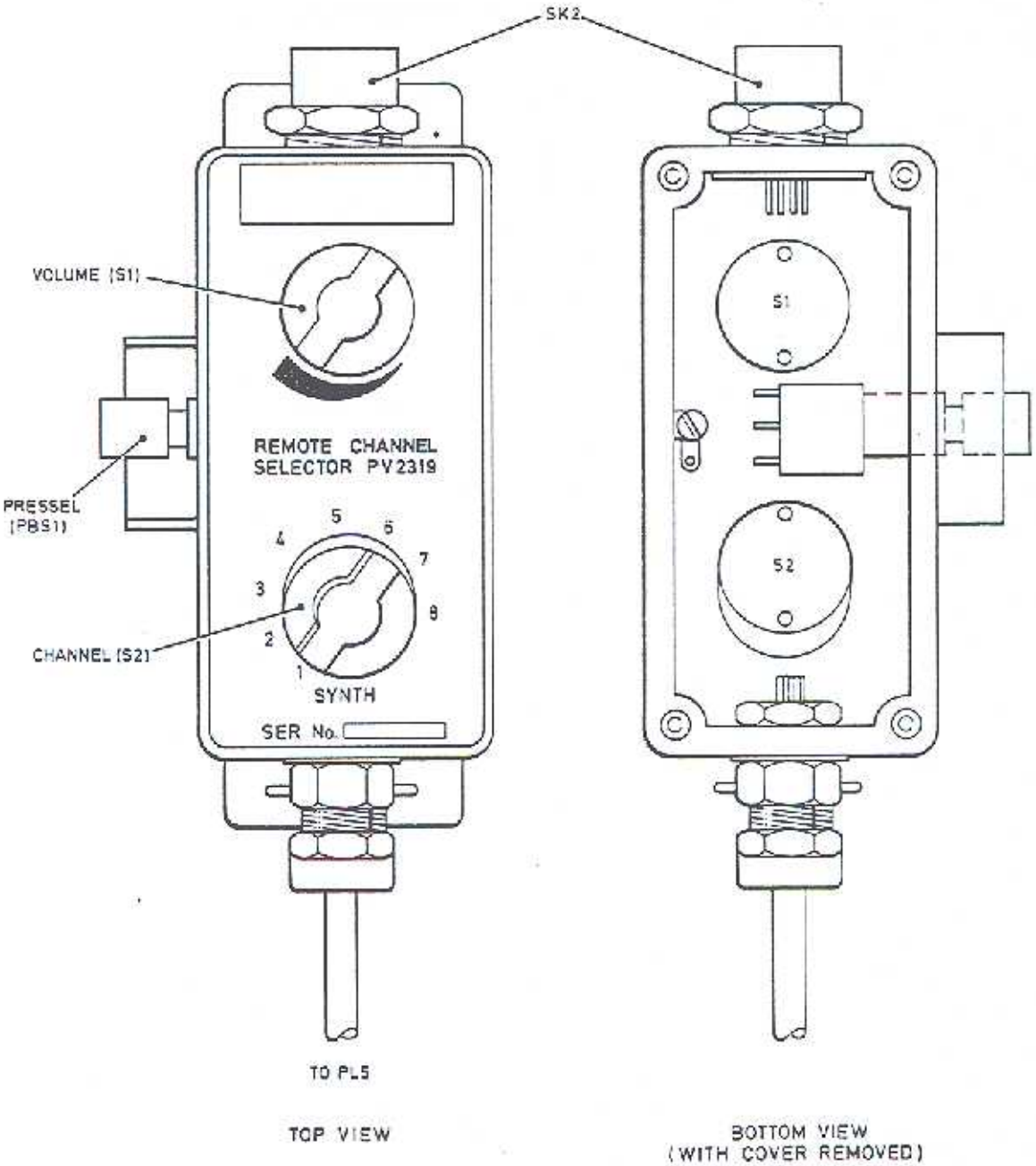

Fig. A1/1 PV2319 : Handheld channel selector

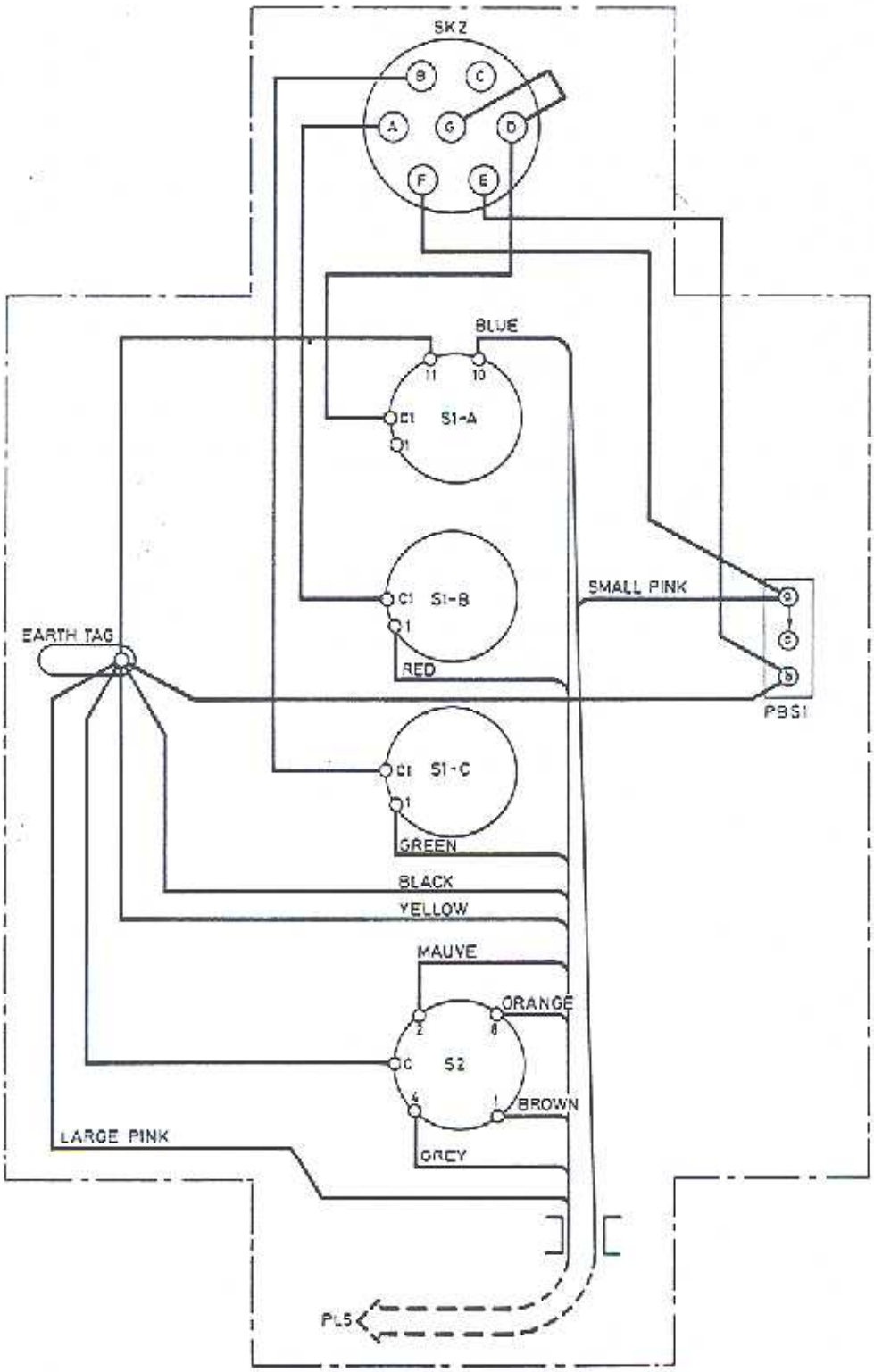

Fig. A1/3 PV2319 : Handheld channel selector - wiring diagram

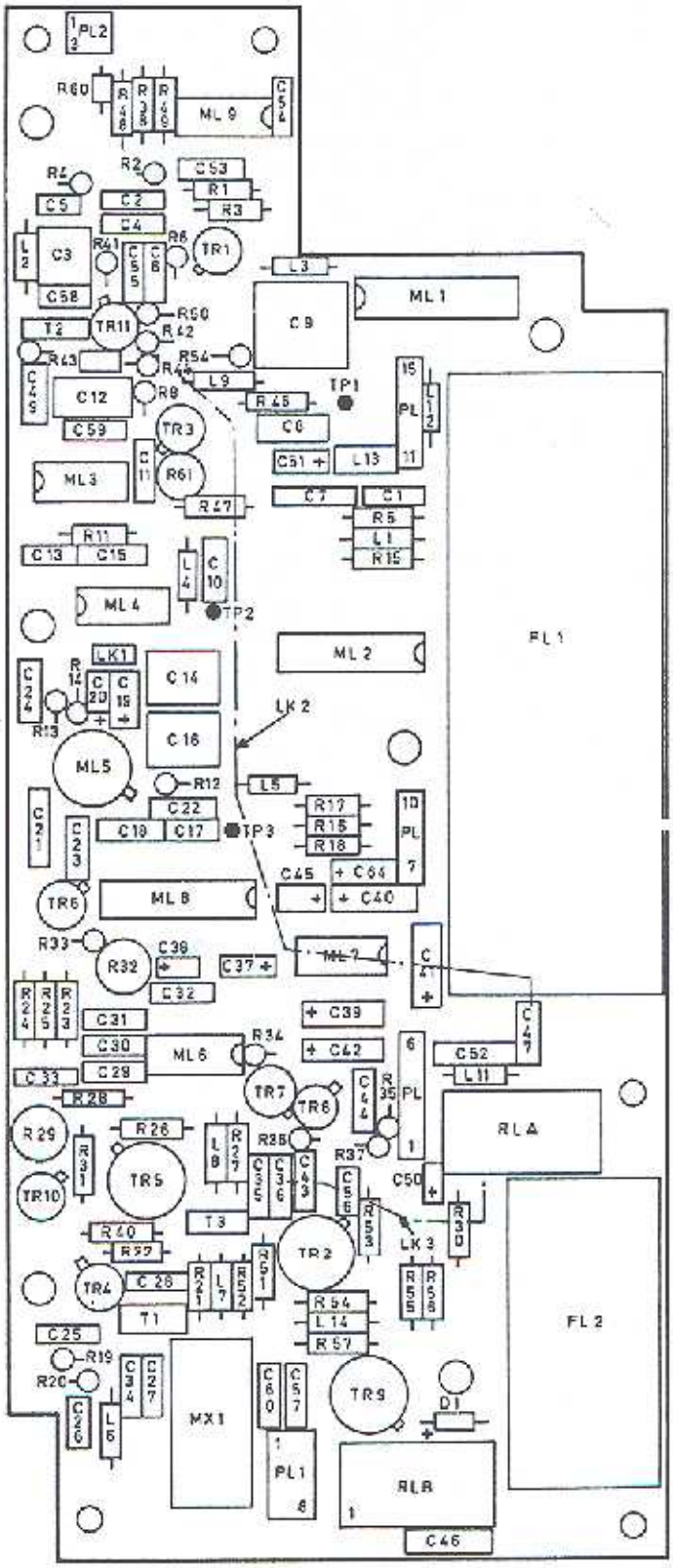

Fig 2 I.F board – component location

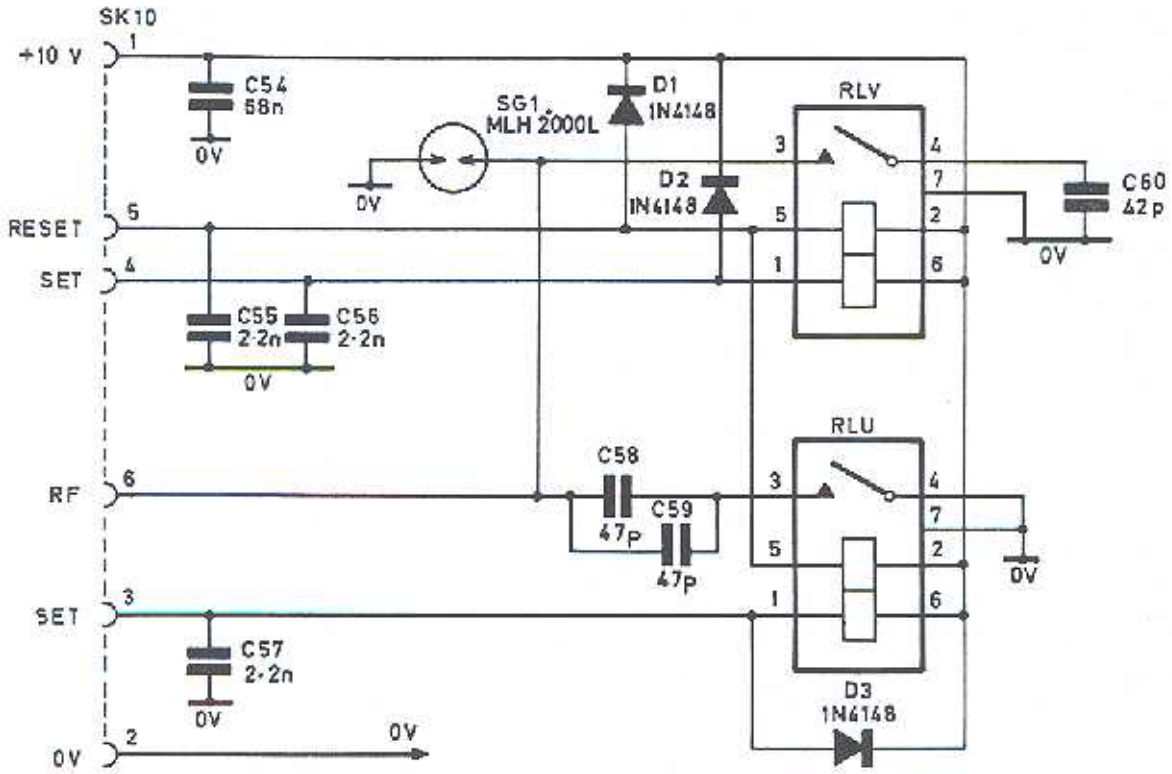

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Fig.2 ATU board 2 : circuit diagram

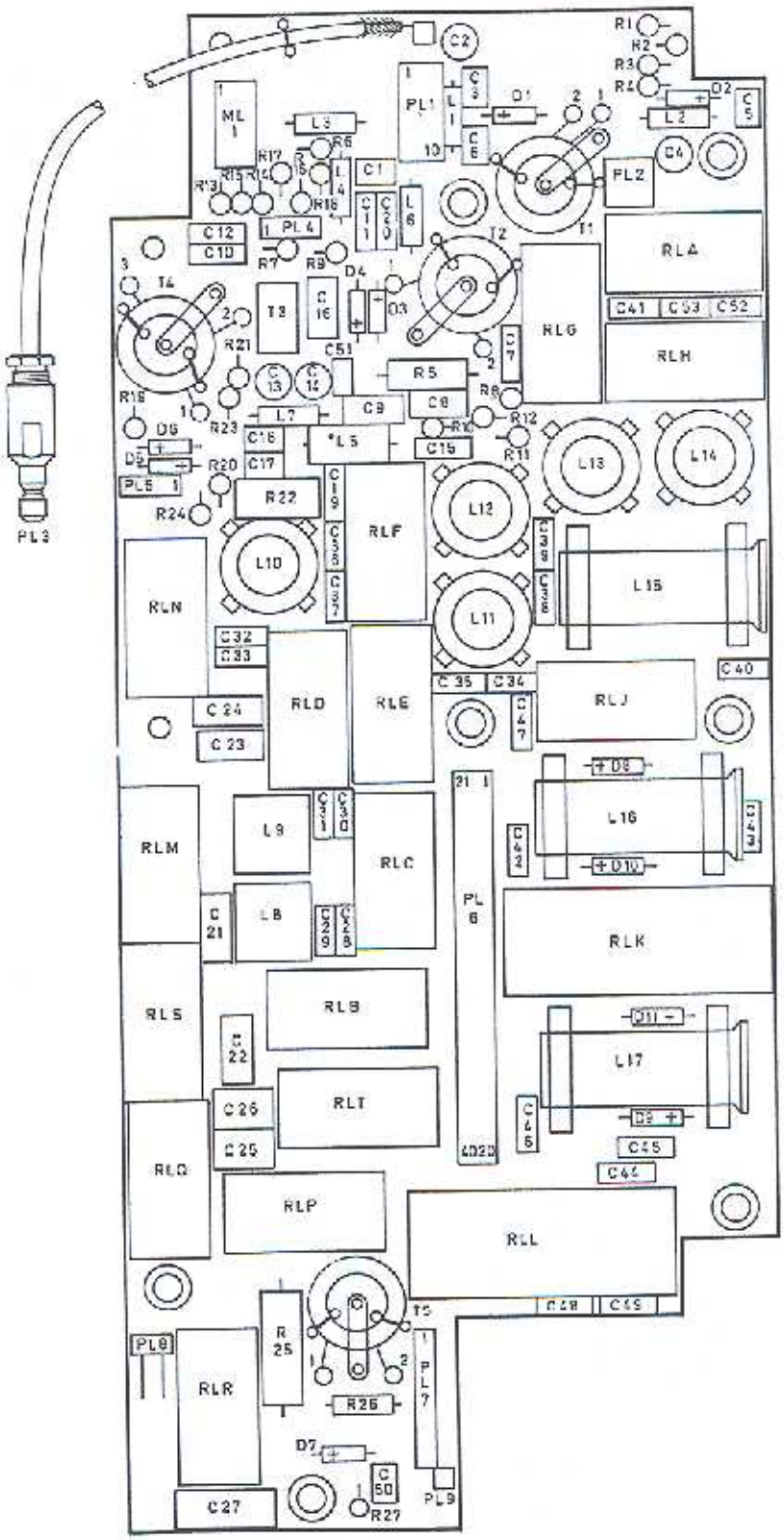


Fig 3 ATU board 1 - component layout

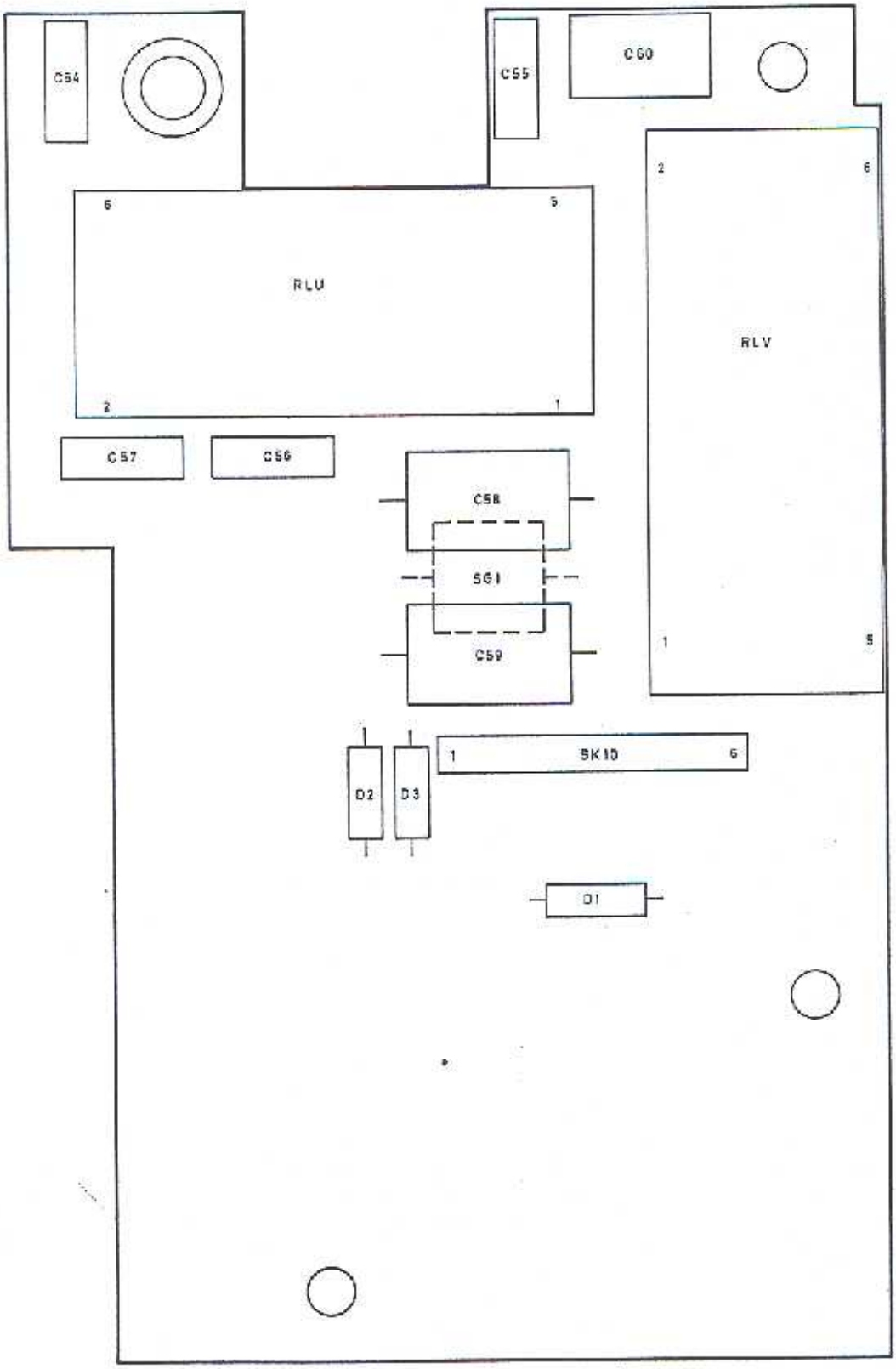
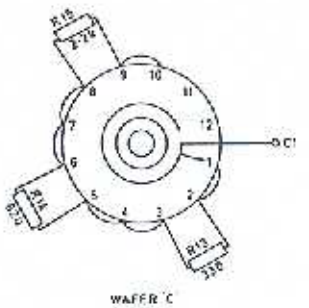


Fig 4 ATU board 2 – component layout



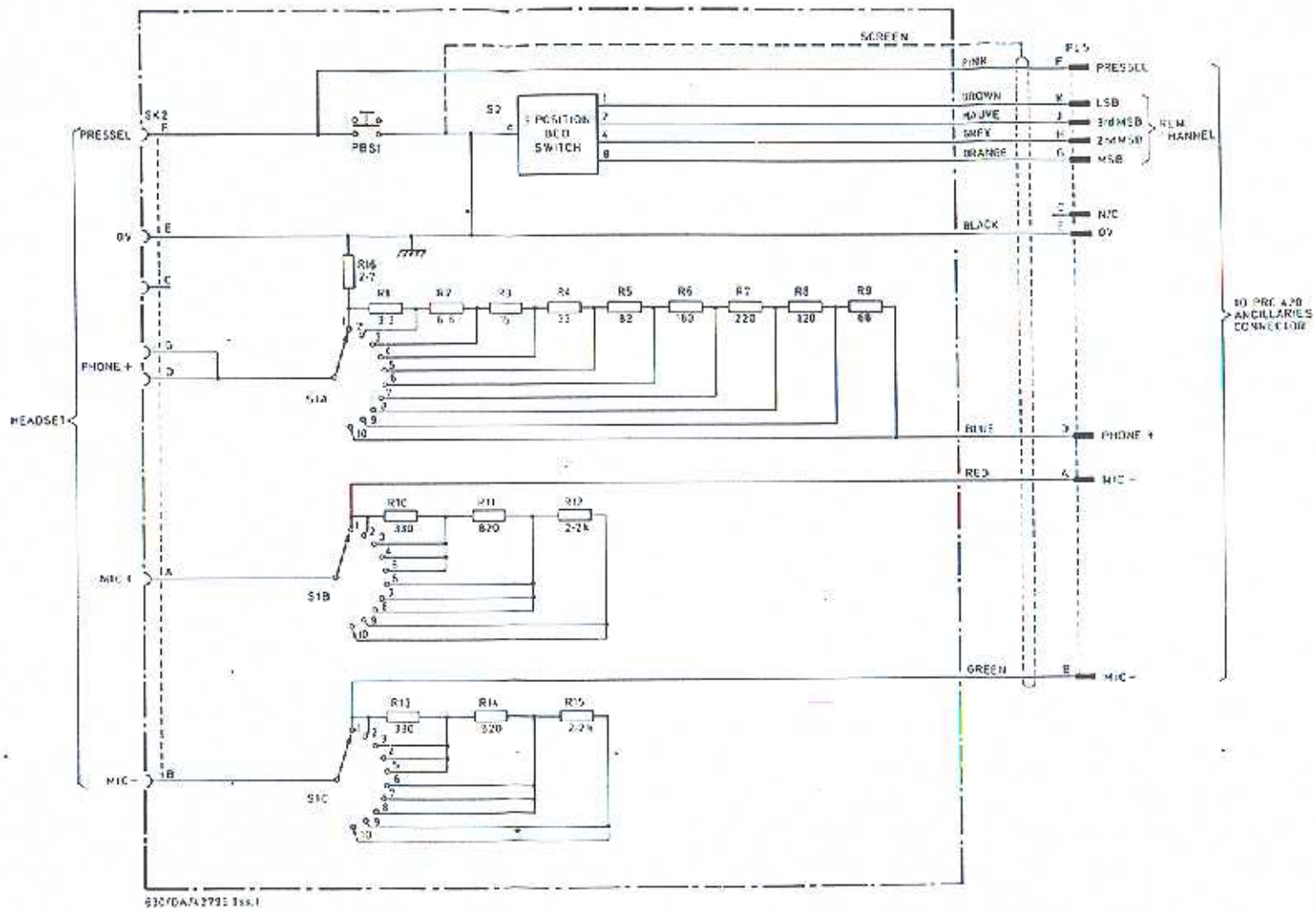


Fig. A1/2

PV2319 Hand held channel selector - circuit diagram

Fig

Fig 1 IF board circuit diagram

Fig. 1

A1B board : circuit diagram