

TECHNICAL TRAINING COURSE

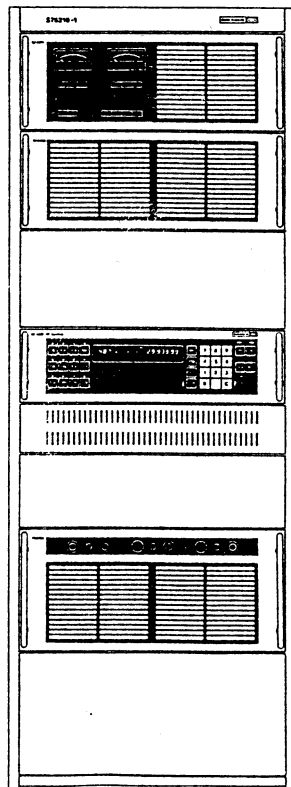
FOR

NORSKE TELEVERKET & LUFTFARTSVERKET

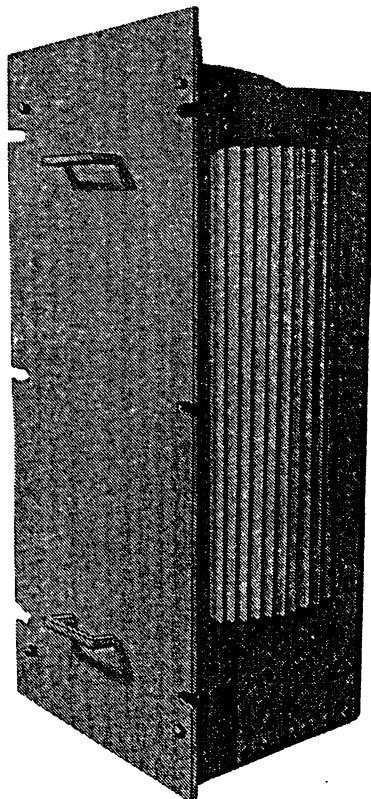
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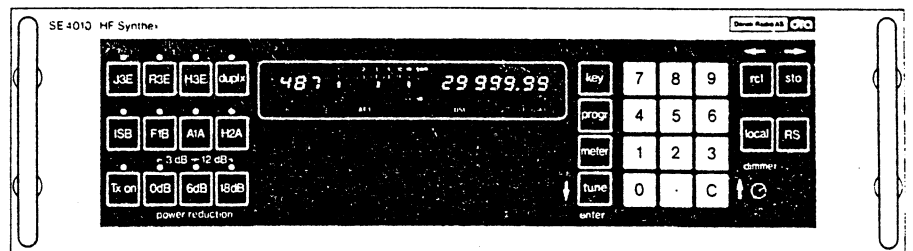
HF SSB/ISB Communications Transmitter



TU 4013
Antenna Tuner



SE 4010
HF Synthesizer



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26	TU4013 SELF TEST AND PROGRAM FACILITIES
27	REMOTE OPERATION
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SYSTEM DESCRIPTION

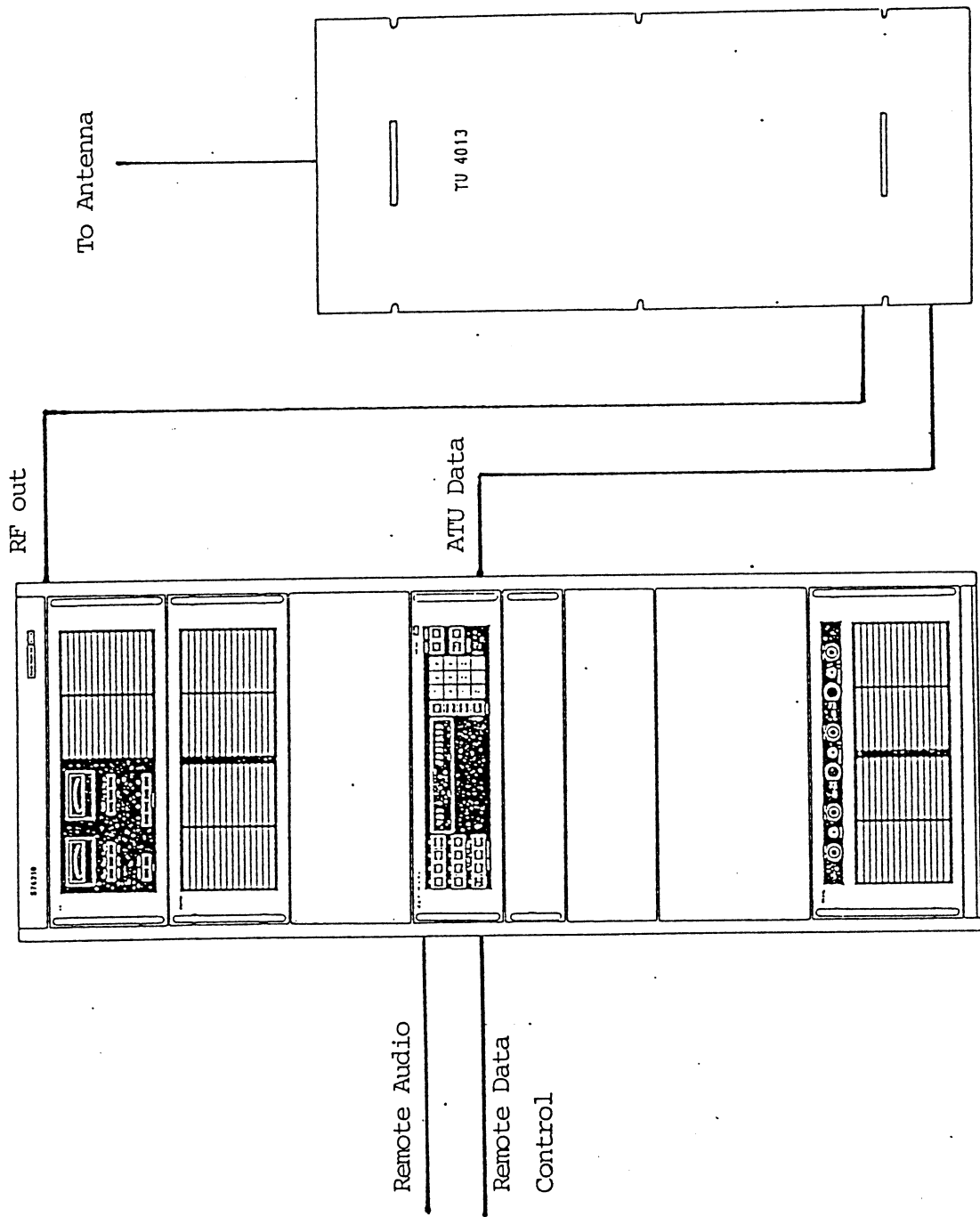
The system consists of two (three), see the figure, items:

- one 500 Watt transmitter
- one antenna tuner
- (one antenna)

The system interconnection is simple:

- Only two cables, one coax and one multi-cable, between the transmitter and the antenna tuner.
- Only two cables for the remote control.

All interconnections, except for the data lines for the antenna tuner, are terminated in easily installable connectors.



System Configuration

CONFIGURATION SE4010

The overall functional block diagram of the exciter is shown in the figure.

In the Modulator Assembly A7 the AF inputs are mixed with the first LO at 1.4 MHz. In this way the two sidebands are generated. Finally the two sidebands and the carrier are amplified, by controlled amplifiers, to the wanted amplitudes and then summed together.

On the IF Assembly A3, the 1.4 MHz signal from the Modulator Assembly is mixed with second LO signal at 73.6 MHz and the sum-frequency at 75.0 MHz is fed to a voltage controlled attenuator via a bandpass filter. This attenuator is, via the Interface Assembly A5 and the Microcomputer Assembly A8, controlled by the detected output power of the corresponding transmitter. In this way the output power is constantly held on the selected level. After the controlled attenuator, the 75.0 MHz signal is mixed to the output frequency with the third LO at 76.5 MHz to 105 MHz. Finally the signal is amplified up to 1 W in the WBA Assembly A4. The Standard Assembly A2 generates the first LO signal at 1.4 MHz, the second LO signal at 73.6 MHz and the Synthesizer Assembly reference signal.

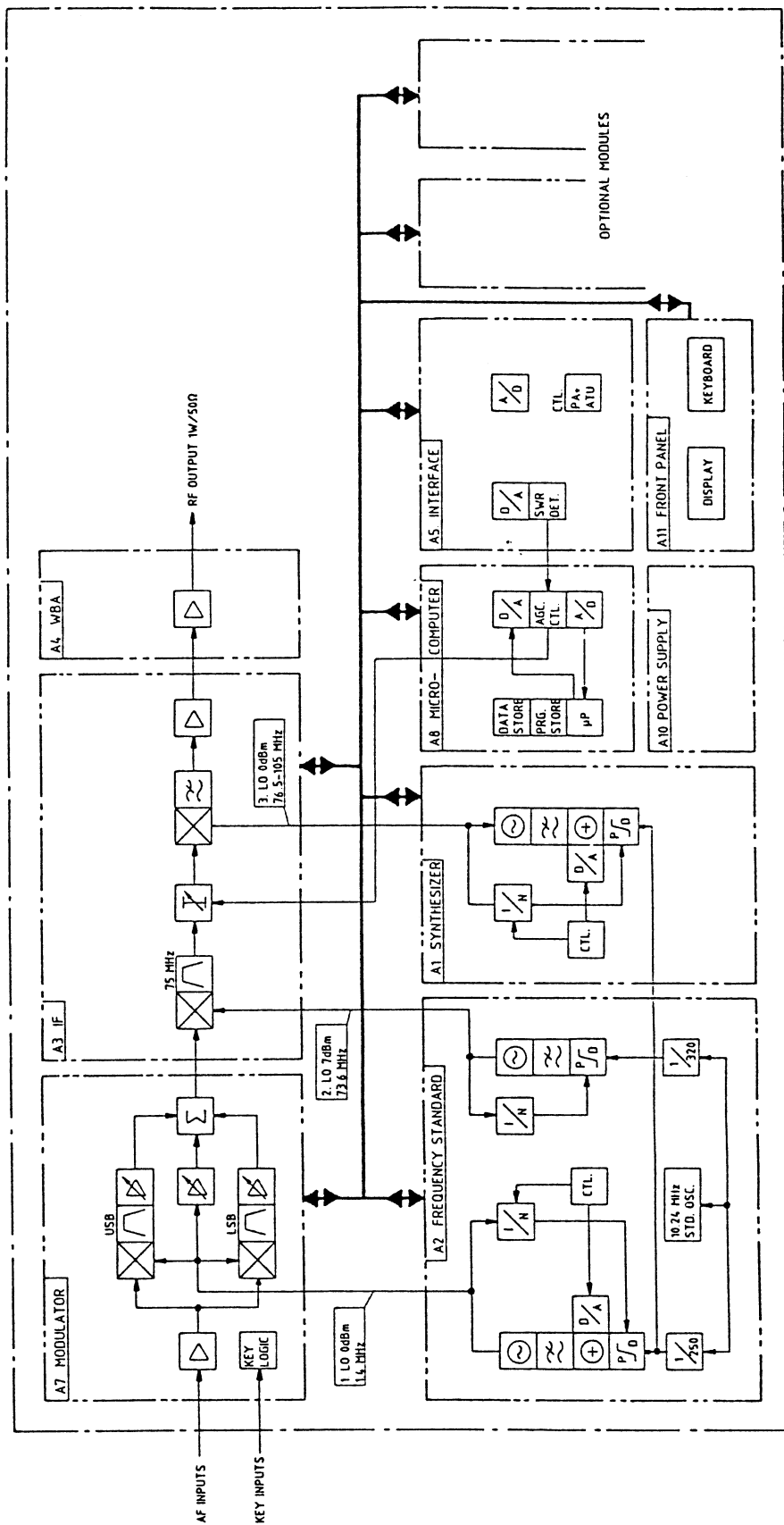
The Synthesizer Assembly A1, generates the third LO signal tunable from 76.5 MHz to 105 MHz in 10 Hz increments.

The Microcomputer Assembly A8 performs the overall control of the exciter.

Typical tasks handled by the assembly:

- Control of the individual assemblies
- Keyboard and step-tune reading
- Display refreshing
- ALC through multiplexed D/A-A/D conversion
- Power level set-up
- Programmable memory set-ups
- Remote control
- Diagnostic routines

Communication between the Microcomputer Assembly and the remaining assemblies is conducted over an internal bus running on the mother PC-board and the front panel ribbon cable.



Overall Functional Block Diagram.

FAST SYNTHESIZER MODULE A1/SE4010

The functional block diagram of the synthesizer is shown in the next figure.

The assembly generates the 75 to 105 MHz local Oscillator (LO) signal for Assembly A3. The synthesizer is based on the Direct Digital Synthesis (DDS) technique, enabling fast frequency shift. The DDS submodule A1A1 generates a 2.672 to 4.0 MHz reference signal for the main loop, variable in 10 Hz steps. A clock signal for the DDS comes from the Clock Loop. A dedicated block diagram of the DDS is shown in a separate figure.

In the Clock Loop a 20.97152 MHz VCXO is locked to the 40.96 kHz reference signal from the master reference oscillator on Standard Assembly A2.

The Clock Loop also delivers a clock signal to the Coarse Loop, where this is divided down to a 327.68 kHz reference signal. The N divider of the Coarse Loop combined with the 16(17) prescaler has a division ratio between 241 and 332, resulting in a Coarse Loop output frequency that is 2.672 to 4.0 MHz higher than the LO output from the Main Loop.

In the Main Loop the output of the main oscillator is mixed down with the Coarse Loop output. The resulting signal is routed to a phase detector where it is compared with the DDS output. The frequencies of these two signals are the same when the loop is locked, resulting in a 75 to 104.99999 MHz LO output with 10 Hz resolution.

A clamping circuit prevents the Main Loop from exceeding its locking range and the loop has a variable loop filter, controlled by a lock detector timing circuit, to assure high switching speed.

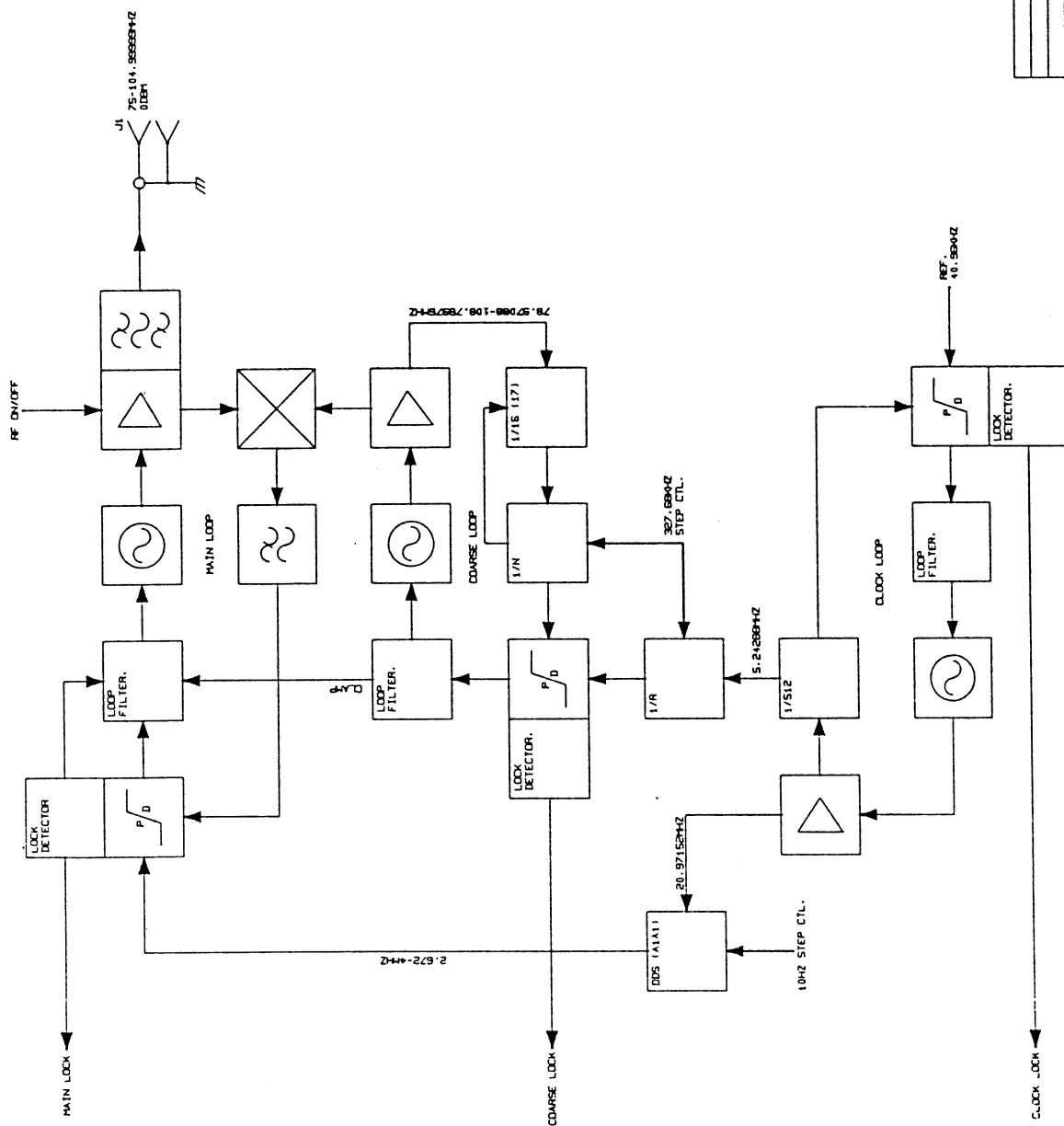
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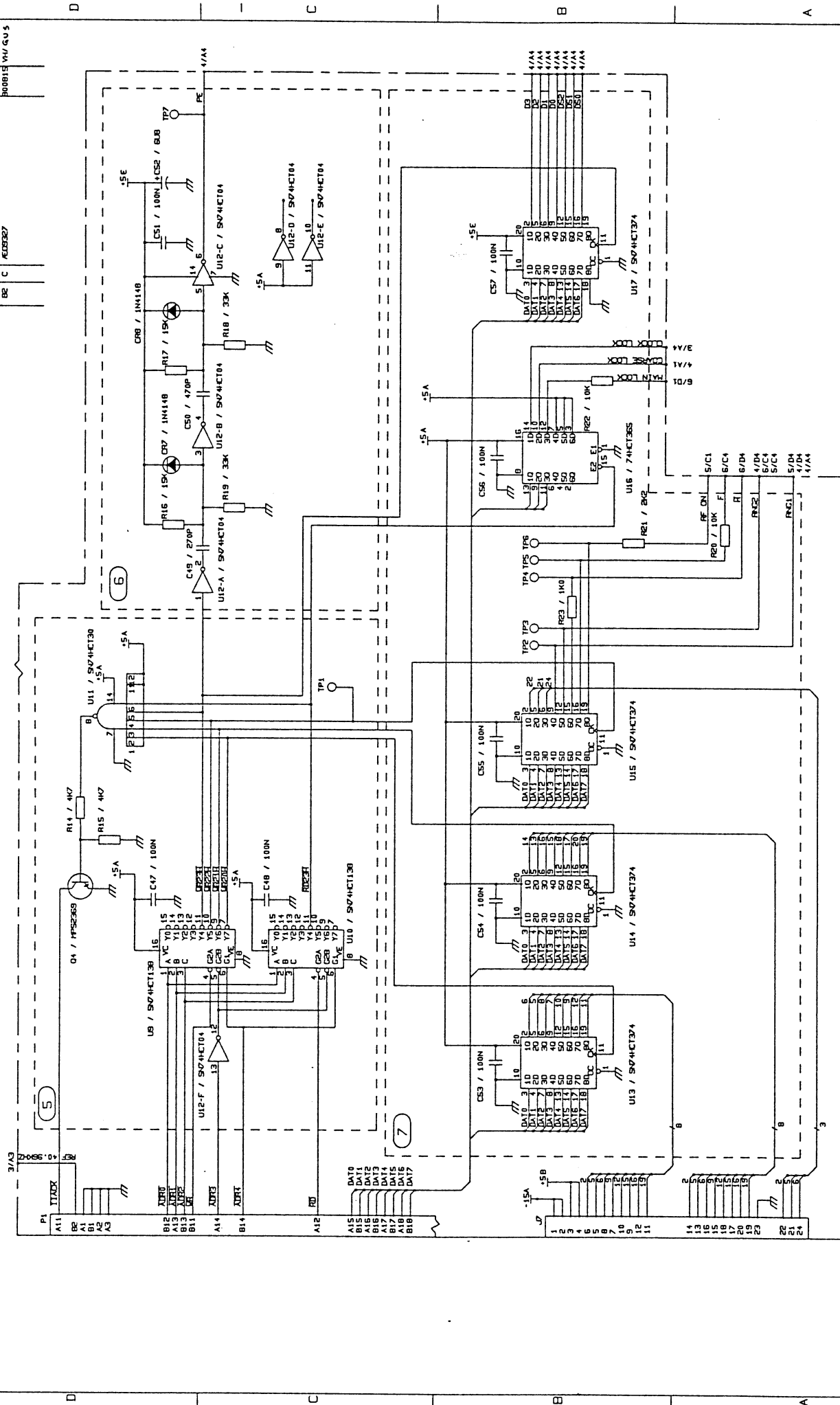
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REVISIONS		DATE	APPROVAL
206	LTH	300827	VH
DESCRIPTION			
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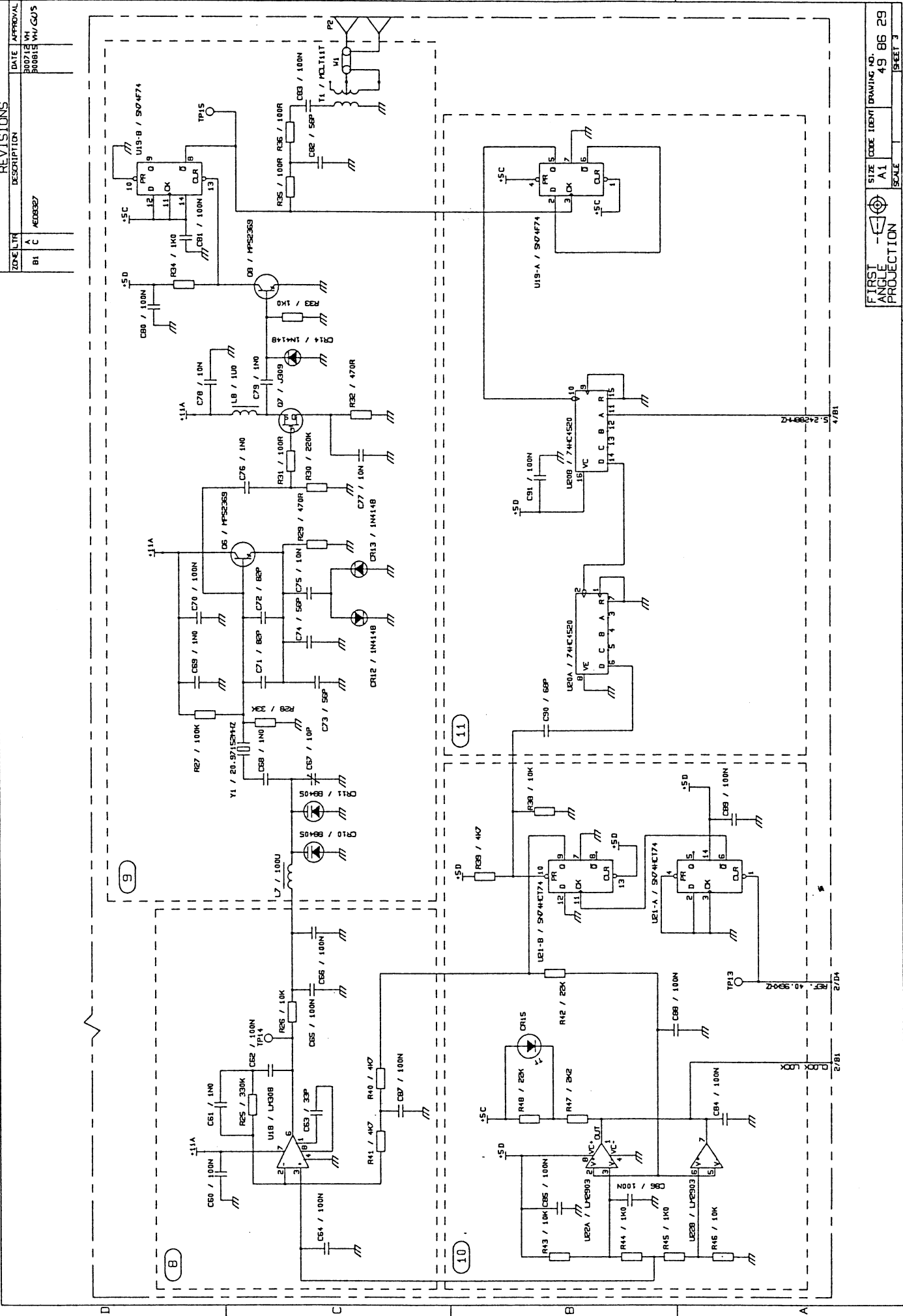
DANSK RADIO AS		DANSK RADIO AS	
1	A	1	A
TITLE		TITLE	
CONFIGURATION		CONFIGURATION	
FAST SYNTHESIZER A1		FAST SYNTHESIZER A1	
SIZE		SIZE	
CODE 1007		CODE 1007	
DRAWING NO.		DRAWING NO.	
A1		A1	
SCALE		SCALE	
49 86 29		49 86 29	
SHEET 1 OF 1		SHEET 1 OF 1	
FIRST ANGLE PROJECTION		FIRST ANGLE PROJECTION	
MATERIAL		MATERIAL	
USED ON		USED ON	
APPLICATION		APPLICATION	
NEXT ASSY		NEXT ASSY	
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DR.		DR.	
VH 300827		VH 300827	
AW 100111		AW 100111	
AP.		AP.	
GUS 100120		GUS 100120	

REVISIONS		DATE	APPROVAL
20	ELTR	000712 VH	
19	BE	000815 VH/GUS	
18	C	000927	

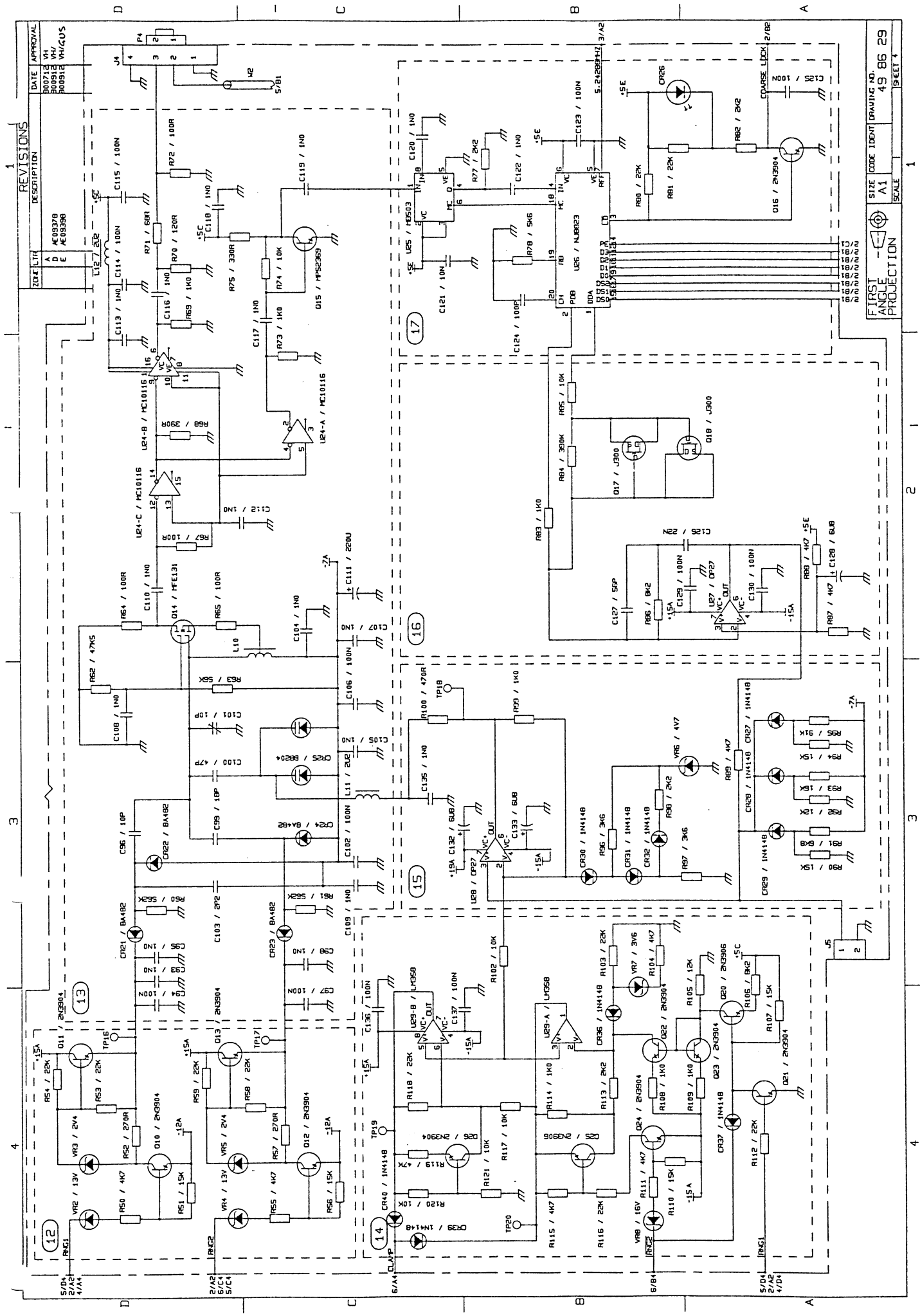


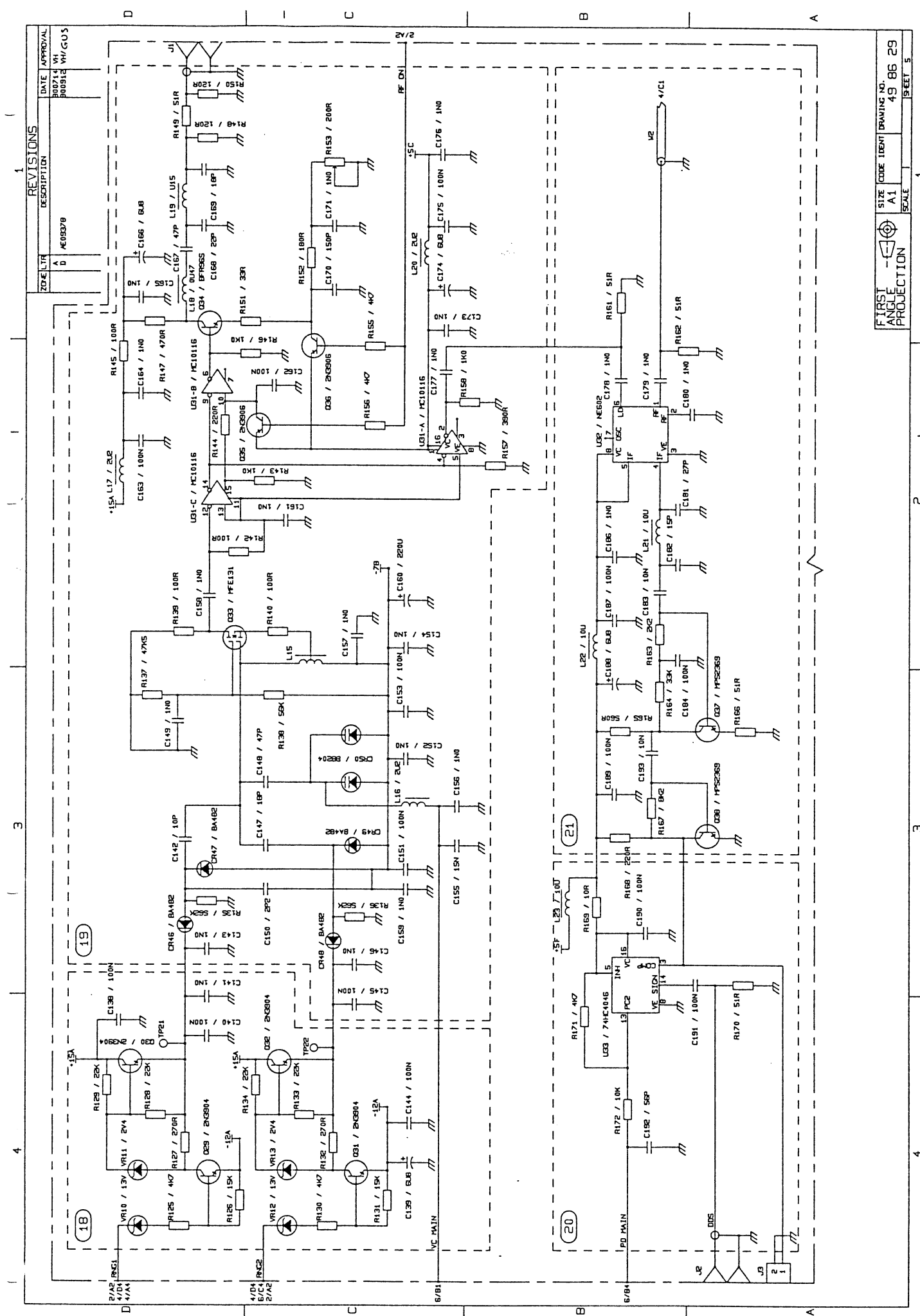
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	SCALE		SHEET 2

REV	DATE	APPROVAL
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02	000815	WH/GJS
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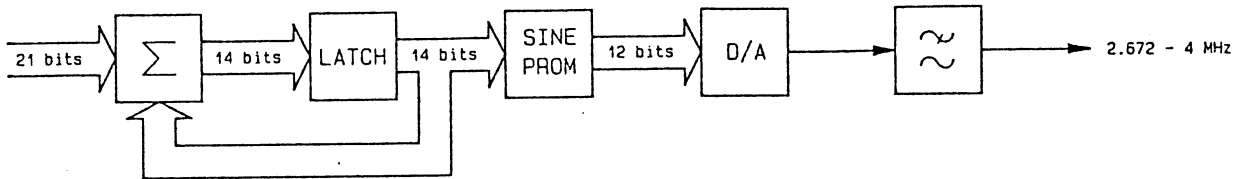
DATE	000718	WH
DESCRIPTION	000815	WH/GJS
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Direct Digital Synthesizer A1A1/SE4010

The functional block diagram of the DDS is shown in the figure below.



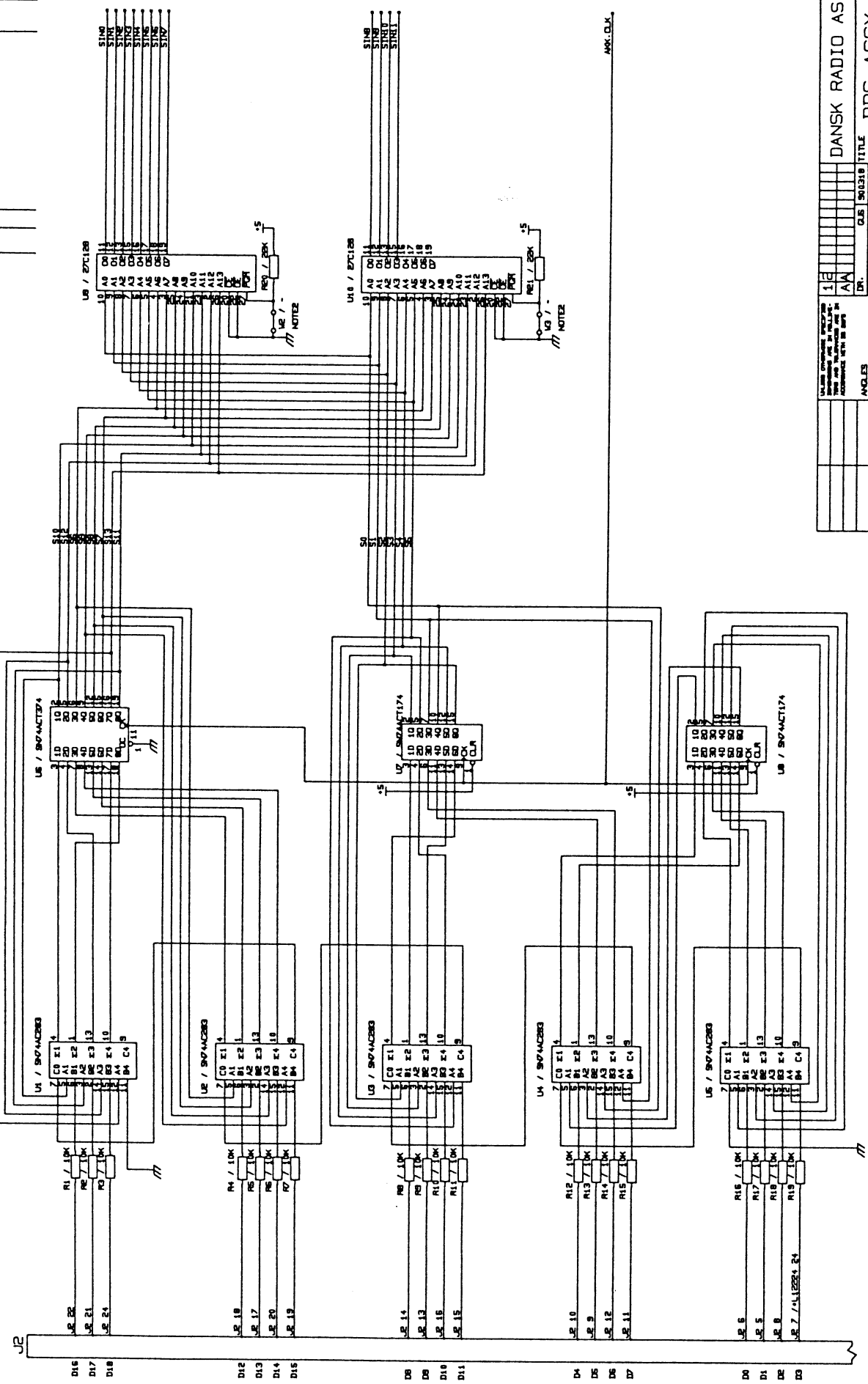
The adder and the following latch form a fast phase accumulator. The 21 bits input to the phase accumulator is truncated to 14 bits at the output and sent to the sine-PROM. These 14 bits represent the phase of a sinewave. The 12 bits output of the sine-PROM represents the corresponding magnitude of the sinewave. The 12 bits are clocked into a very linear D/A converter and the analog output of the converter is fed to a lowpass filter. The resulting output signal of the DDS is a signal with a fundamental frequency of 2,672-4MHz.

NOTE: 1. SUFFIX IN PARTNAME (E.G. 10K-A1)
IS FOR FACTORY USE ONLY.
NOTE: 1M2 AND V3 NOT MOUNTED FOR 128K PROD

DATE	APPROVAL
190705	CLS
190705	CLS

REVISIONS

DATE	DESCRIPTION
190705	CLS

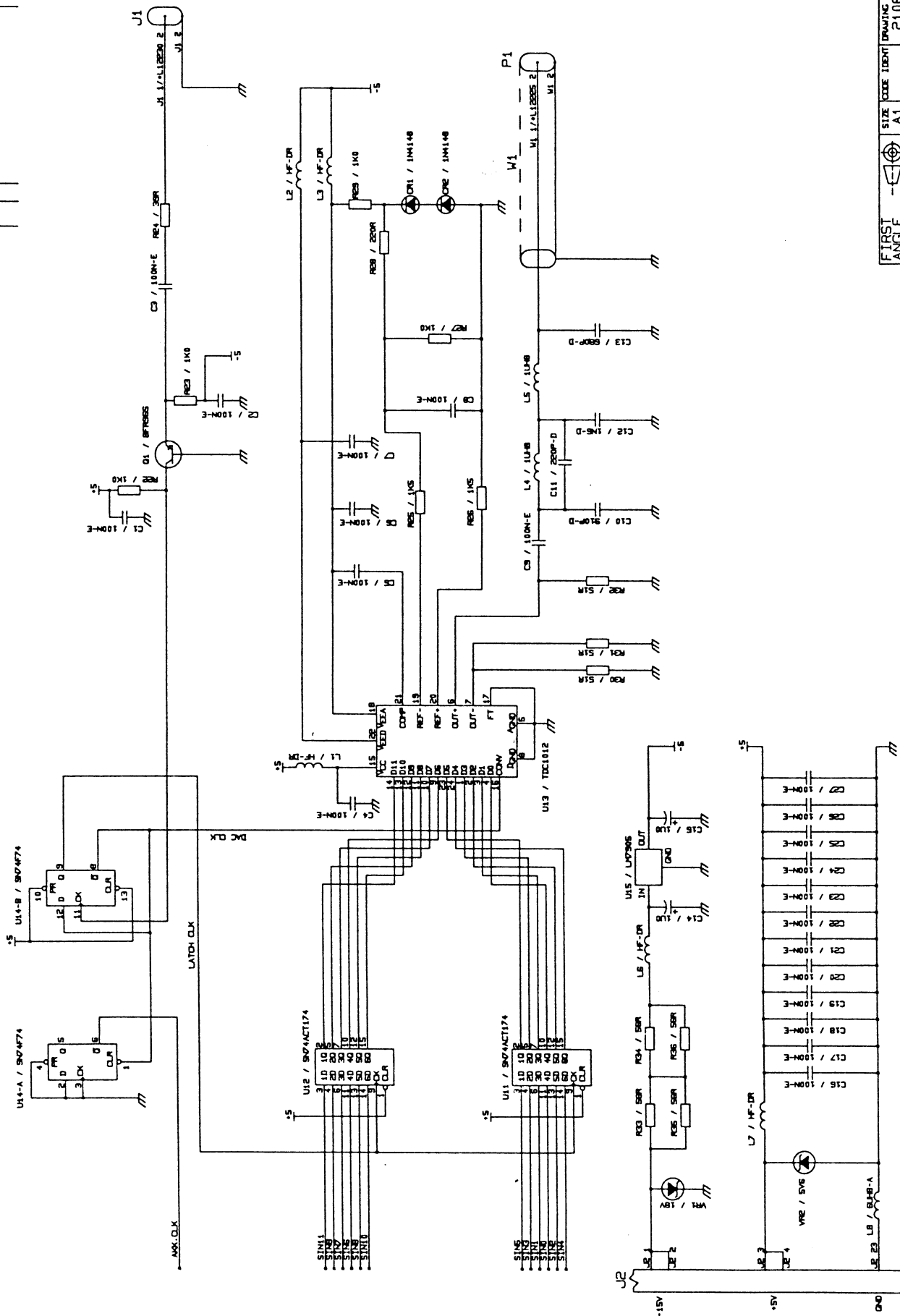


DANSK RADIO AS	
TITLE DDS ASSY	
A1A1	
Q15 500319	RV (187)
Q16 500705	AP
Q17 500705	AP
Q18 500705	AP
Q19 500705	AP
Q20 500705	AP
Q21 500705	AP
Q22 500705	AP
Q23 500705	AP
Q24 500705	AP
Q25 500705	AP
Q26 500705	AP
Q27 500705	AP
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Q94 500705	AP
Q95 500705	AP
Q96 500705	AP
Q97 500705	AP
Q98 500705	AP
Q99 500705	AP
Q100 500705	AP

NOTE 1. 1X IN PARTNAME (E.G. 10K-A)
IS FOR FACTORY USE ONLY.

REVISIONS

DATE	APPROVAL
10/17/85	CLS
10/17/85	CLS
10/17/85	CLS



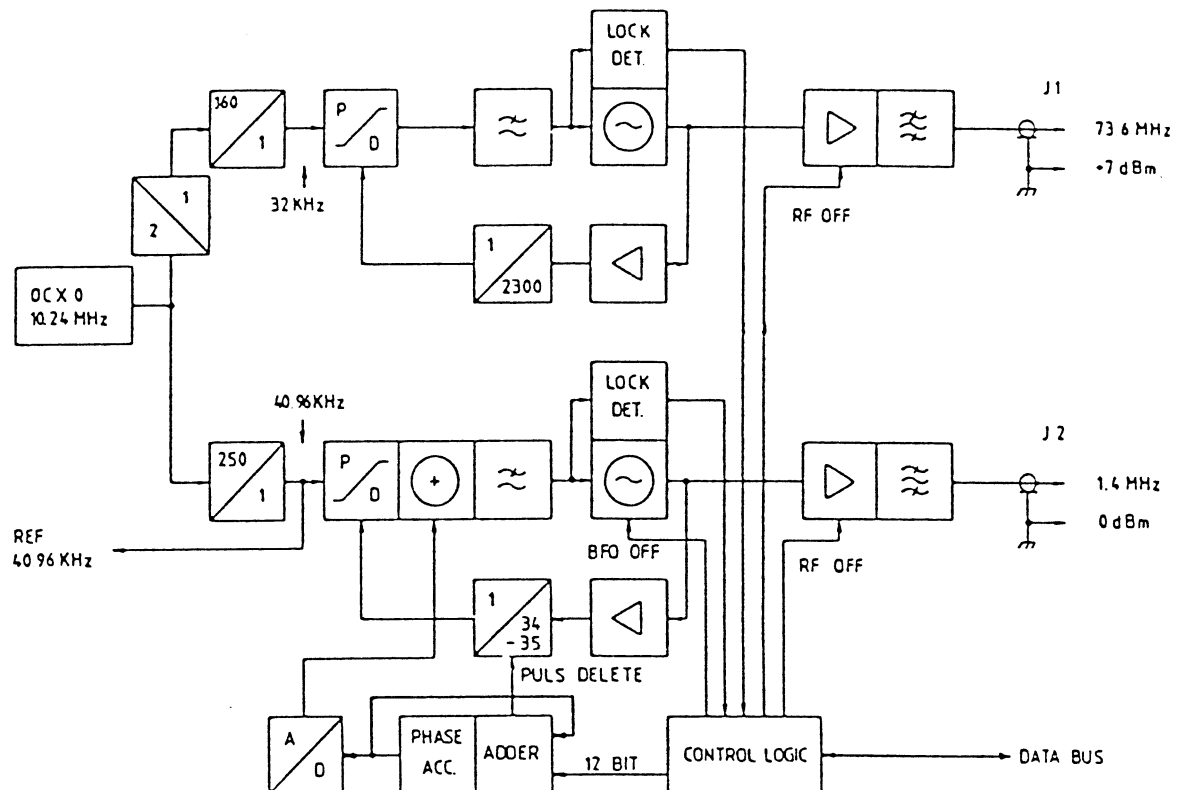
FIRST ANGLE PROJECTION	SIZE A1	CODE 1001	DRAWING NO. 210662-EC
SCALE	1	1	1
SHEET 2			

FREQUENCY STANDARD MODULE A2/SE4010

The functional block diagram of the Standard Assembly is shown below.

The assembly holds three basic functions:

- 10.24 MHz stable master oscillator
- 73.6 MHz synthesized 2nd L0
- 1.4 MHz synthesized 1st L0



The output signal from the 10.24 MHz oven controlled crystal oscillator (OCXO) is applied to two divider chains. One generating 32 kHz reference clock for the 73.6 MHz loop, and one generating 40.96 kHz reference clock for the 1.4 MHz loop and the A Standard Assembly with temperature compensated crystal oscillator (TCXO) instead of OCXO is optionally available. Also standard assemblies with TCXO or OCXO with possibilities for synchronizing to external 1, 5 or 10 MHz reference signals are available. Another option is an assembly with OCXO and reference output of 5.12 MHz.

FREQUENCY STANDARD MODULE A2/SE4010

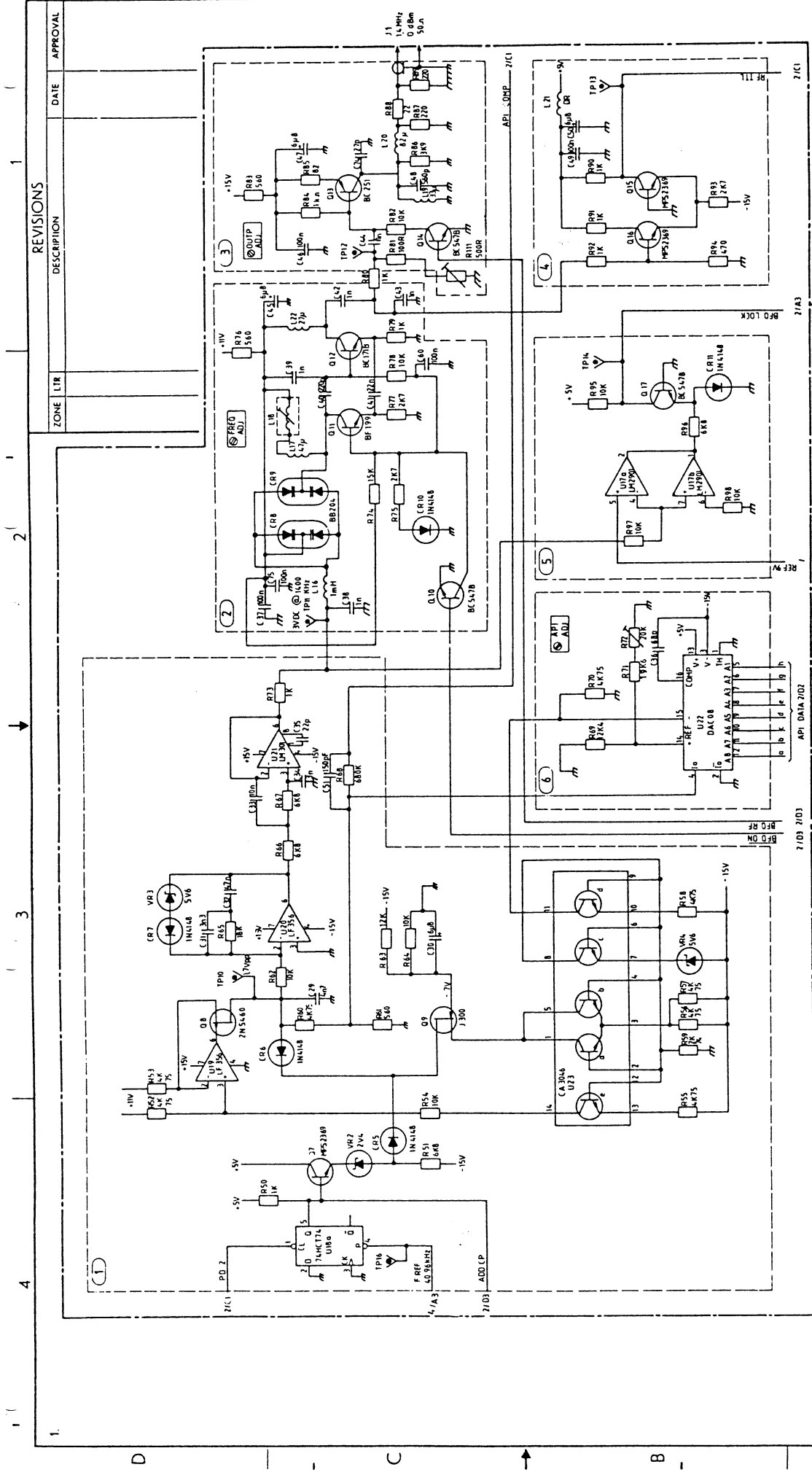
The 73.6 MHz oscillator is formed by a voltage controlled crystal oscillator ensuring low side-band noise. The loop has a 10 Hz bandwidth compensating for frequency drift.

The 1.4 MHz synthesizer is tunable in 10 Hz increments. The loop reference frequency is 40.96 kHz and the corresponding loop bandwidth approx. 800 Hz.

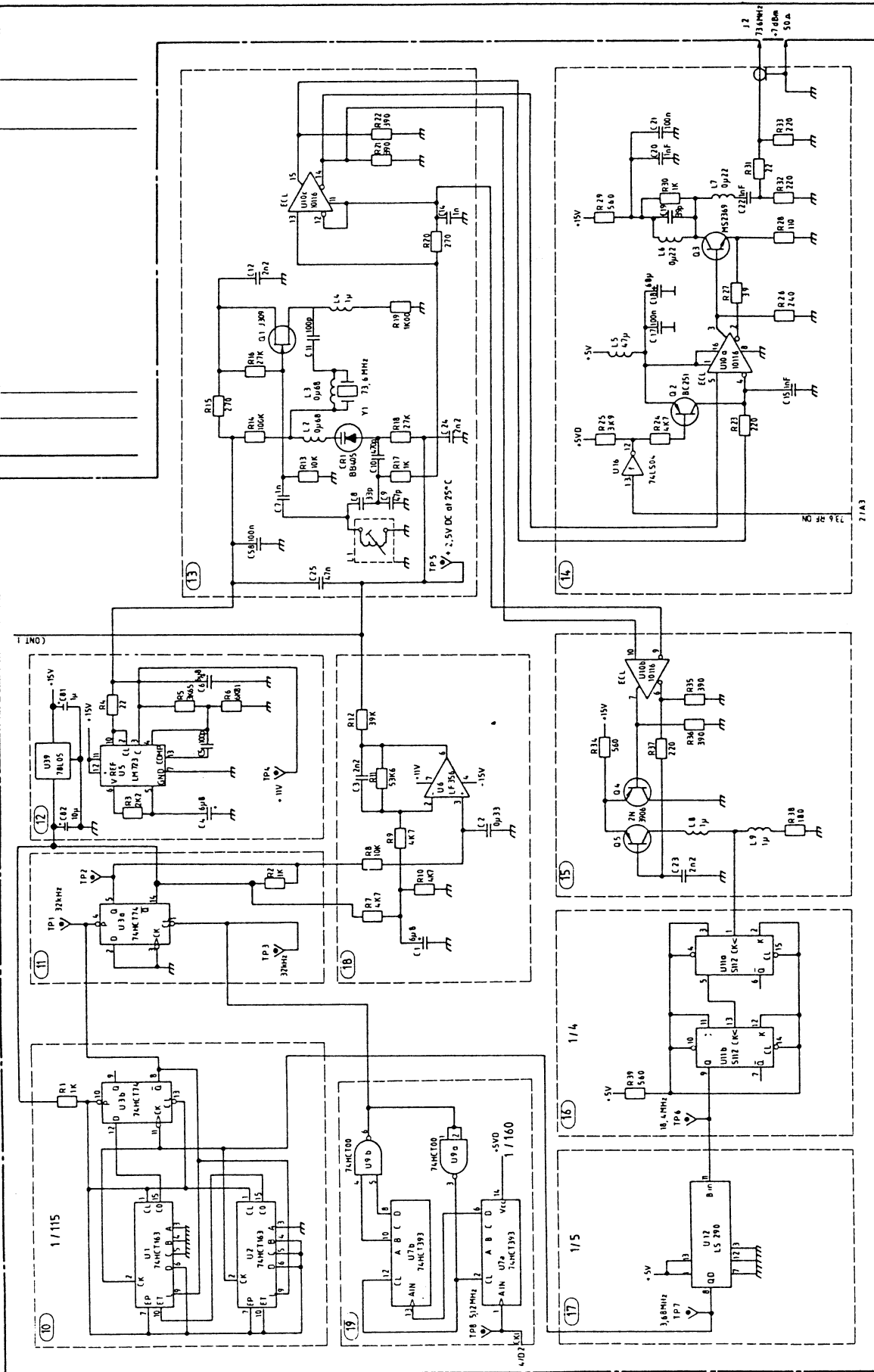
The loop uses a fractional N technique, where the loop output frequency is equal to the number of N.P. times the reference frequency, where N and P are positive integers. Due to the limited tuning requirements for the loop, the N number is fixed 34. The programmed number P is used as input to a digital loop adding the fractional ratio to an accumulated residual fraction.



Every time the accumulated residual fraction overflows, the N divider is commanded to divide by 35, deleting one vco clock pulse. The average vco frequency will be raised in this way with

40.96 kHz divided by P. To compensate for pulse delete sidebands on the 1.4 MHz signal, the residual fraction is converted to an analogue signal and added to the error signal from the phase detector. The composed error signal is filtered before entering the control input of the voltage controlled oscillator.



Dansk Radio AS		dlr	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLI- METRES AND TOLERANCES IN ACCORDANCE WITH DS 2075		TITLE: STANDARD OCXO w/ input AZ	
ANGLES: LIN. DIM.:		DR: VH 17.1 1989	
MATERIAL: NEXT ASSY		CH: R	
APPLICATION		AP: A2	
SE/RX4010		NO: 49 28 17-A	
USED ON		SCALE	
APPLICATION		SHEET 1 OF 4	

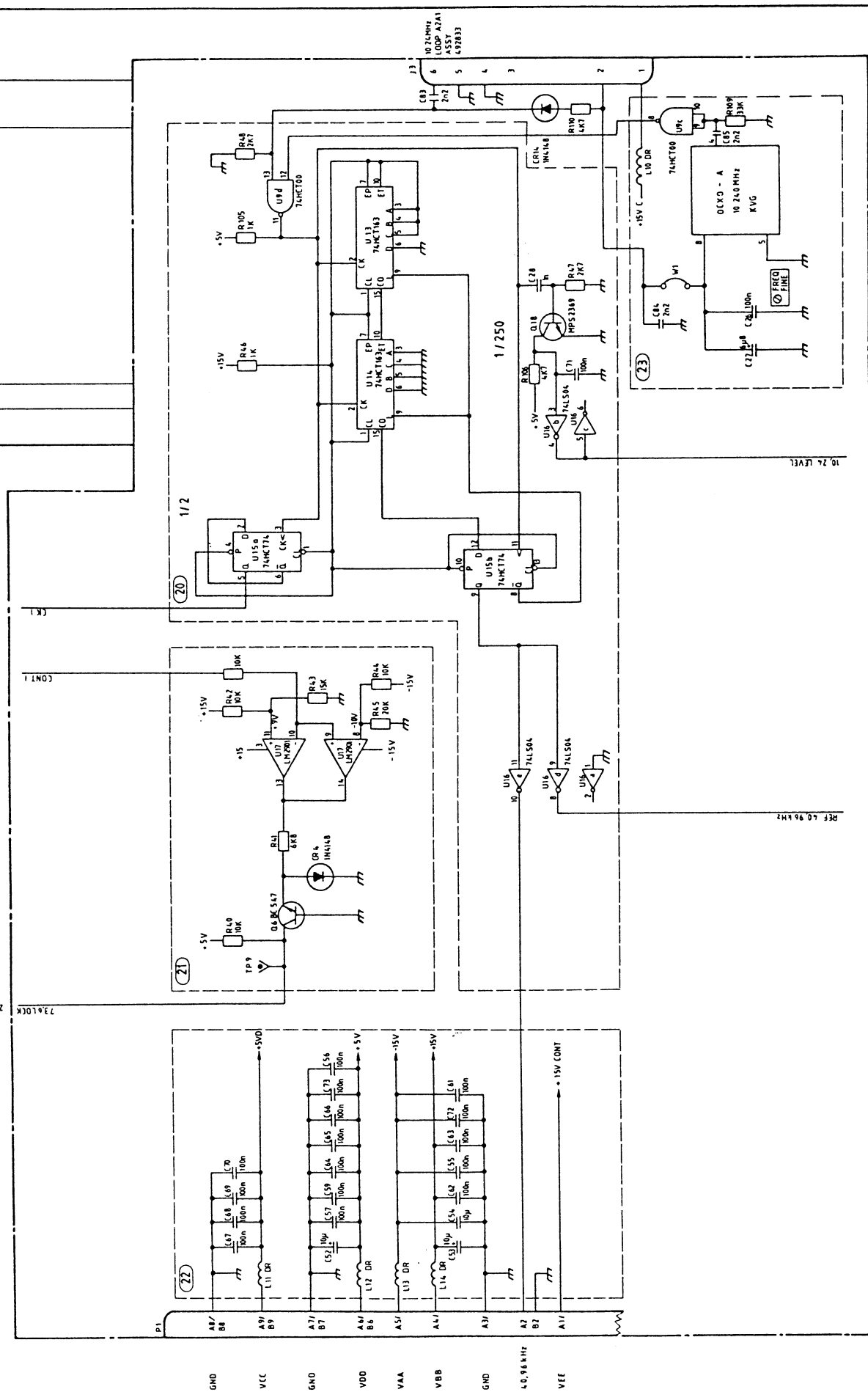


FIRST ANGLE		SIZE A2	CLASS:	NO.:
				49 28 17-A

APPROVAL

DESCRIPTION

ZONE	LTR
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SIZE	CLASS:
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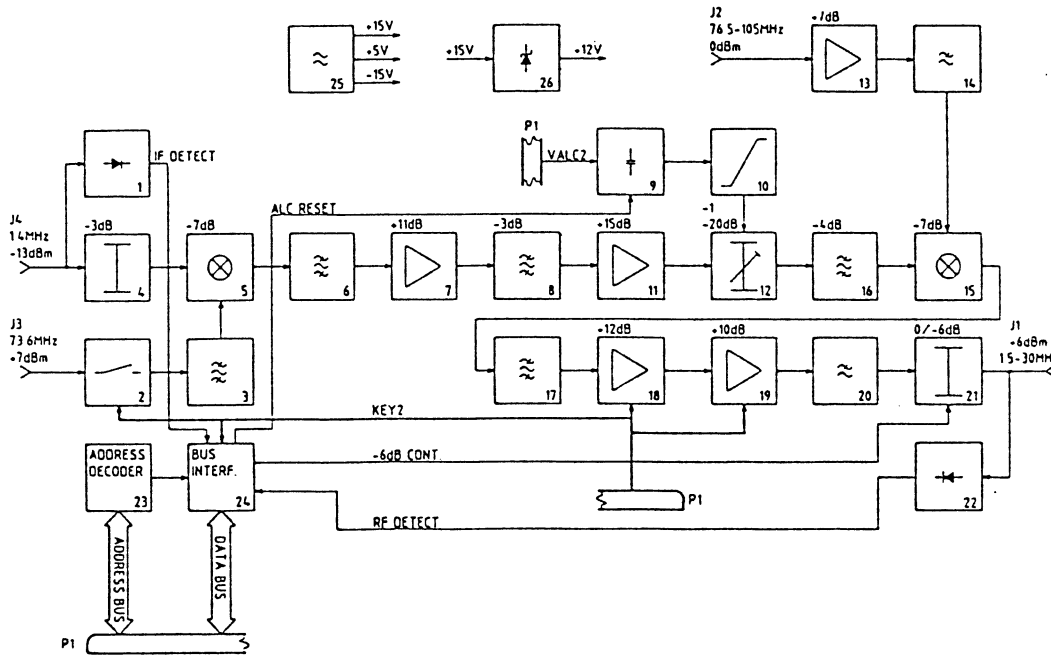
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IF MODULE A3/SE4010

The functional block diagram of the IF Assembly is shown in the figure below:

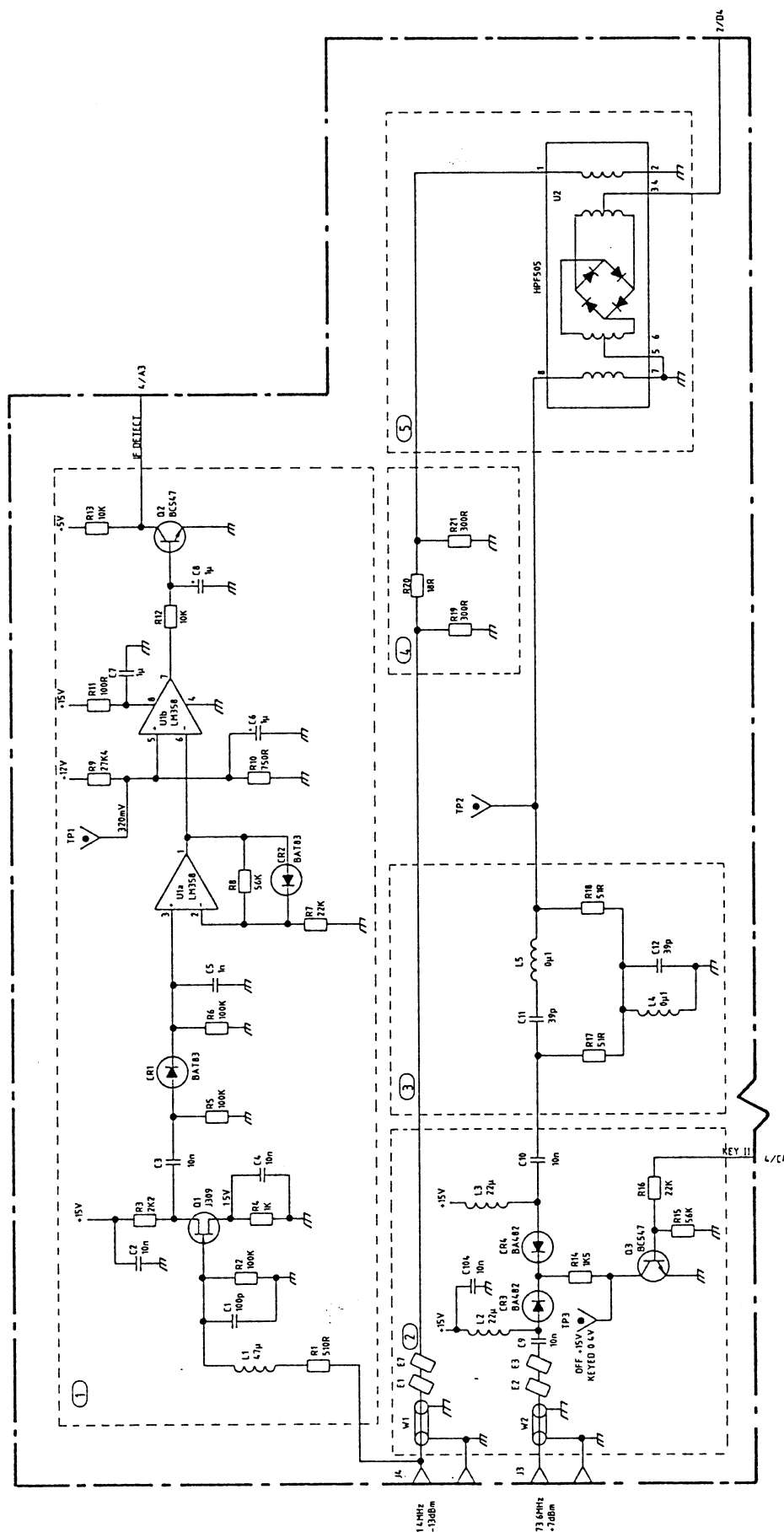


The IF is a double conversion circuit. It first converts the 1.4MHz signal to 75MHz and from 75MHz to a signal in the frequency range of 1.5MHz to 30MHz. The double conversion takes place to ease the suppression of the image signals.

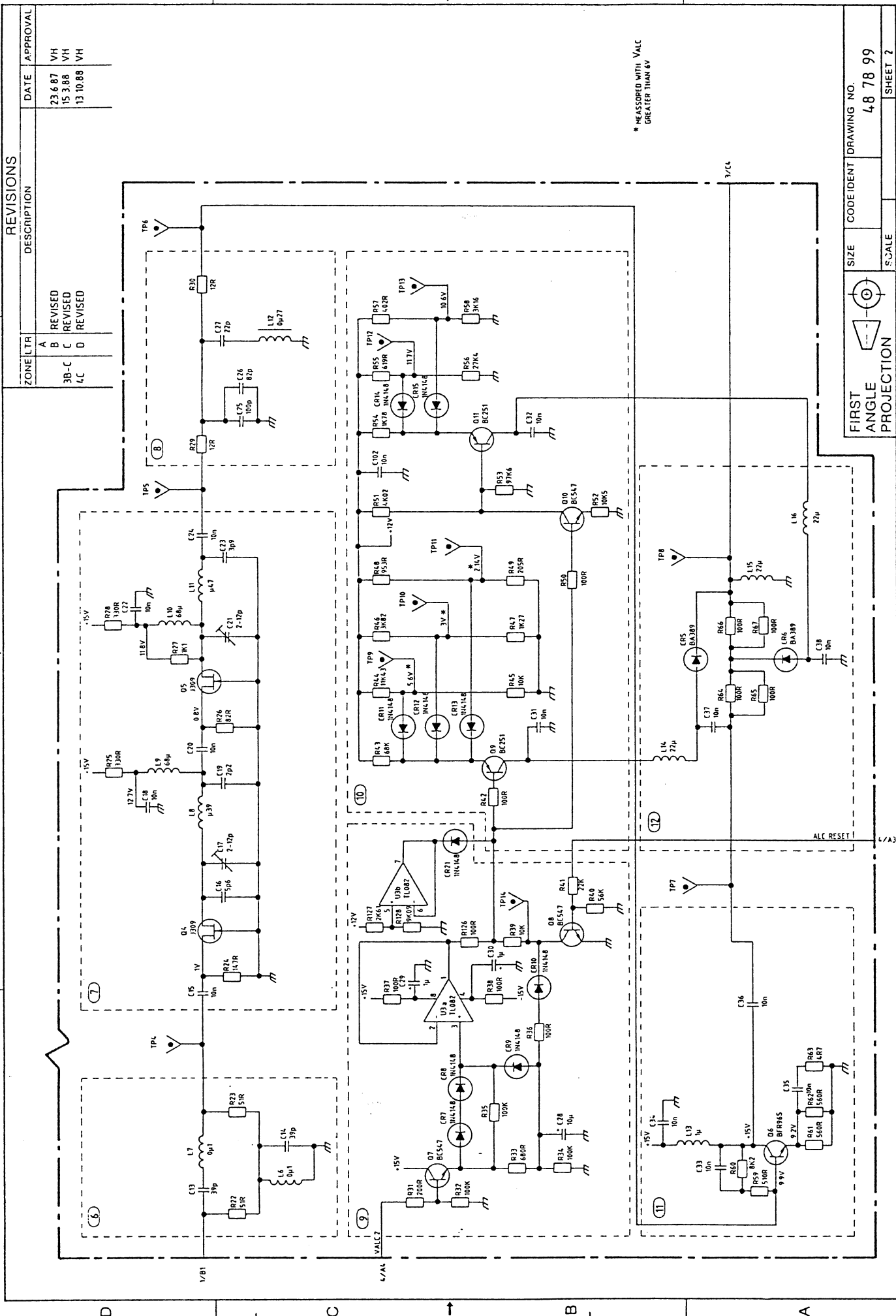
The 1.4MHz signal is converted to a 75MHz signal in the second mixer 5 which is fed with a 73.6MHz signal controlled by KEY2. The 75MHz signal is amplified in 7 and 11, its level is controlled in 12 and the bandwidth in 16, a crystal filter. The third mixer is driven by a LO signal in the frequency range of 76.5-105MHz. The output from the third mixer is band-limited in 17, a diplexer, and amplified in 18 and 19, two amplifiers controlled by KEY2. The amplifiers are followed by a lowpass filter 20 and a controlled 6dB attenuator 21.

The interface part of the IF controls the 6dB attenuator and ALC reset function, while it at the same time allows the microprocessor to check the input and output levels in the circuit, through the detectors located at the input 1 and the output 22. Also the status of KEY2 is read on the IF assembly.

REVISIONS		DATE	APPROVAL
ZONE/CTR	DESCRIPTION		
S.3	AE09145	8.6.90	VH
3/D4	REVISED /EM88128	22.4.88 27.4.89	VH



Dansk Radio AS		TITLE	
		IF MODULE A3	
		SE4010	
		VH 24.3 1987	
		CH.	
		AP.	
		AP.	
		FIRST ANGLE PROJECTION	
		SIZE A2	
		CODE IDENT	
		DRAWING NO.	
		48 78 99	
		SCALE	
		SHEET 1 OF 4	



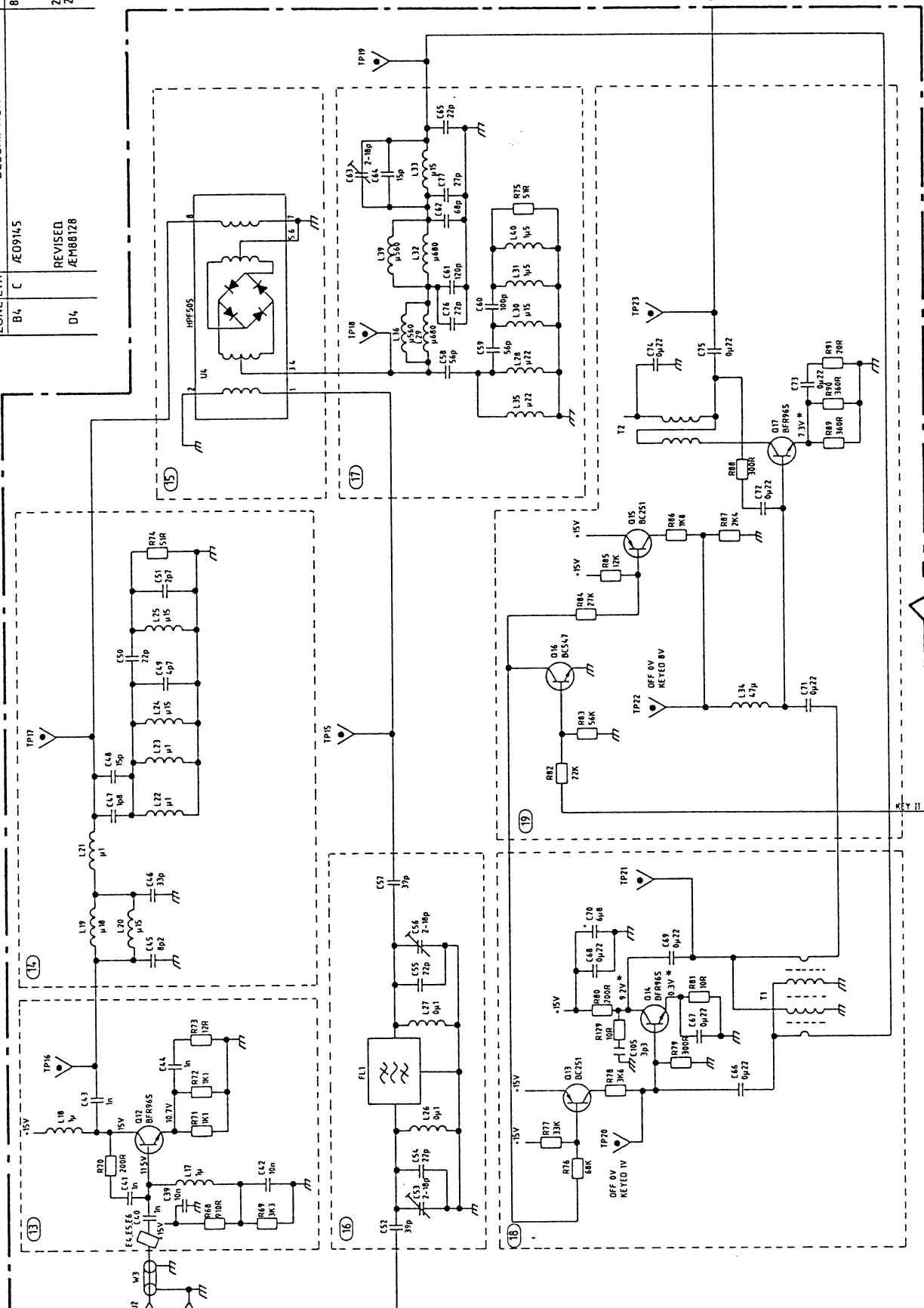
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GREATER THAN 6V

REVISIONS	DATE	APPROVAL
A	23 6 87	VH
B	15 3 88	VH
C	13 10 88	VH
D		

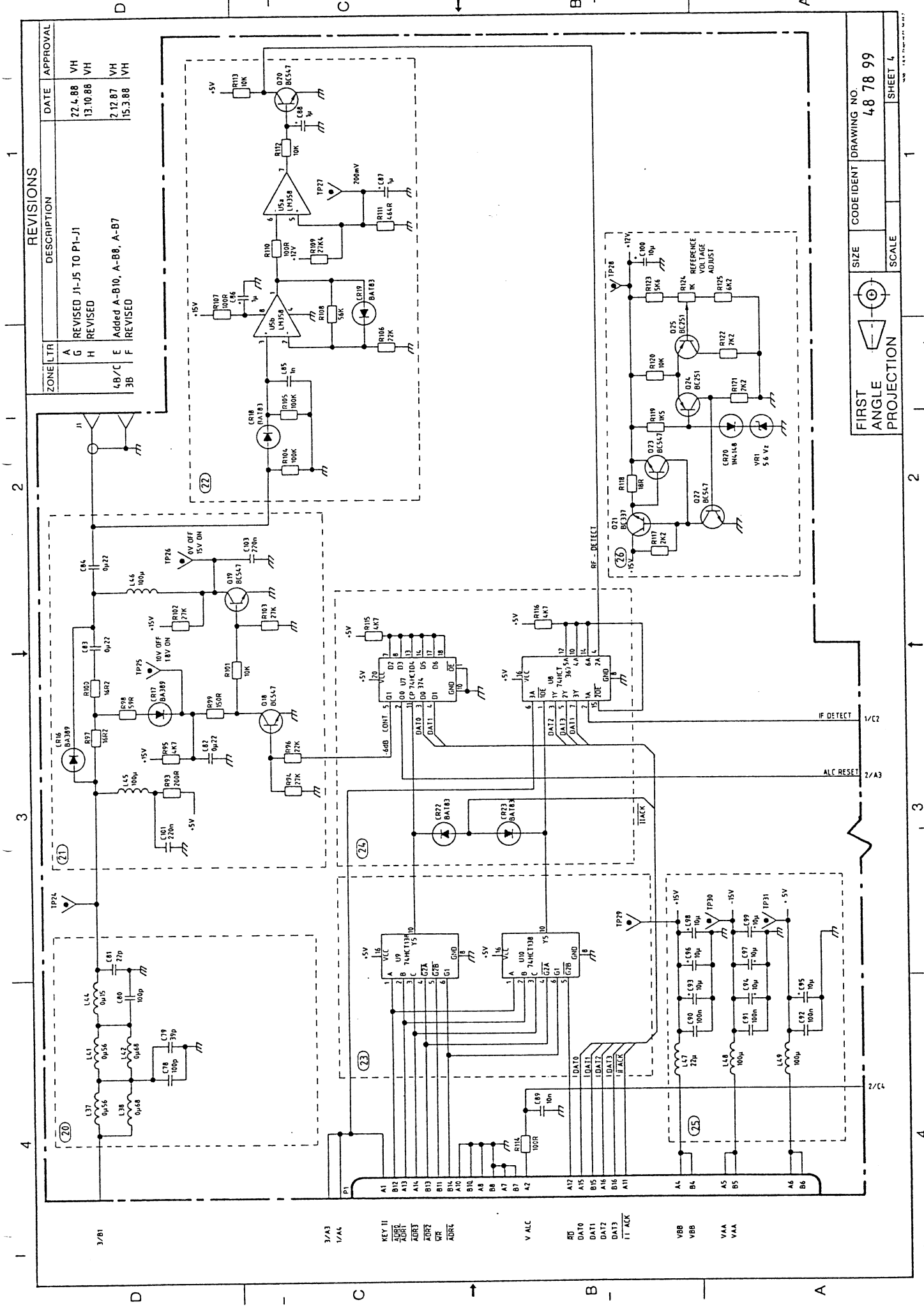
ZONE/LTR	DESCRIPTION
3B-C	REVISED
4C	REVISED

SIZE	CODE/IDENT	DRAWING NO.
1	1	48 78 99
SCALE	FIRST ANGLE PROJECTION	SHEET 2
1	1	1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
B4	C	Æ09145	8.6.90	VH
		REVISED	22.4.88	VH
D4		ÆM88128	27.4.89	VH



Service Sheet A3

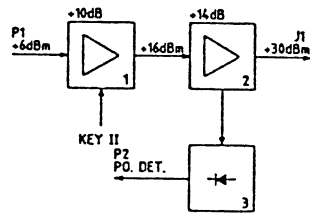


REVISIONS		
ZONE/LTR	DESCRIPTION	DATE APPROVAL
A	REVISED J1-J5 TO P1-J1	72.4.88 VH
H	REVISED	13.10.88 VH
E	Added A-B10, A-B8, A-B7	2.12.87 VH
F	REVISED	15.3.88 VH

FIRST ANGLE PROJECTION		SIZE	CODE IDENT	DRAWING NO.
				48 78 99
SCALE		SHEET 4		

WIDEBAND AMPLIFIER A4/SE4010

The functional block diagram of the WBA Assembly is shown in the figure below:



The Wide Band Amplifier increases the RF output level of the IF Assembly from nominal +6dBm to the level required to drive the power amplifier of the Transmitter.

The WBA consists of two amplifiers, one with a gain of 10dB 1 and one with a gain of 14dB 2. The output level can be monitored on the front panel meter by means of the detector 3.

INTERFACE MODULE A5/SE4010

The ADDRESS DECODING AND DATA IN/OUT BUFFERS circuit, decodes the addresses used by the module. The 8 bit external data bus is buffered by the in/out buffer circuit.

The REFERENCE VOLTAGE circuit consists of an 8 bits DAC controlled by the microprocessor. The reference voltage circuit gives a 10 volt reference voltage for the ALC circuit, too.

The INTERRUPT HANDLING CIRCUIT consists of 6 mutually independent D-flip flops. The interrupt status can be read by the microprocessor and the flip flops can be reset without affecting the interrupt status.

The SUPPLY VOLTAGE WATCH DOG circuit continuously measures the supply voltage. If the voltage drops below 4.7 volts the circuit interrupts the microprocessor and disables the output latches. The A/D CONVERTER CIRCUIT consists of a 4 channel ADC. The input circuits protect the ADC and convert the applied signals.

The 12 BITS OUTPUT CIRCUIT consists of 12 similar internal pull up to 5 volts active low open drain outputs.

The 8 BITS OUTPUT CIRCUIT consists of 8 output circuits designed to give the correct output voltage for the PA unit.

The 4 DIGITAL INPUT CIRCUIT consists of 4 similar input internal pull up to 5 volts.

The 2 DIGITAL INPUT circuit consists of two different input circuits. The input impedance of each input can be change depending on type of the PA unit the SE4010 has to control.

The BAUD RATE CLOCK CIRCUIT consists of a X-tal controlled clock generator for driving the serial communication to the ATU.

The ATU IN/OUT PUT INTERFACE circuit consists of 2 digital inputs and 3 not pulled up active low open drain outputs.

The ATU SENSE CIRCUIT detects if an ATU is connected.

The SERIAL COMMUNICATION TO ATU circuit consists of an USART which gives the proper communication to the ATU. The line driver gives the correct driver capability according to the RS485 standard.

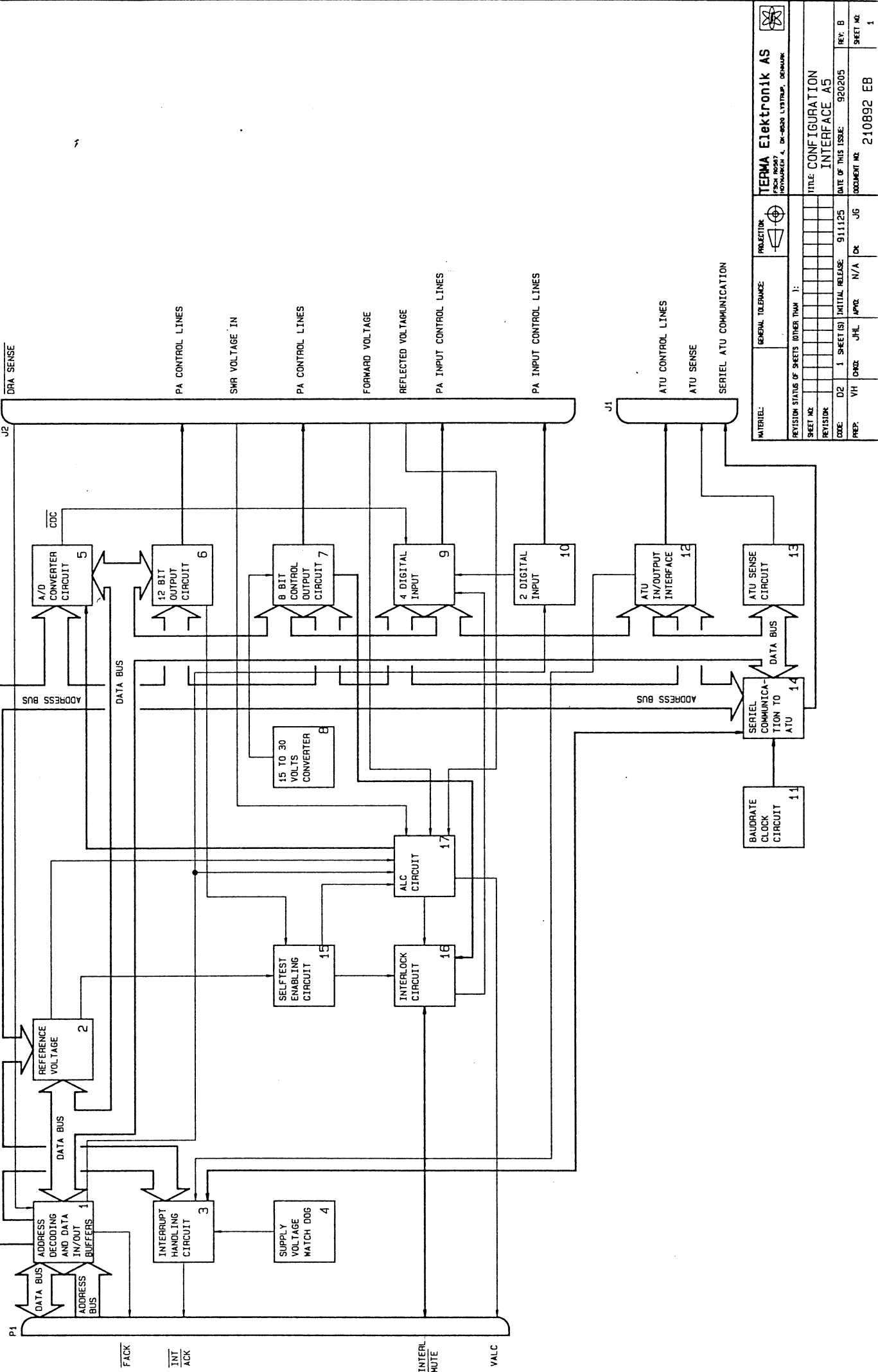
The SELFTEST ENABLING CIRCUIT is active during selftest.

The INTERLOCK CIRCUIT is active when the SWR voltage is too high. The INTERLOCK CIRCUIT is controlled by the microprocessor.

The ALC CIRCUIT contains the necessary circuits for control of the output power level of the Power Amplifier. The circuit includes a power reduction circuit which reduces the output power in accordance with mismatch on the antenna output.

CHANGE ORDER/REVISION				REV.				REV.			
CD	9570	REV.	B	CD	9570	REV.	B	CD	9570	REV.	B
CHKD	DK	JG	DK	CHKD	DK	JG	DK	CHKD	DK	JG	DK

CHANGE ORDER/REVISION				REV.				REV.			
CD	9570	REV.	B	CD	9570	REV.	B	CD	9570	REV.	B
CHKD	DK	JG	DK	CHKD	DK	JG	DK	CHKD	DK	JG	DK



TERMA Elektronik AS				REV. B				REV. B			
PSCH. NO. 9570	REV. B	CD	9570	PSCH. NO. 9570	REV. B	CD	9570	PSCH. NO. 9570	REV. B	CD	9570
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SHEET NO.				SHEET NO.				SHEET NO.			
REVISION				REVISION				REVISION			
CODE: D2	1	SHEET(S)	INITIAL RELEASE	911125	DATE OF THIS ISSUE	920205	DATE OF THIS ISSUE	920205	DATE OF THIS ISSUE	920205	DATE OF THIS ISSUE
PREP: VH	CHKD: JHL	APPROV: N/A	DATE	JG	DATE	JG	DATE	JG	DATE	JG	DATE
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210892	EB			210892	EB			210892	EB		
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NOTE: SUP. IN PARTNAME (E.G. 18C-A)
IS FOR FACTORY USE ONLY.

REVISION

DATE APPROVAL

DATE

DESCRIPTION

ZONE LTR

84

AE08859

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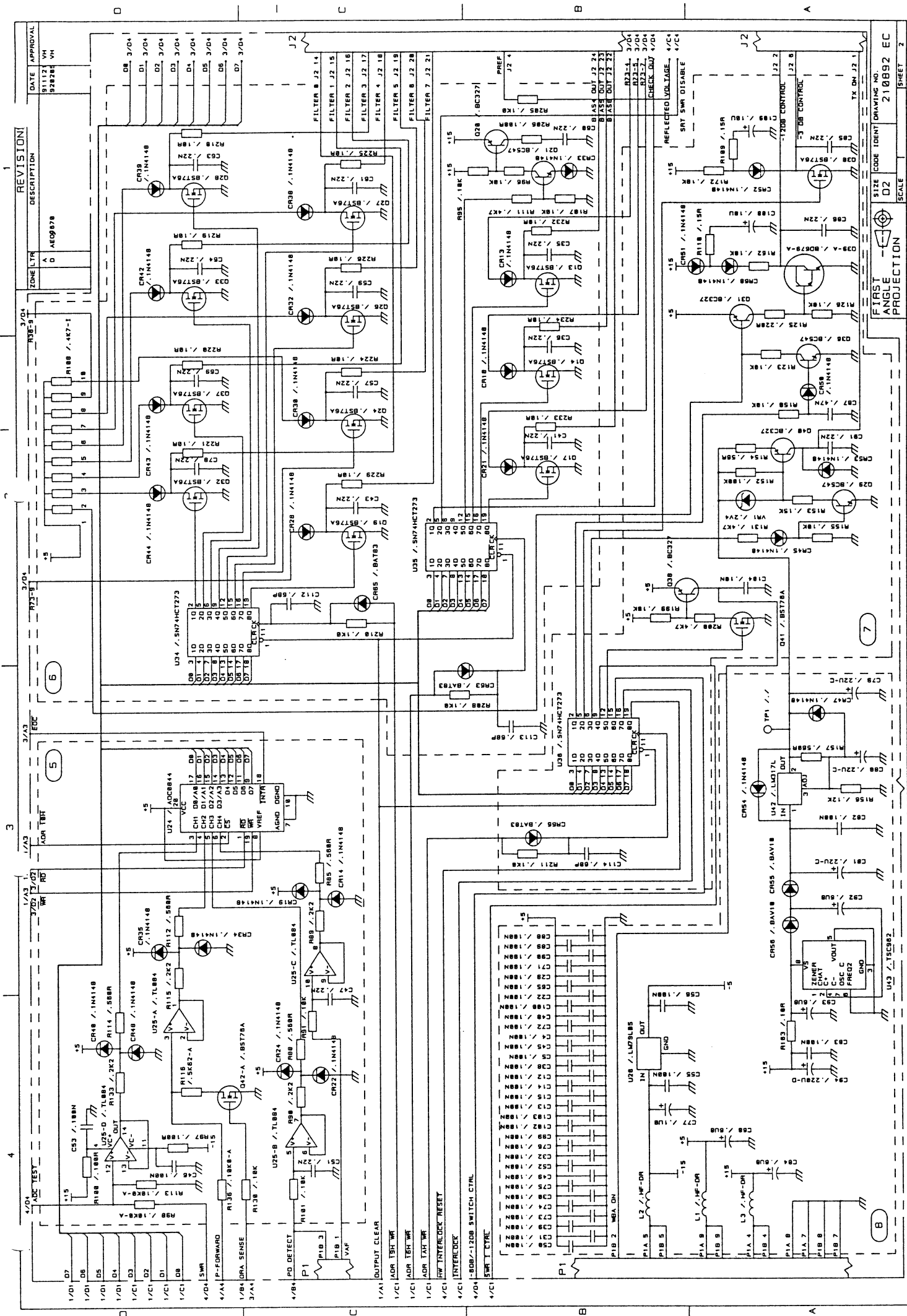
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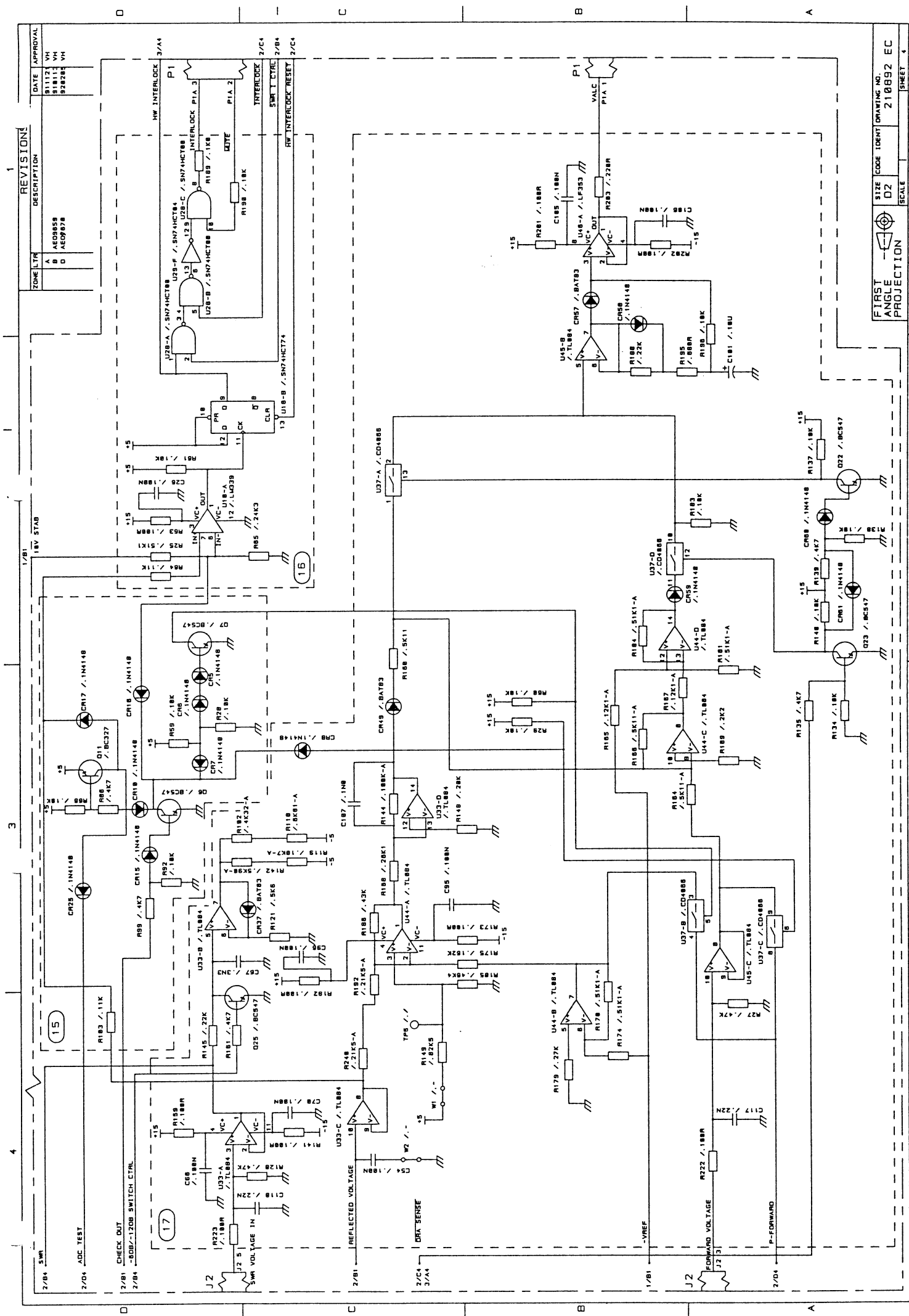
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DATA3

DATA2

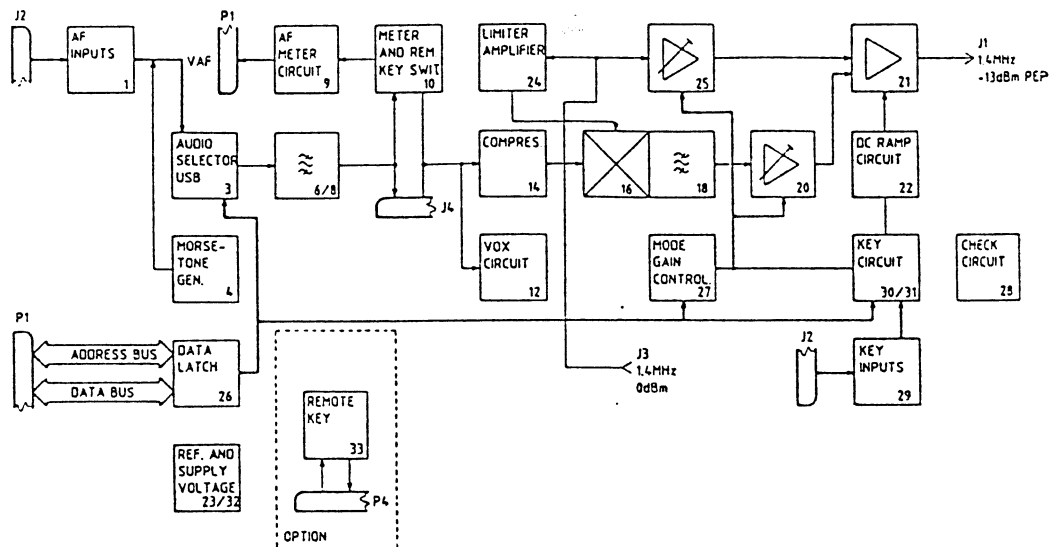
DATA1





MODULATOR MODULE A7/SE4010

The functional block diagram for the SSB version of the Modulator Assembly is shown in the figure below.



Modulator Assembly, SSB version

The AF-signals are fed to the Modulator Assembly via the balanced line transformers or the microphone amplifiers. The wanted AF-input is selected and fed to the compressor through a bandpass filter.

The meter and remote key switch switches the AF meter circuit between LSB and USB, and is also used when the Remote Key is supplied*.

The VOX is placed immediately before the compressor. With this circuit it is possible to key the exciter when the amplitude of the supplied AF-signal exceeds a certain level.

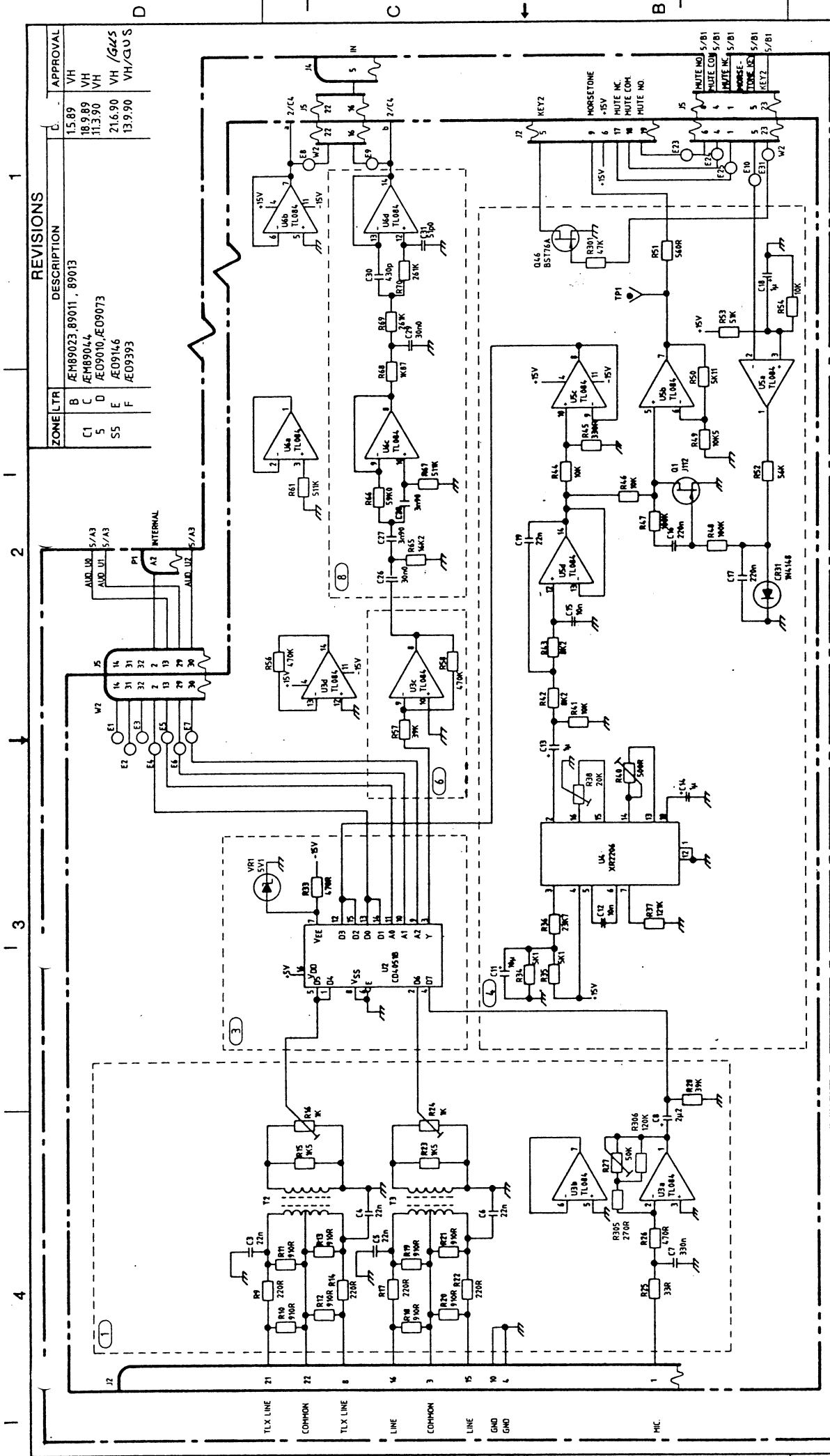
After the compressor, the compressed signal is mixed with the first LO signal at 1.4MHz in the mixer, and the respective sideband is selected by the following crystal filter. The wanted sideband (USB or LSB) is selected by offsetting the first LO signal of 1.4MHz.

The 1.4MHz signal is fed to the mixers through a limiter amplifier. The signal from the limiter amplifier is a square wave signal with an amplitude independent of temperature variations.

The sideband and a 1.4MHz carrier signal are fed into a gain controlled amplifier before the two signals are summed together. The gain of the amplifiers is dependent of the mode.

The shaper after the summing amplifier shapes the envelope of the output signal when the exciter is keyed. Finally the signal is amplified to -13dBm/50Ω.

* The Remote Key is an option, which is used to key the exciter in connection with the Transmitter Remote Control TC4010.

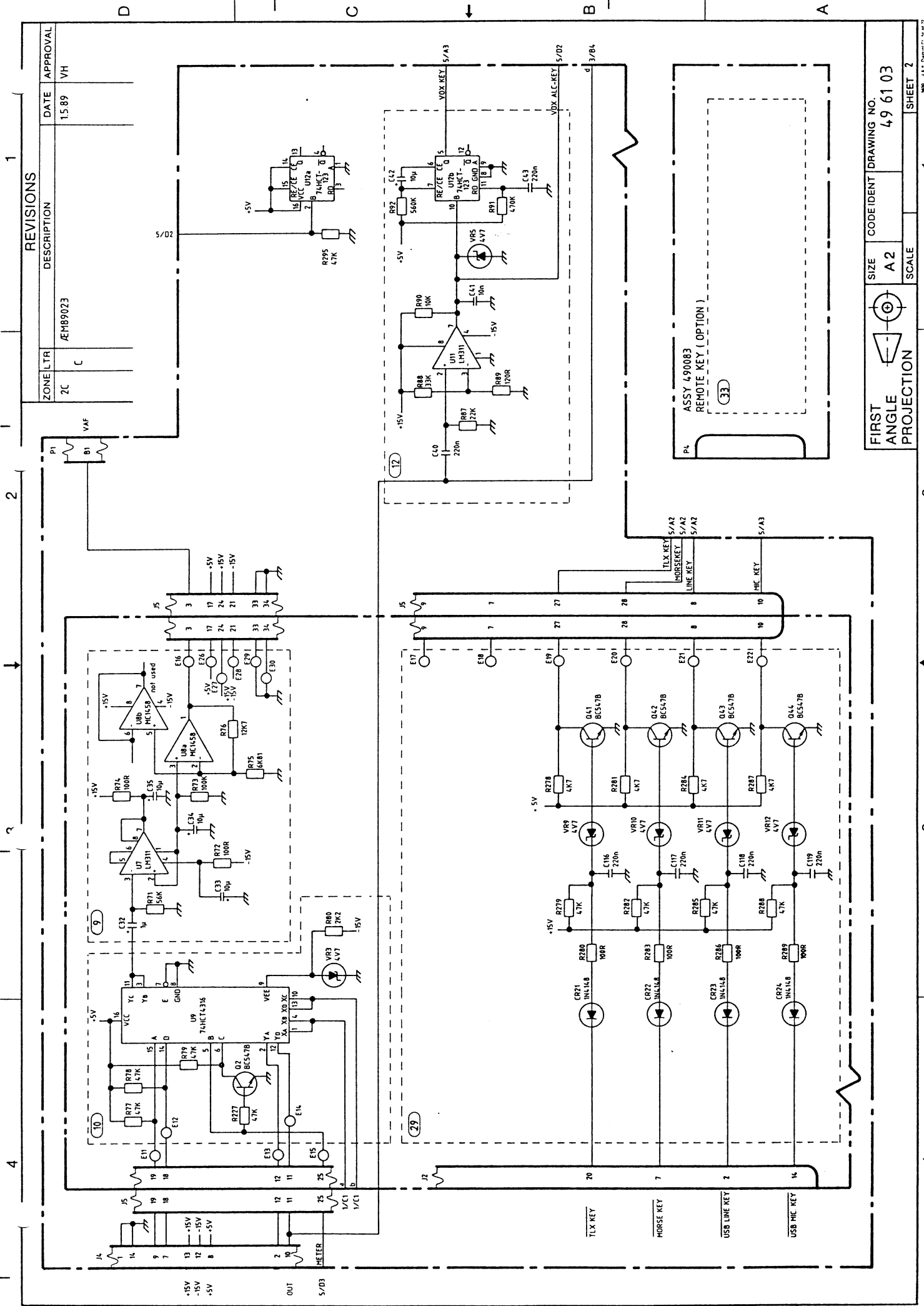


REVISIONS

ZONE/LTR	DESCRIPTION	APPROVAL
B	AEH89023 89011, 89013	VH
C	AEH89044	VH
S	AE09010, AE09073	VH
S5	AE09146	VH /G4/S
E	AE09146	VH/G4/S
F	AE09393	VH/G4/S

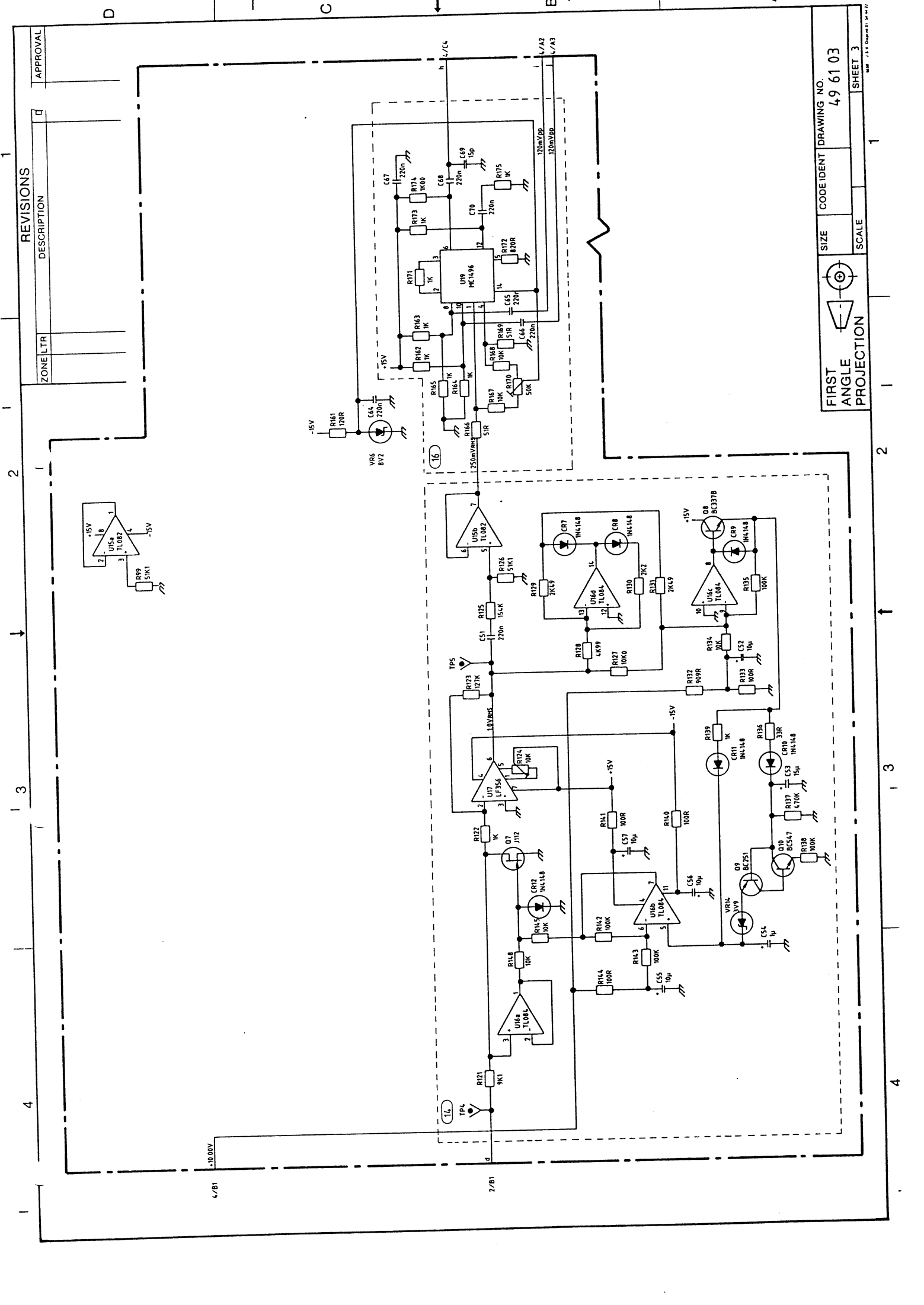
Dansk Radio AS

DR.	VH 4,11 1988	TITLE	MODULATOR A7, SSB SE4010
CH.		SIZE	A2
AP.		CODE IDENT	DRAWING NO. 49 61 03
AP.		SCALE	SHEET 1 OF 5
FIRST ANGLE PROJECTION		APPLICATION	
MATERIAL		USED ON	
48 81 00		NEXT ASSY	
ANGLES LIN. DIM.		APPLICATION	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLI- METERS AND TOLERANCES ARE IN ACCORDANCE WITH DS 2075		APPLICATION	



REVISIONS			
ZONE/LTR	DESCRIPTION	DATE	APPROVAL
2C	ÆM89023	15.89	VH
C			

FIRST ANGLE PROJECTION	SIZE A2	CODE/IDENT DRAWING NO. 49 61 03	SHEET 2
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REVISIONS	
ZONE/LTR	DESCRIPTION

APPROVAL

FIRST ANGLE PROJECTION

SIZE

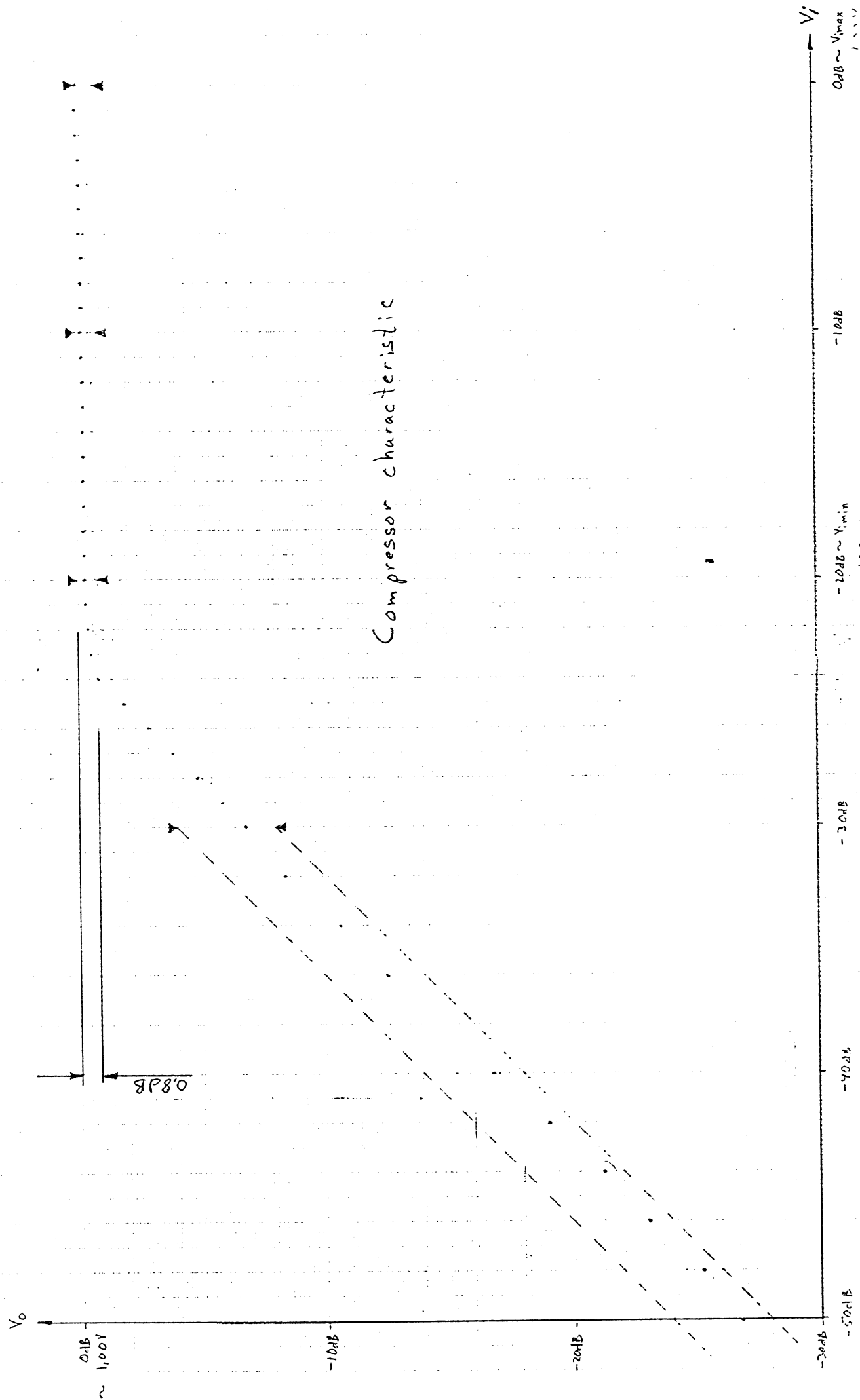
CODE IDENT

DRAWING NO.
49 61 03

SCALE

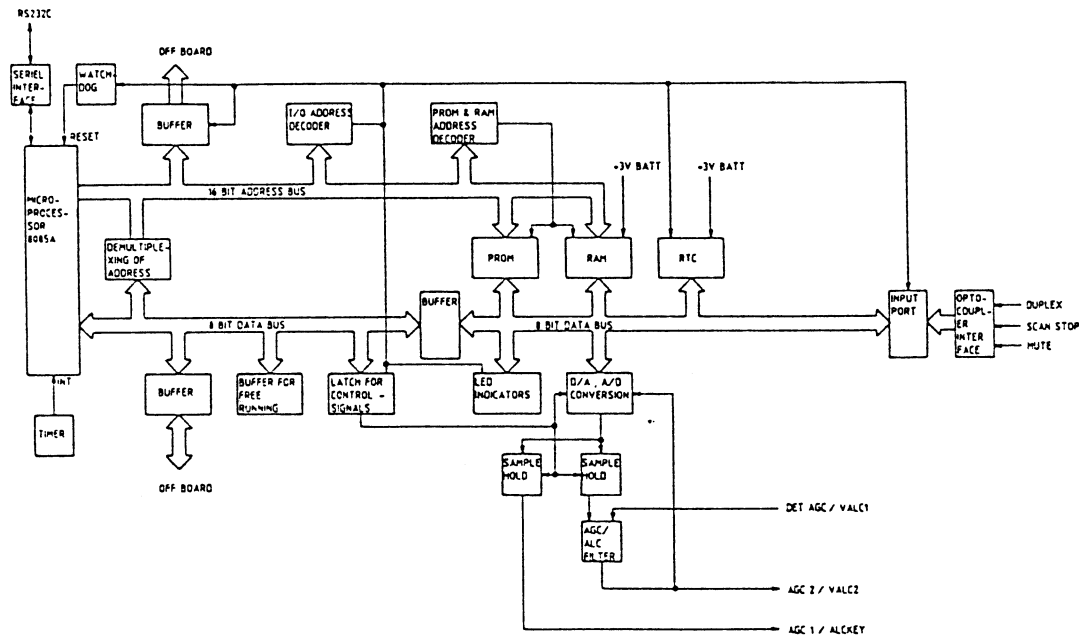
SHEET 3

DATE: 11.8.2008 BY: M. R. J.



MICROCOMPUTER ASSEMBLY A8/SE4010

The functional block diagram of the Microcomputer Assembly is shown below:



The assembly consists of a 8085 microprocessor large scale integrated circuit that controls all basic functions within the exciter.

The operating system software for the microcomputer is stored in three programmable read-only memories (PROM's). Each PROM is capable of storing 16K x 8-bit words.

A random access memory chip (RAM), capable of storing 8k x 8-bit words, is required for the temporary storage and manipulation of input and output data. During power failure and receiver standby, the RAM is powered from a 3V battery backup preventing interruptions from disturbing the stored data.

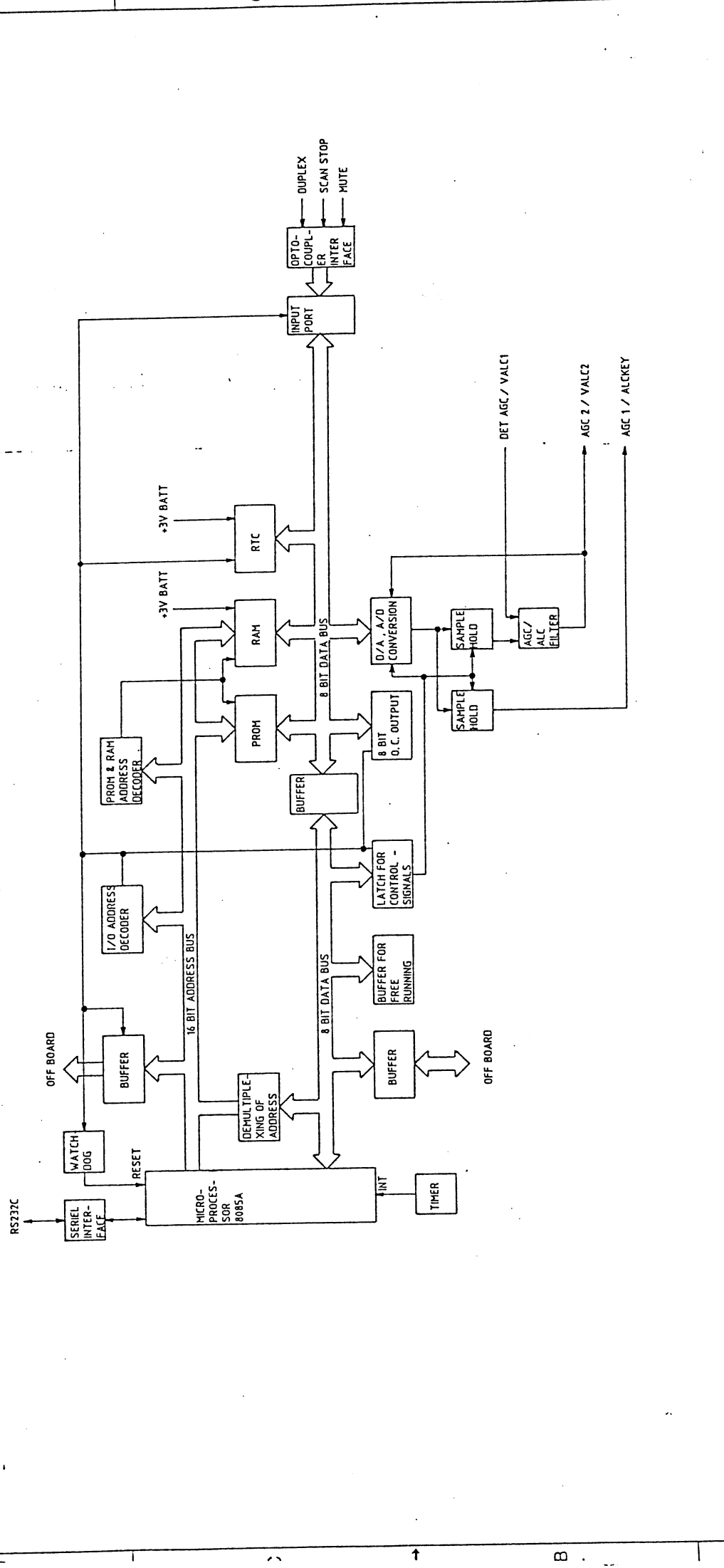
Various buffers and decoders assure proper drive levels and timing to and from various circuits and input/output ports.

A battery back-upped real time clock integrated circuit is mounted to ensure correct time keeping even during power failure or exciter standby.

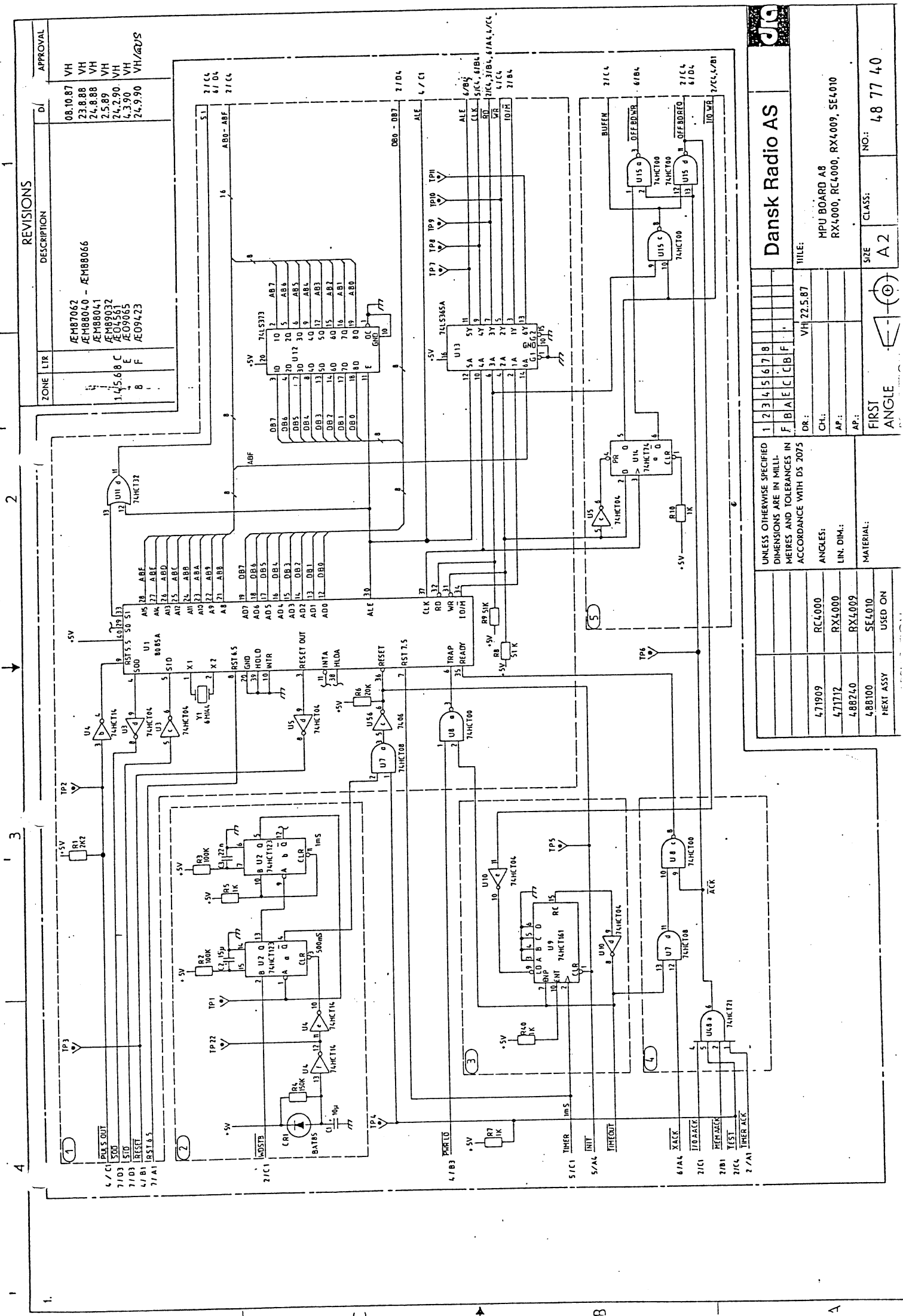
Timing of the Assembly is via a 6.144MHz crystal oscillator contained in the CPU.

The Microprocessor Assembly performs the automatic level control ALC. Analogue loops provides fast attack ALC-levels for the IF assembly. The peak voltage of VALC1 is held by a sample and hold circuit. As long as ALCKEY is a logical "1", the microcomputer will approach VALC2 to VALC1.

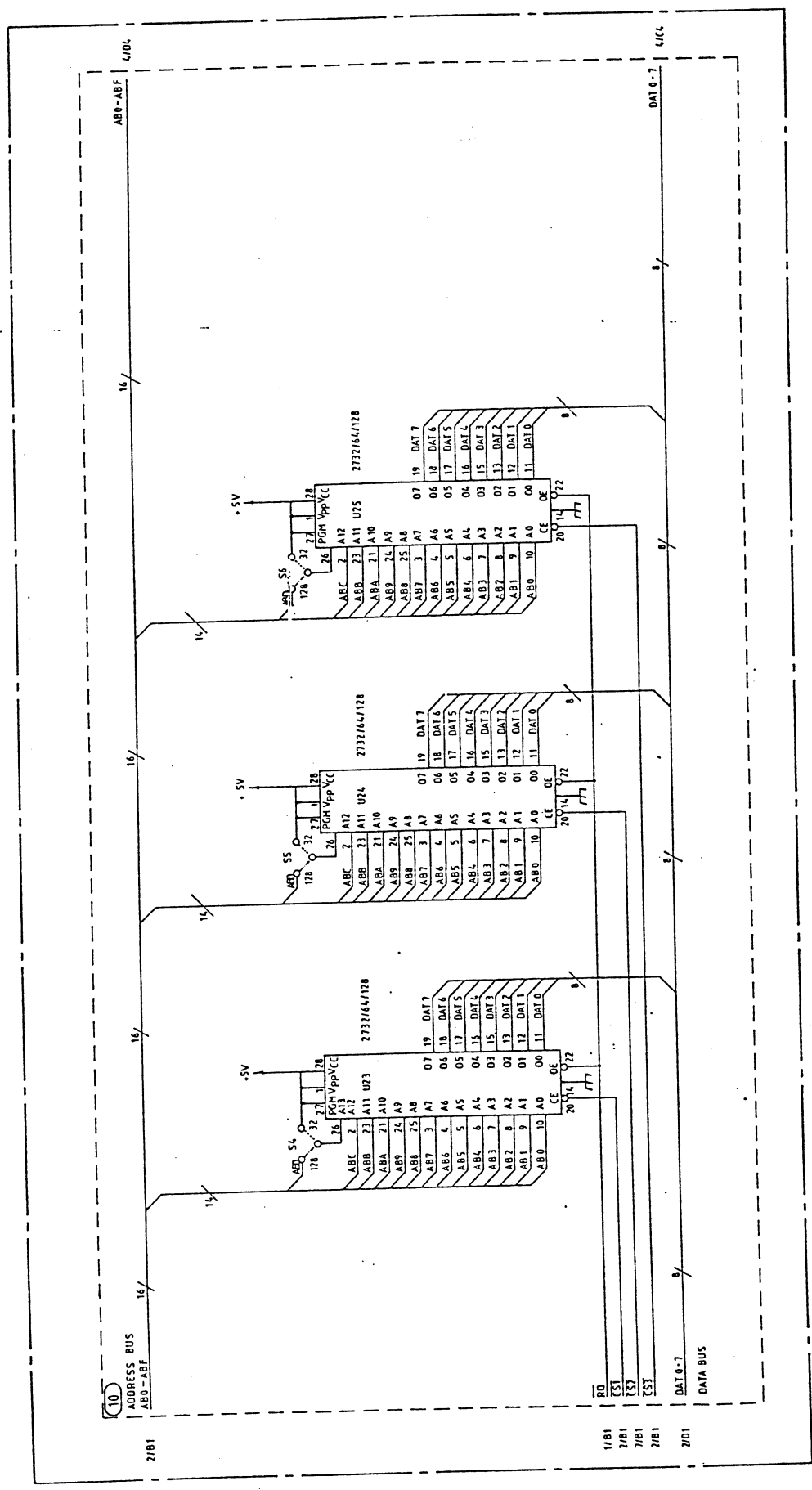
REVISIONS			APPROVAL
ZONE	DESCRIPTION		
1			
2			
3			
4			



Dansk Radio AS		TITLE	
		DR.	VH 22.5.87
		CH.	
		AP.	M/F 11.05.87
		AP.	
		CONFIGURATION	
		MPU BOARD	
		RC4000, RX4000, RX4009, SE4010	
		SIZE	A2
		CODE IDENT	
		DRAWING NO.	48 77 40-B
		FIRST ANGLE	
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETRES AND TOLERANCES ARE IN ACCORDANCE WITH DS 2075	
		ANGLES	
		LIN. DIM.	
		MATERIAL	
471909	RC4000		
471712	RX4000		
488240	RX4009		
488100	SE4010		
		NEXT ASSY USED ON	



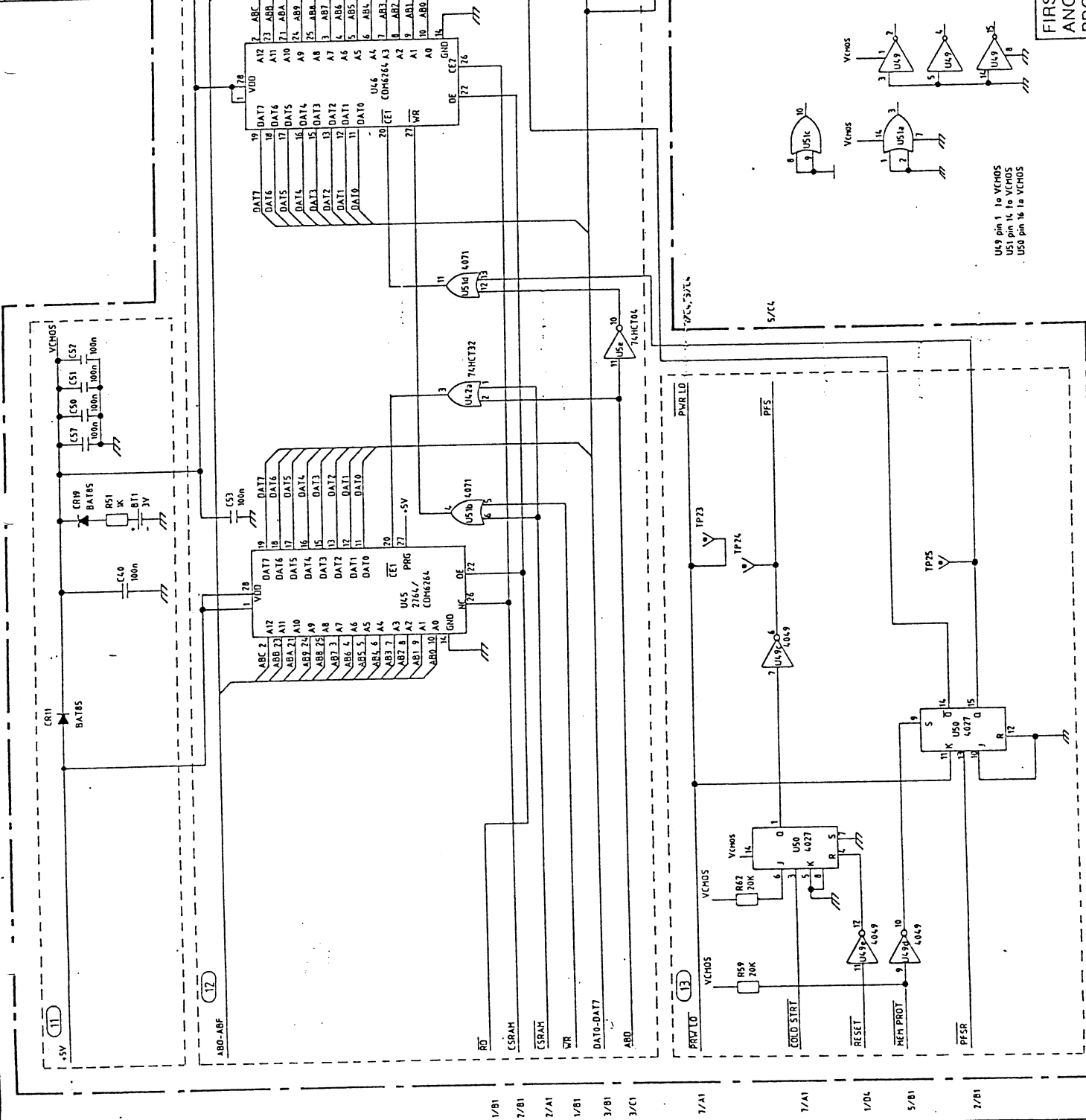
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2				
3				
4				



--- 27128
 2732

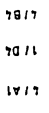
REVISIONS

ZONE/LTR	DESCRIPTION	DATE	APPROVAL
	DEM87062, DEM87067	08.10.87	VH
	DEM88110	18.11.88	VH
	DEM89032	25.89	VH
	DEM04561	24.2.90	VH
	DEM09065	4.3.90	VH

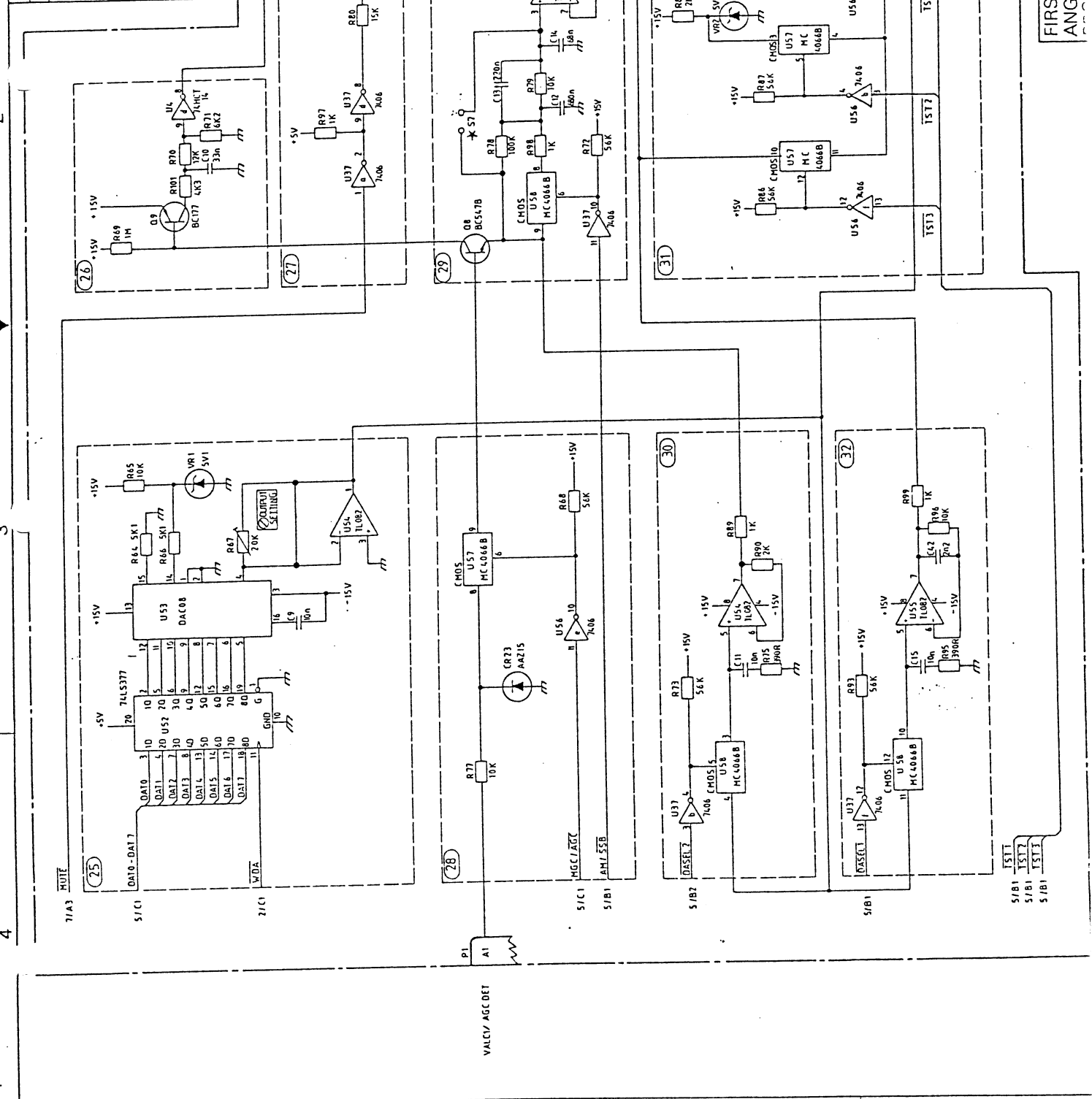


★ ONLY MOUNTED WHEN USING A RTC WHITOUT BUILT IN X-TAL

9.10.87	VH	APPROVAL
3.5.89	VH	

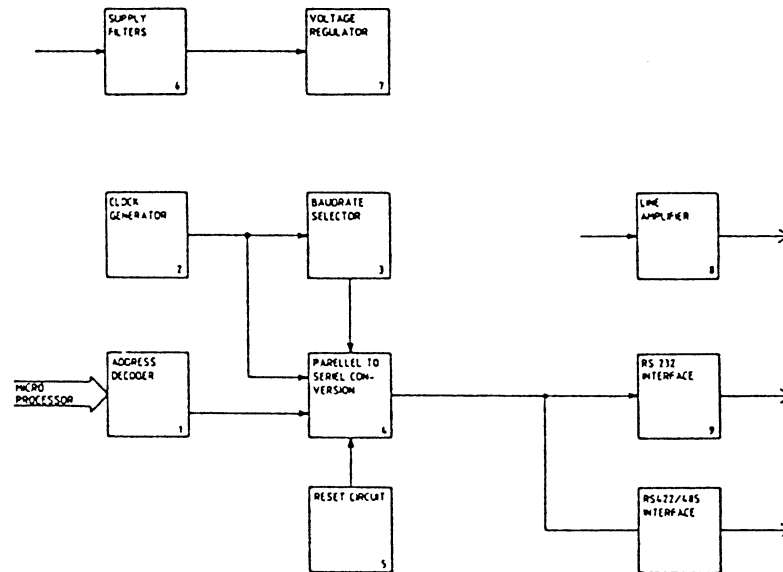


REVISONS		DESCRIPTION
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		ÆM87062
		ÆM88040
		ÆM88035, 88041
		ÆM88110
		ÆM89032
		ÆOL561
		Æ09423
	C	
	F	



REMOTE MODULE A9/SE4010

The functional block diagram of the Remote Interface Assembly is shown below:



The clock generator (2) running at 6.144 MHz delivers clock pulses to the parallel to serial conversion circuit (4) with a frequency of 1.2288 MHz. The baudrate generator (3) controls the baudrate of the remote communication. The parallel to serial conversion circuit (4) interfaces the serial databus to an 8-bit databus which is controlled by the microprocessor of the equipment via the address decoder (1). The serial databus is converted to RS232C, RS422 or RS485 levels in the interface circuits. A balanced line output (8) is available when the module is installed in an RX4010 receiver.

ZONE	UTR	DESCRIPTION	DATE	APPROVAL

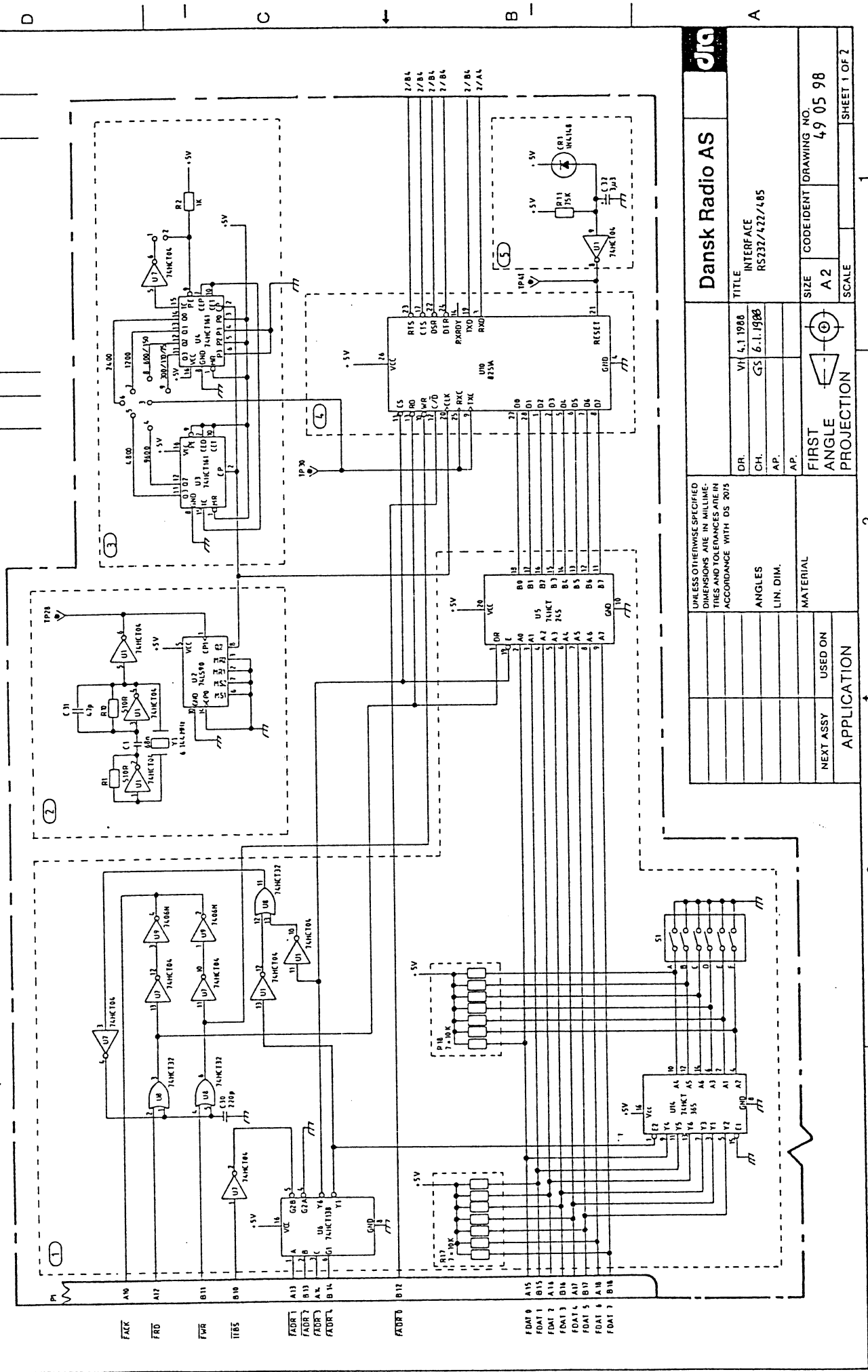
REVISIONS

1

2

3

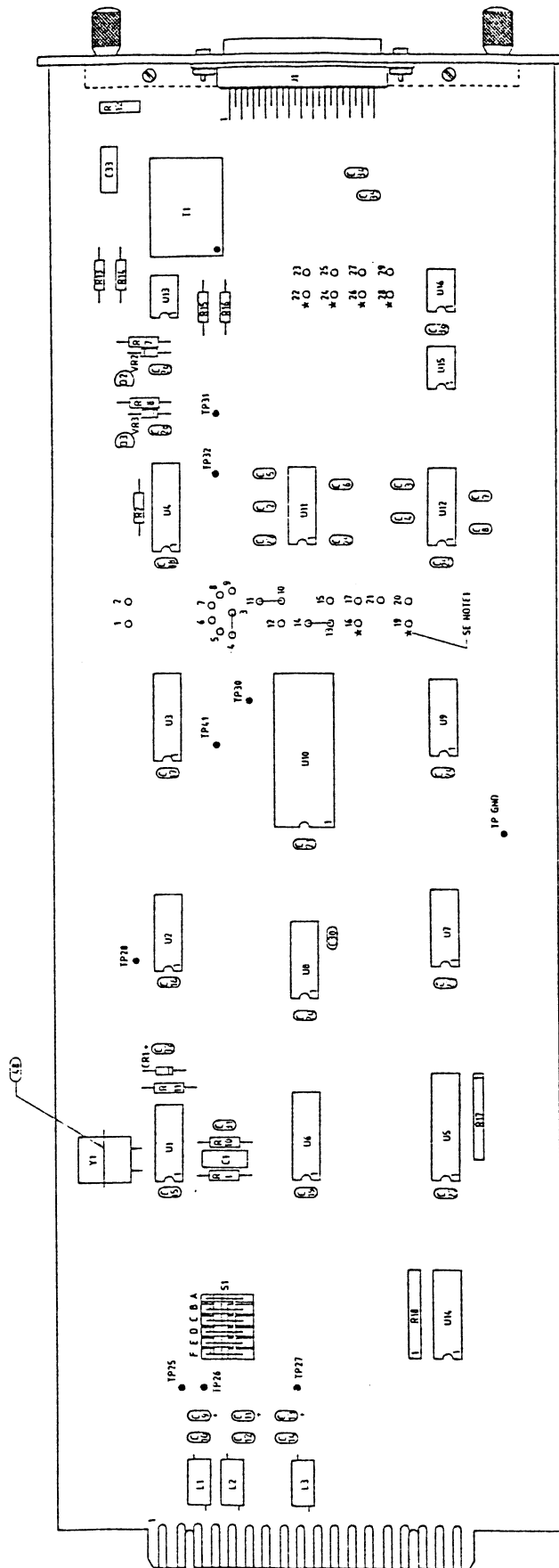
4



Dansk Radio AS		TITLE	
INTERFACE		RS232/422/485	
DR.	VH 4.1.1988	CH.	GS 6.1.1988
AP.		AP.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLI- METERS AND TOLERANCES ARE IN ACCORDANCE WITH DS 2075		FIRST ANGLE PROJECTION	
APPLICATION		MATERIAL	
NEXT ASSY		USED ON	
SIZE		CODE IDENT	
A2		DRAWING NO.	
SCALE		49 05 98	
SHEET 1 OF 2		1	

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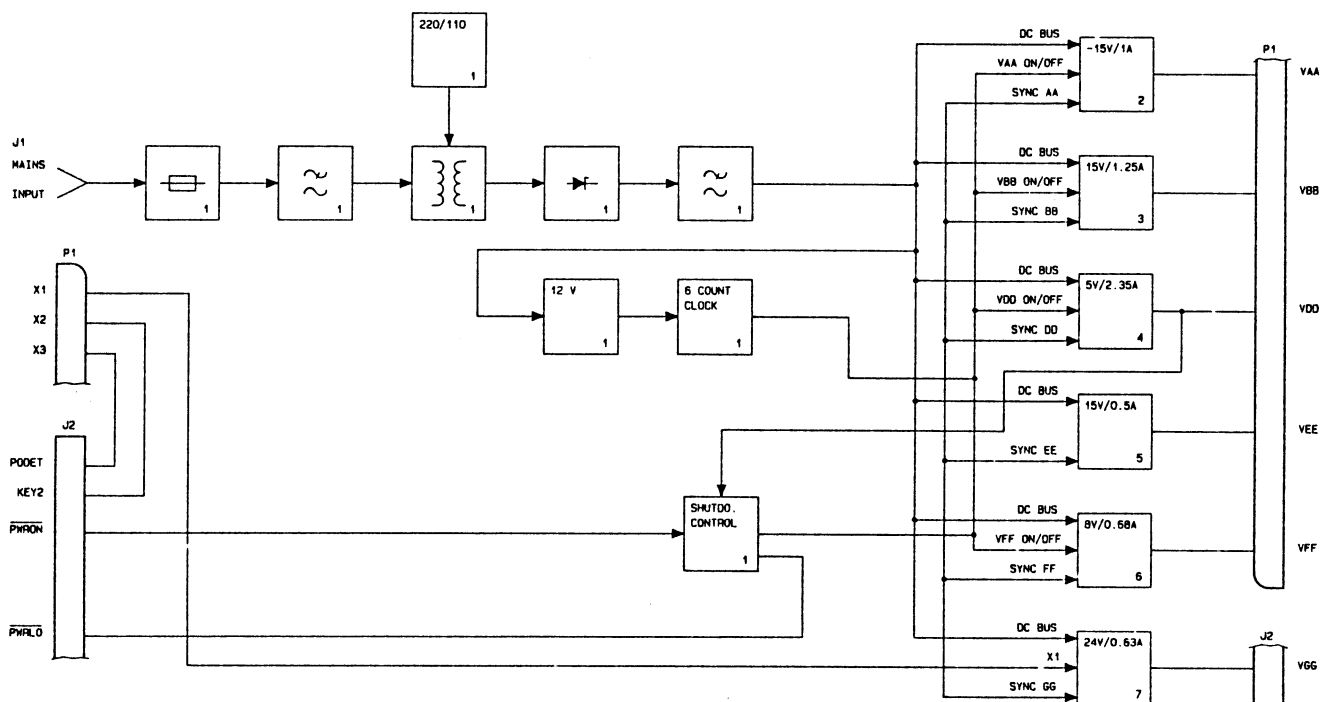
REVISIONS		DATE	APPROVAL
ZONE	TR		
A	B	409659	VII
C	C	409641	VII
D	D	408838	VII



Dansk Radio AS		TITLE	
Dansk Radio AS		COMPONENT LOCATION	
Dansk Radio AS		INTERFAC	
Dansk Radio AS		R533/437/435	
Dansk Radio AS		SITE	
Dansk Radio AS		CORE IDENT	
Dansk Radio AS		DRAWING NO	
Dansk Radio AS		49 05 98	
Dansk Radio AS		SHEET 1 OF 1	
Dansk Radio AS		SCALE 1:1	
Dansk Radio AS		FIRST ANGLE PROJECTION	
Dansk Radio AS		UNLESS OTHERWISE SPECIFIED	
Dansk Radio AS		DIMENSIONS ARE IN MILLIMETERS	
Dansk Radio AS		TOLERANCES UNLESS OTHERWISE SPECIFIED	
Dansk Radio AS		FRACTIONAL ANGLES	
Dansk Radio AS		UN DIM	
Dansk Radio AS		MATERIAL	
Dansk Radio AS		USED ON	
Dansk Radio AS		APPLICATION	
Dansk Radio AS		MATERIAL	
Dansk Radio AS		APPLICATION	

POWER SUPPLY A10/SE4010

The functional block diagram of the Power Supply Assembly is shown in the figure below.



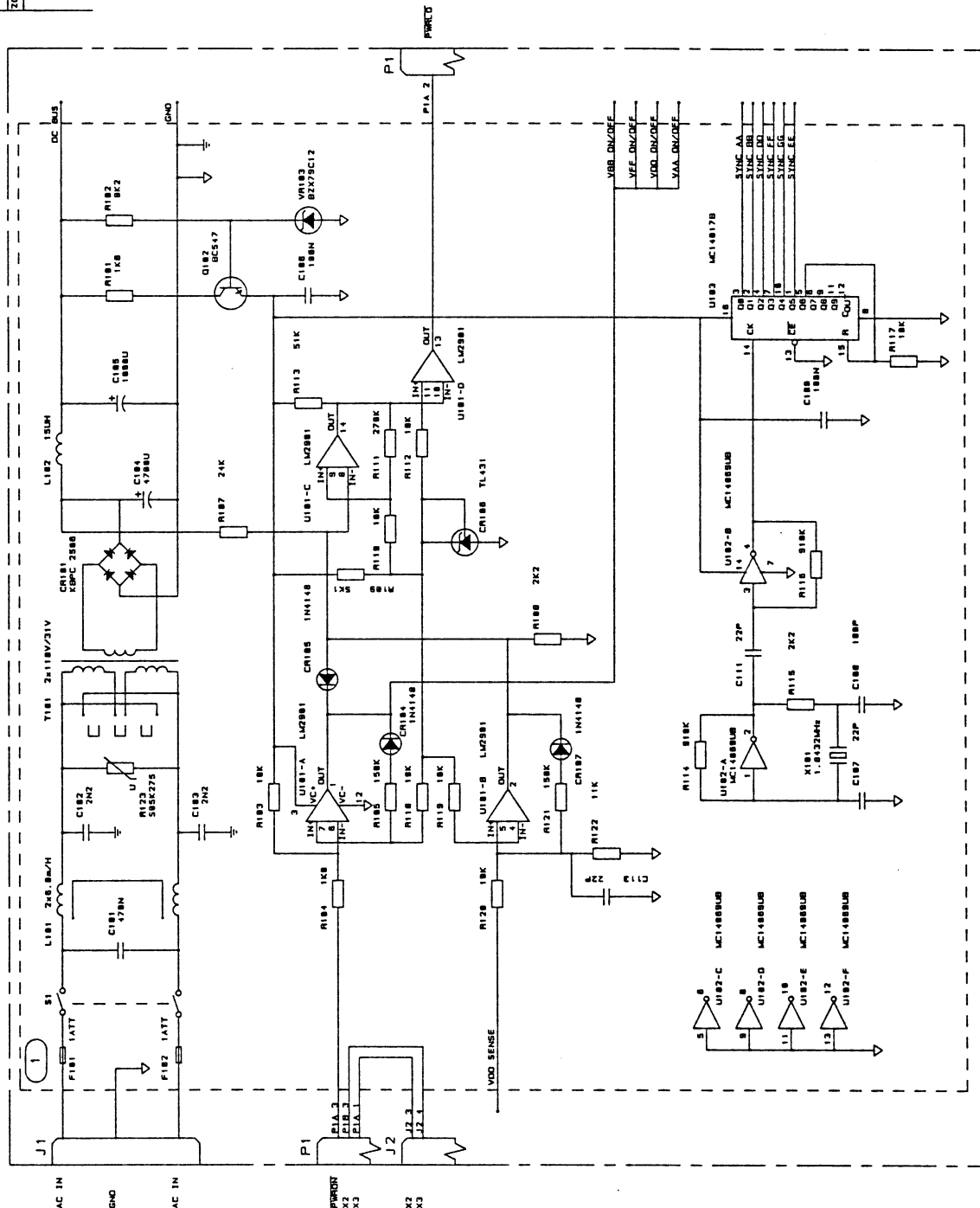
The Power Supply Assembly is a secondary switch mode power supply with 6 output voltages and a total of 70W output power. A secondary switch mode power supply is a power supply where the mains is connected through a transformer, giving the galvanic insulation between input and output.

Block 1 contains the transformer, rectifier and filter and a 6-phase clock used for the 6 regulators. Blocks 2 to 7 contain the regulators for the 6 different output voltages. Further block 1 contains the Shutdown control, which controls the 5 regulators. The 6th regulator, 5 giving VEE can only be shut down by switching off the mains. The signal PWRON energize the regulators giving VAA, VBB, VDD and VFF, while the regulator giving VGG is controlled by the signal X1.

All the regulators are overvoltage protected, as well as current limited.

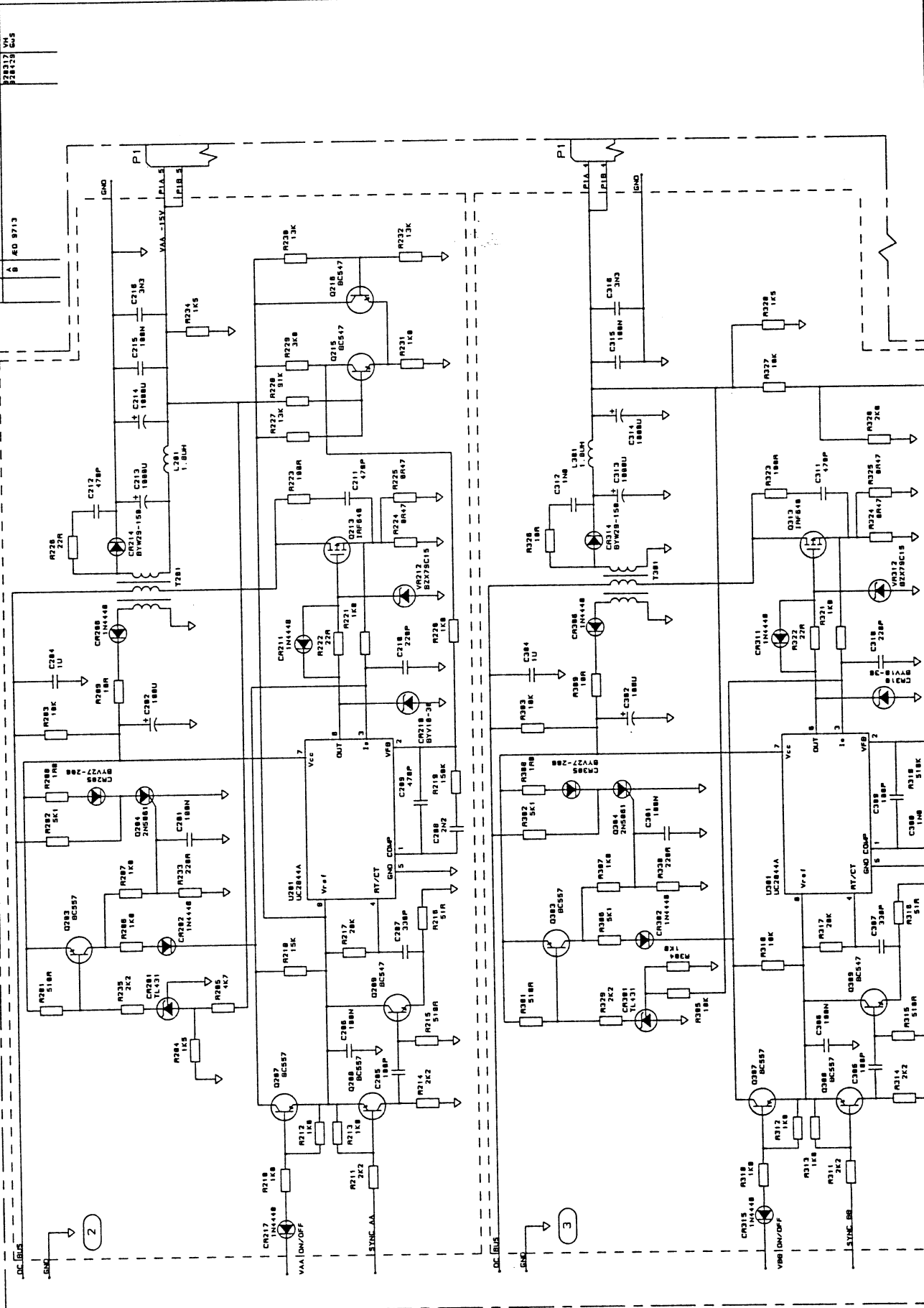
REVISIONS

ZONE	LTN	DESCRIPTION	DATE	APPROVAL
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B			28312	VM
C			28312	VM

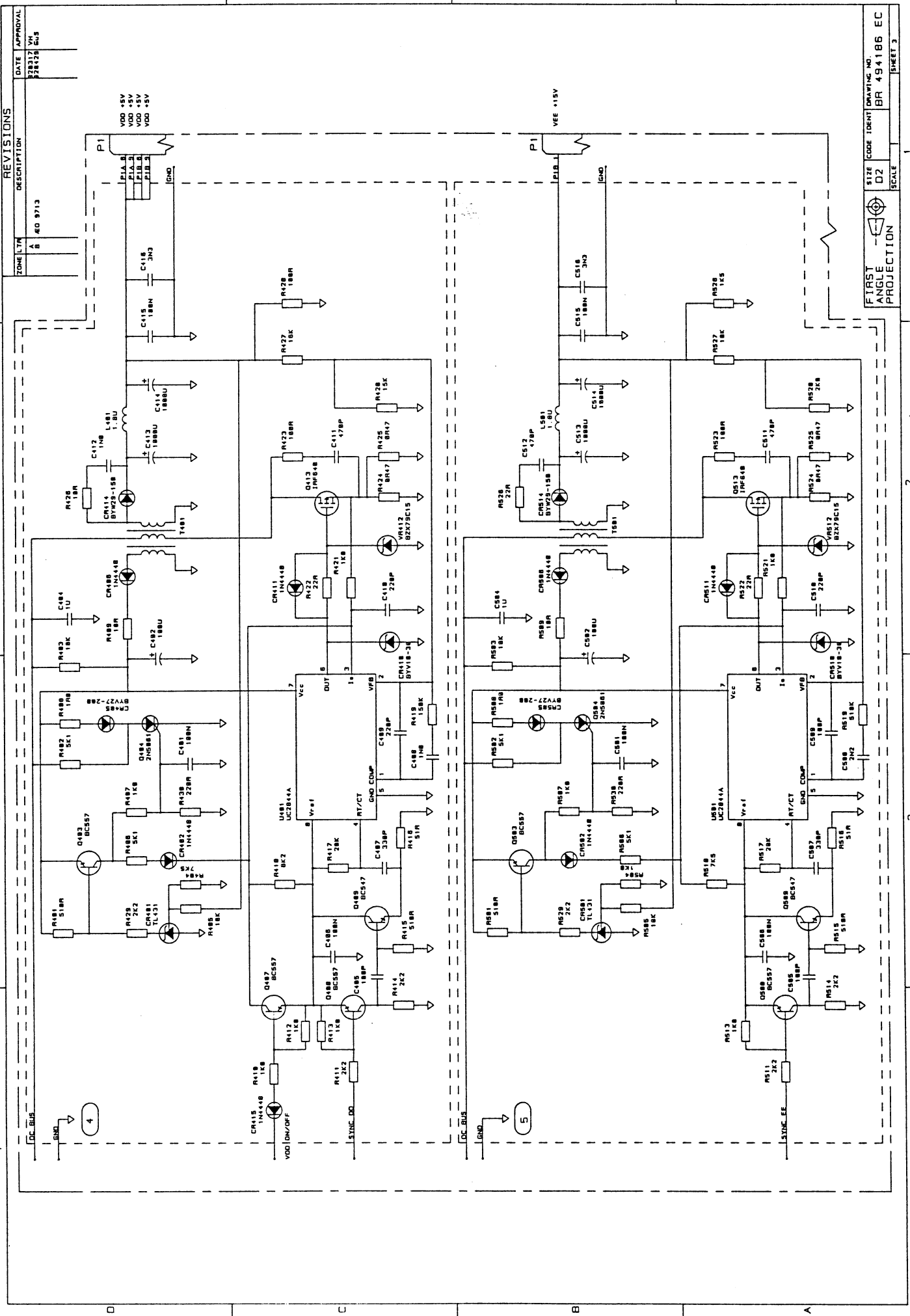


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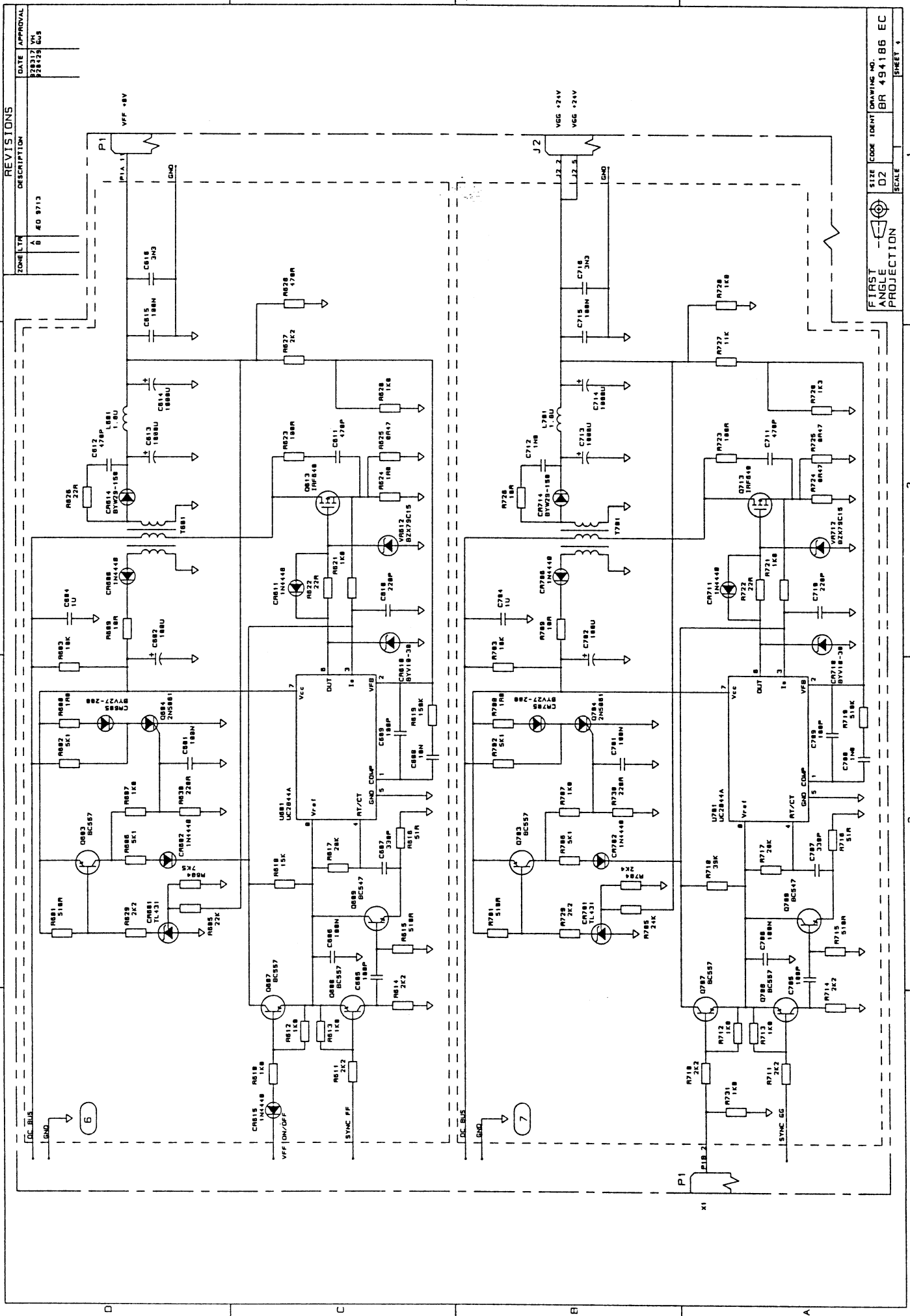
REVISIONS	DATE	APPROVAL
1	28/3/73	WJ
2	28/3/73	WJ
3	28/3/73	WJ
4	28/3/73	WJ



SIZE	CODE	IDENT	DRAWING NO.
D2			BR 494186 EC
SCALE	PROJECTION	FIRST ANGLE	SHEET 2



REVISIONS			DATE	APPROVAL
1	DESCRIPTION	228317 VM	40 97/3	
2		228317 VM		
3		228317 VM		
4		228317 VM		

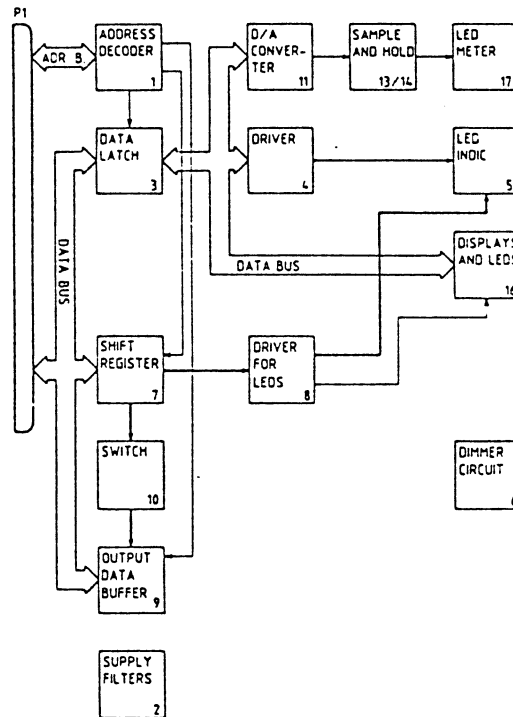


REVISIONS		
ZONE	DESCRIPTION	DATE
A	40 3713	228317
B		228425

FIRST ANGLE PROJECTION	SCALE	SHEET 1
SIZE	CODE	IDENT
D2	BR	494186 EC

FRONT PANEL A11/SE4010

The functional block diagram of the front panel assembly is shown in the figure below:



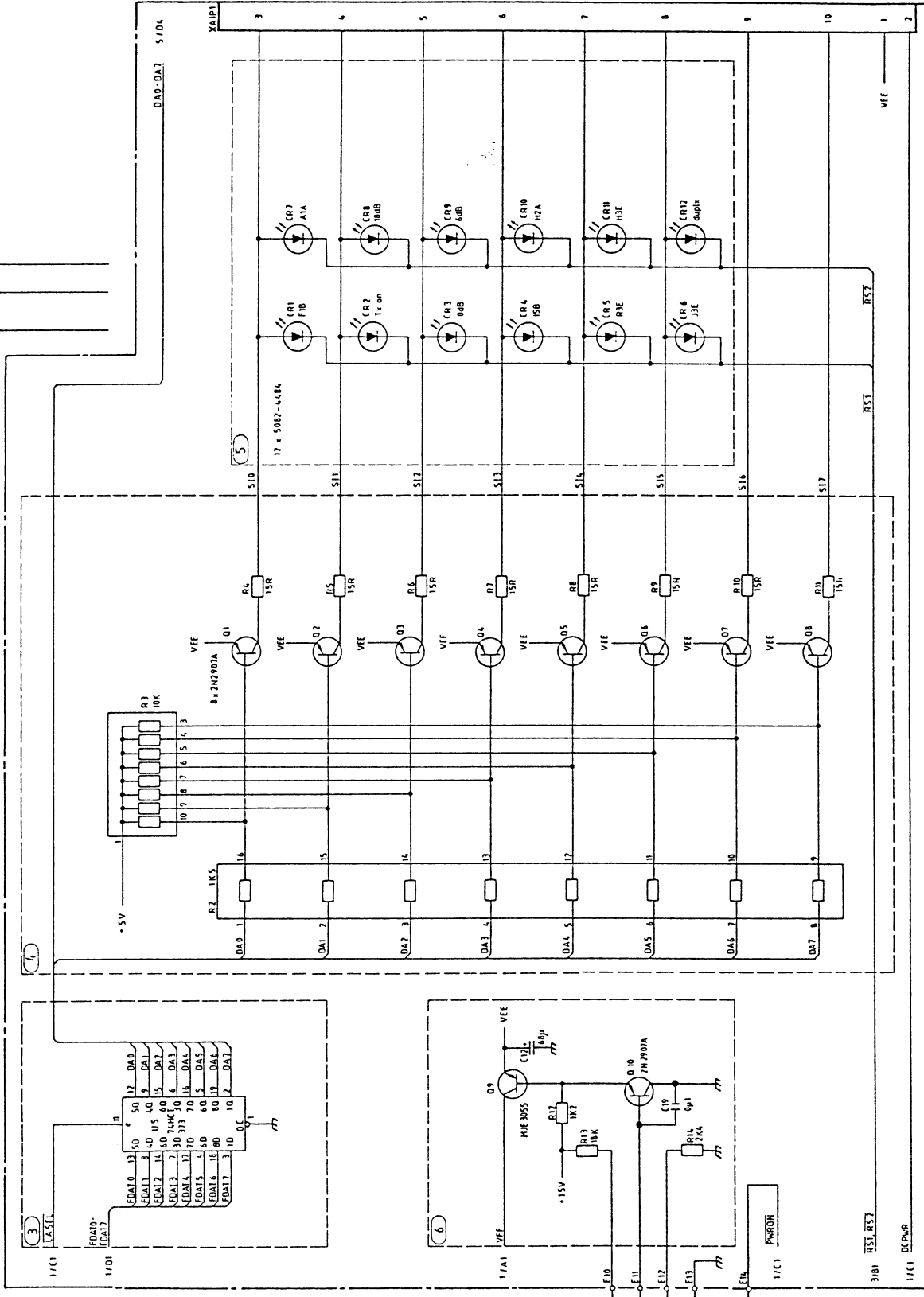
The front panel assembly mounts and interconnects most of the front panel controls, including power ON/OFF dimmer, mode-, key-, meter- and power select. The LEDs and meter read-outs are also mounted on this assembly.

All digital controlled push buttons are scanned by the Microcomputer Assembly. The LED read-outs and the front panel meter are synchronously updated.

A single ribbon cable interconnects the assembly to the exciter mother board.

REVISIONS

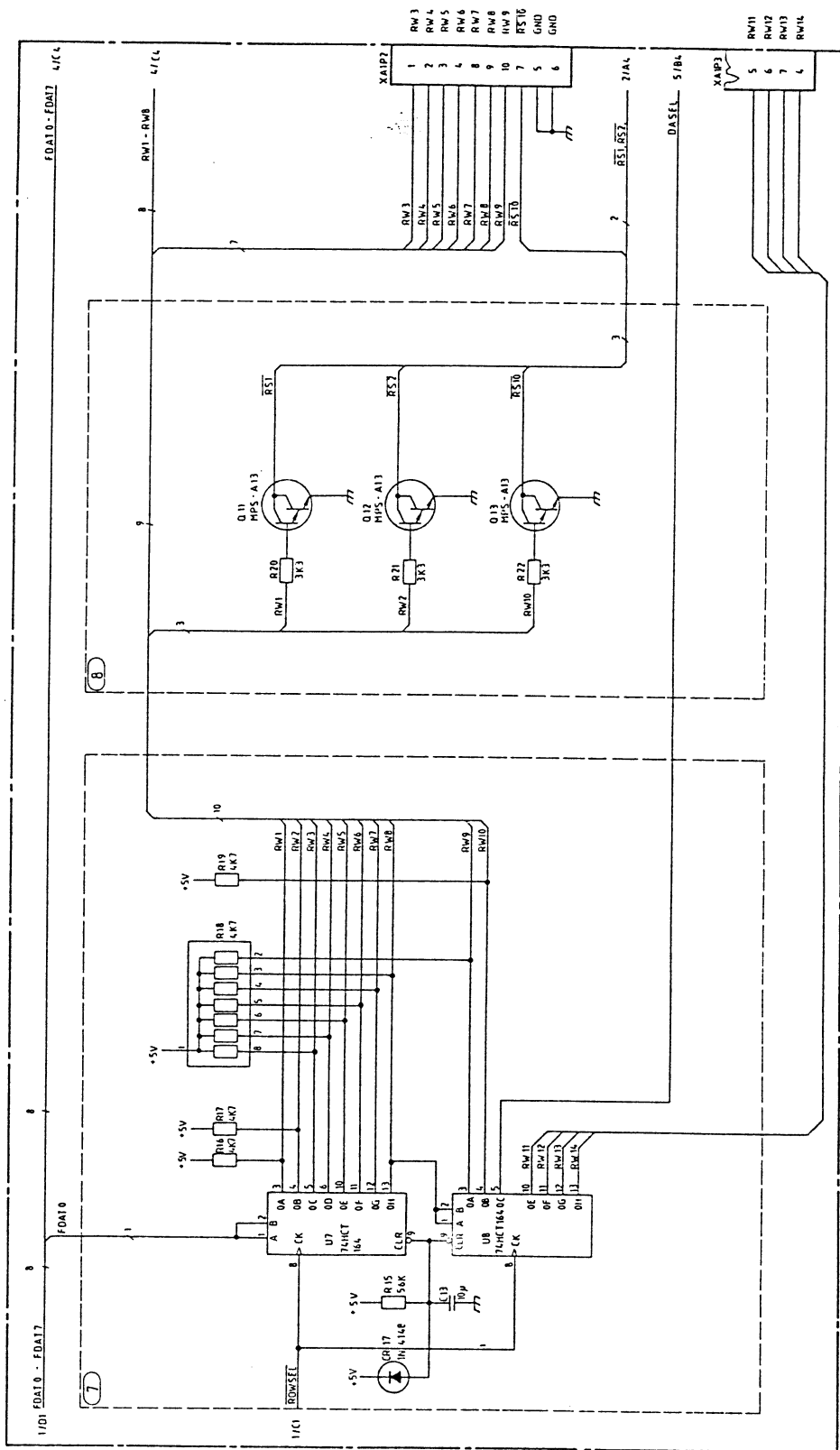
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
A				
B		REVISED	20.10.88	VH



SIZE	CODE IDENT NO	DRAWING NO
1	48 83 56	48 83 56
SCALE	SHEET 2	

FIRST ANGLE PROJECTION

<p>FIRST ANGLE PROJECTION</p>	<p>SIZE</p>	<p>CODE IDENT NO</p>	<p>DRAWING NO 48 83 56</p>	<p>SHEET 3</p>
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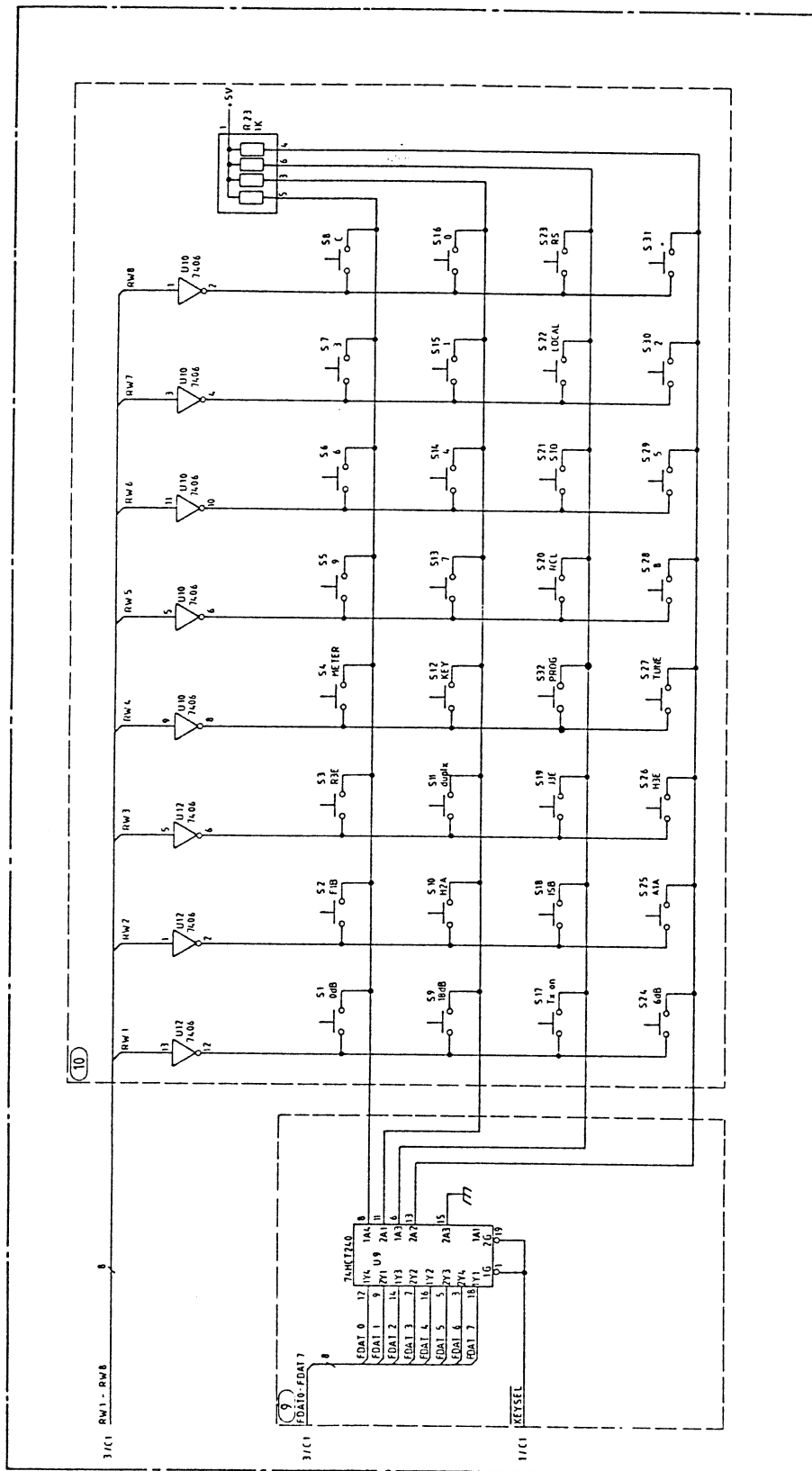



REVISIONS

ZONIF	11R	DESCRIPTION	DATE	APPROVAL
A		B REVISED	20.10.88	VH

REVISIONS		
ZONE	LTR	DESCRIPTION
B4	A	REVISED
	B	REVISED
	C	REVISED

DATE	APPROVAL
13.9.88	VH
20.10.88	VH



		DRAWING NO 48 83 56	
FIRST ANGLE PROJECTION		CODE IDENT NO	SHEET 4
SIZE		SCALE	

SELF TEST AND PROGRAM FACILITIES SE4010

The Program Function

The program function is selected by pressing the [PROGR] key followed by the program number. The program number is accepted by pressing the [enter] key.

The operation of the programs can be illustrated in this way:

1) Select the program.

2) The main menu will be displayed.

main menu

3) The menus are scrolled by [←] and [→] keys.

main menu <—> sub menu 1 <—> sub menu 2 <—>

4) The first message is displayed when a menu is selected by pressing [enter] while the menu is shown.

message 1

5 Sub messages may be scrolled by using [←] and [→] keys.

message 1 <—> sub mess.1.1 <—> sub mess.1.2 <—>

6) Messages are scrolled by using the down arrow and the up arrow keys.

message 1 <—> sub mess.1.1 <—> sub mess 1.2 <—>

*
*
*

message N <—> sub mess.N.1 <—> sub mess.N.2 <—>

7) Pressing the down arrow keys after the last message returns the SE4010 to the former setting.

SELF TEST AND PROGRAM FACILITIES SE4010

SE4010 Programs

Program 1: 24 hours clock.

Program 30: F1B audio frequency offset.

Program 31: Selection of data side band in B9W mode, not applicable.

Program 34: FSK Modulator (A6) frequency selection, not applicable.

Program 35: FSK Modulator (A6) on/off, not applicable.

Program 40: AEL Automatic Error Log.

Program 41: ARTEL Automatic Remote Transmission Error Log.

Program 42: Accumulated On-time.

Clock Viewing and Setting

Program 1

Display and setting of clock used for alarm functions.

F1B Audio Frequency Offset

Program 30

In a F1B transmission the center frequency of the two tones is normally transmitted as the displayed frequency. Program 30 allow programming of audio center frequencies in steps of 10 Hz.

Selection of data side band in B9W mode

Program 31

Not applicable using SSB version of SE4010.

FSK Modulator (A6) frequency selection

Program 34

Not applicable.

FSK Modulator (A6) on/off

Program 35

Not applicable.

SELF TEST AND PROGRAM FACILITIES SE4010

AEL Automatic Error Log

Program 40

Used to display faults in the synthex and the connected transmitter. The status are continuously monitored by the microprocessor in the synthex.

ARTEL Automatic Remote Transmission Error Log

Program 41

By installations where the equipment is remote-controlled, the quality of the remote transmission is continuously registered.

Accumulated On-time

Program 42

An internal counter in the synthex counts the number of hours the synthex has been switched on. Another counter counts the number of hours the transmitter has been switched on.

Self Test Program, manual

Program 49

Manual test of the exciter functionability.

Self Test Program, automatic

Program 49

Automatic test of the exciter functionability.

Clear All

Clears all user programmable channels and programs.

SELF TEST AND PROGRAM FACILITIES SE4010

Test Sequences of the Self Test

- a) If the remote module (A9) is present (option), the remote address of the SE4010 is displayed.
- b) Software version.
- c) Software options.
0000000 means no options.
- d) Key board test.
- e) LED and display test.
- f) (A8 module) Real Time Clock, DAC and SH circuit test.
- g) (A2 module) Standard Oscillator test.
- h) (A1 module) Synthesizer test.
- i) (A7A2 module) Remote Key test. (option)
- j) (A5 module) Interface module test.
- k) (ATU) Antenna Tuner test. (option)
- l) (A3 module) IF module test.
- m) (A7 module) Modulator module test.
- n) (A4 module) Wide Band Amplifier test.
- o) Assembly status.
- p) Test end. Return to setting displayed in the displays when entering the self test program.

SELF TEST AND PROGRAM FACILITIES SE4010

Key Values During Self-Test

KEY DEPRESSED	VALUE DISPLAYED
J3E	11
R3E	10
H3E	12
duplx	13
ISB	18
F1B	19
A1A	1A
H2A	1B
0dB	21
6dB	22
18dB	24
key	36
progr	38
meter	35
C	37
.	8A
0	80
1	81
2	82
3	83
4	84
5	85
6	86
7	87
8	88
9	89
rcl	31
sto	30

SELF TEST AND PROGRAM FACILITIES SE4010

Self-Test Fault Analysis Table

Error code			Fault Description
no	A1		A1 is not mounted.
Err	A1	1	A1 has not locked on 29999.99kHz: A1 or A2 defect.
Err	A1	2	A1 has not locked on 25000.00kHz: A1 or A2 defect.
Err	A1	3	A1 has not locked on 20000.01kHz: A1 or A2 defect.
Err	A1	4	A1 has not locked on 19999.99kHz: A1 or A2 defect.
Err	A1	5	A1 has not locked on 16000.00kHz: A1 or A2 defect.
Err	A1	6	A1 has not locked on 12000.01kHz: A1 or A2 defect.
Err	A1	7	A1 has not locked on 11999.99kHz: A1 or A2 defect.
Err	A1	8	A1 has not locked on 9000.00kHz: A1 or A2 defect.
Err	A1	9	A1 has not locked on 6000.01kHz: A1 or A2 defect.
Err	A1	10	A1 has not locked on 5999.99kHz: A1 or A2 defect.
Err	A1	11	A1 has not locked on 3000.00kHz: A1 or A2 defect.
Err	A1	12	A1 has not locked on 1500.00kHz: A1 or A2 defect.
Err	A1	13	A2 is not mounted.
no	A2		A2 is not mounted.
Err	A2	1	10.24MHz oscillator not oscillating: A2 defect.
Err	A2	2	73.6MHz loop has not locked: A2 defect.
Err	A2	3	1.4MHz loop has not locked: A2 defect.
no	A3		A3 is not mounted.
Err	A3	1	Test of A3 is not possible because A1 is missing.
Err	A3	2	Test of A3 is not possible because A1 has failed during test.
Err	A3	3	Test of A3 is not possible because A2 is missing.
Err	A3	4	Test of A3 is not possible because A2 has failed during test.
Err	A3	5	Test of A3 is not possible because A7 is missing.
Err	A3	6	Test of A3 is not possible because A5 is missing.
Err	A3	8	A1 has not locked: A1 is defect.
Err	A3	9	No input signal to A3: Cable between A7J1 and A3J4 defect or missing. A7 defect.

SELF TEST AND PROGRAM FACILITIES SE4010

Self-Test Fault Analysis Table, continued

Err	A3	10	No output signal from A3: Missing oscillator signals, defect cables or A3 defect.
Err	A3	11	Input signal to A3 when exciter is interlocked: A5 or A7 defect.
Err	A3	12	Output signal from A3 when exciter is interlocked: A5 or A7 defect.
Err	A3	13	No input signal to A3 after interlock reset: A3, A5 or A7 defect.
Err	A3	14	No output signal from A3 after interlock reset: A3 defect.
Err	A3	15	The Voltage Controlled Attenuator is defect: A3 defect.
Err	A3	16	The Voltage Controlled Attenuator has too much attenuation: A3 defect.
Err	A3	17	The Voltage Controlled Attenuator has too little attenuation: A3 defect.
Err	A3	18	Same as "Err A3 9".
Err	A3	19	ALC Reset defect: A3 defect.
Err	A4	1	Test of A4 is not possible because A1 is missing.
Err	A4	2	Test of A4 is not possible because A1 has failed during test.
Err	A4	3	Test of A4 is not possible because A2 is missing.
Err	A4	4	Test of A4 is not possible because A2 has failed during test.
Err	A4	5	Test of A4 is not possible because A3 is missing.
Err	A4	6	Test of A4 is not possible because A3 has failed during test.
Err	A4	7	Test of A4 is not possible because A5 is missing.
Err	A4	8	Test of A4 is not possible because A7 is missing.
Err	A4	9	Test of A4 is not possible because A7 has failed during test.
Err	A4	13	A1 has not locked: A1 defect.
Err	A4	14	A4 defect or missing.
Err	A4	15	The gain of A4 is too small: A4 defect.
Err	A4	16	A4 defect or missing.
no	A5		A5 is not mounted.
no	A7		A7 is not mounted.
no	A7A2		The Remote Key (option) is not mounted.
Err	A7A2		Conflicting data read: A7J4 bad. A7 or A7A2 defect.
Err	A7	2	Signal from Morsetone Generator through USB not detected: A5 or A7 defect.
Err	A7	3	Signal from Check Circuit through USB not received by A8: A7 defect.

SELF TEST AND PROGRAM FACILITIES SE4010

Self-Test Fault Analysis Table, continued

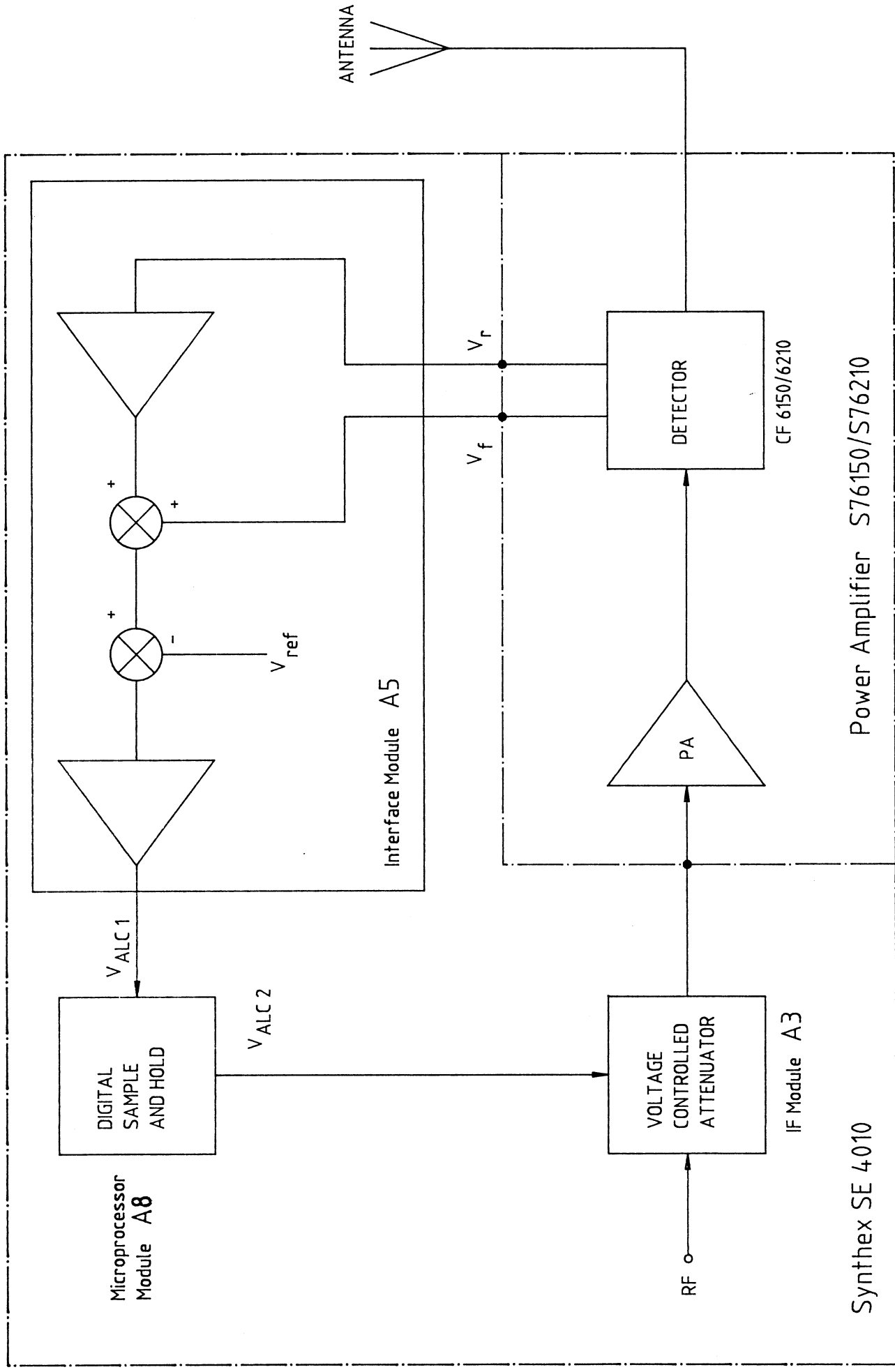
Err	A7	4	Signal from Morsetone Generator through LSB not detected: A5 or A7 defect.
Err	A7	5	Signal from Check Circuit through LSB not received by A8: A7 defect.
Err	A7	6	No USB output from A7: A7 defect. Cable between A7J1 and A3J4 defect or missing.
Err	A7	7	No LSB signal from A7: A7 defect. Cable between A7J1 and A3J4 defect or missing.
Err	A7	8	Test of A7 is not possible because A1 is missing.
Err	A7	9	Test of A7 is not possible because A1 has failed during test.
Err	A7	10	Test of A7 is not possible because A2 is missing.
Err	A7	11	Test of A7 is not possible because A2 has failed during test.
Err	A7	12	Test of A7 is not possible because A5 is missing.
Err	A8 clock		The Real Time Clock is defect: A8 defect.
Err	A8 dAC		D/A Converter defect: A8 defect.
Err	A8 StrP		A8 is not correct strapped.
no	ATU		The Antenna Tuner Controller (option) is not mounted in the Power Amplifier rack or the cables W102, W123 or W124 is bad or missing.
Err	ATU	1	The Antenna Tuner Controller is mounted. Conflicting status read: Antenna Tuner Controller or A5 defect.

SELF TEST AND PROGRAM FACILITIES SE4010

Error Codes

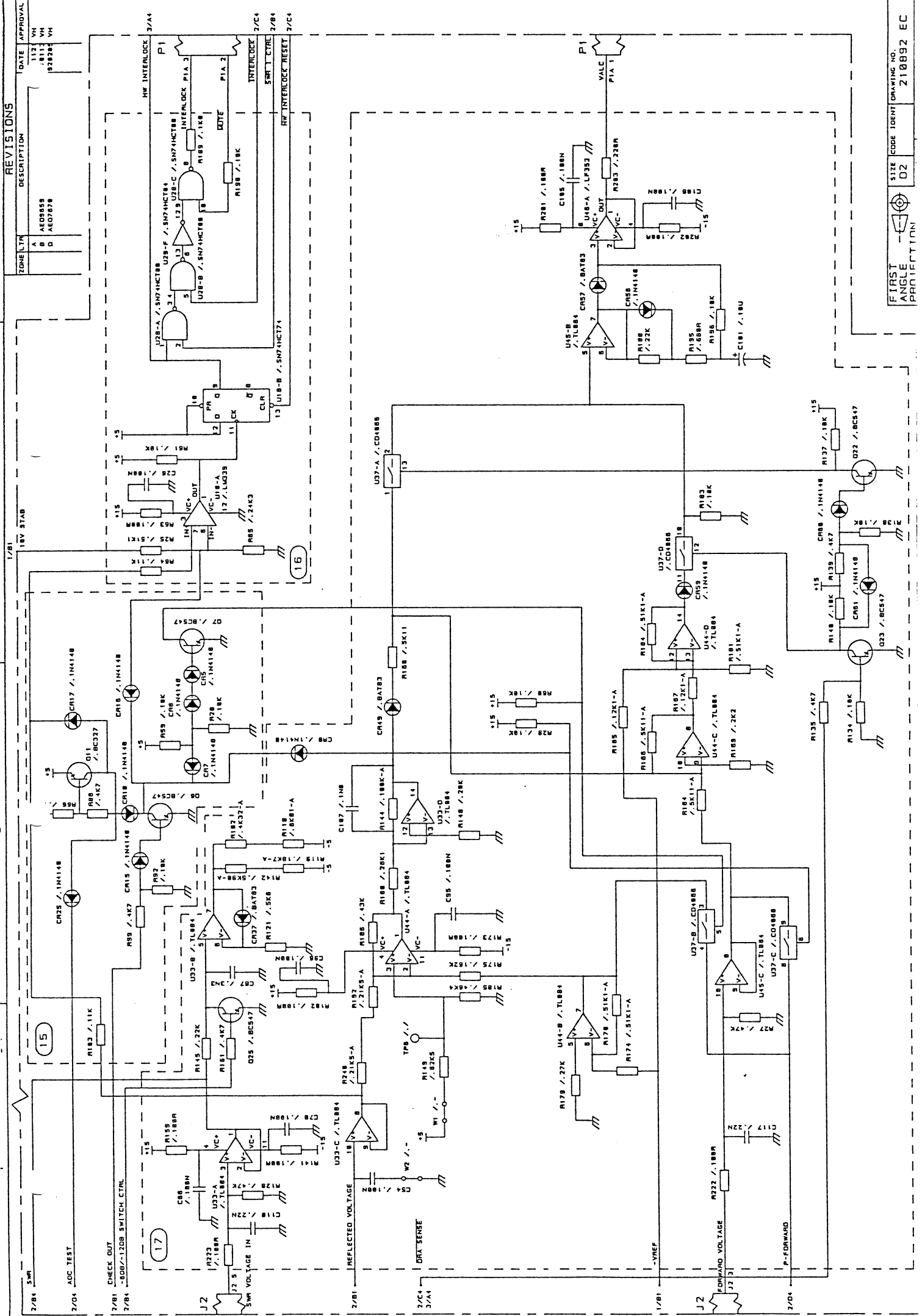
Error Codes	Remarks
Err. 1.4 LOC.	1.4 MHz loop on A2 out of lock
Err. 73.6 LOC.	73.6 MHz loop on A2 out of lock
Err. SYn. LOC.	76.5 - 105 MHz loop on A1 out of lock
Err. rEF. OSC.	Level from reference oscillator on A2 too low.
Err. PA. L.-1	Power Amplifier of upper PA drawer to the left switched off.
Err. PA. r.-1	Power Amplifier of upper PA drawer to the right switched off.
Err. PA. L.-2	Power Amplifier of lower PA drawer to the left switched off. (1 kW transmitter only).
Err. PA. r.-2	Power Amplifier of lower PA drawer to the right switched off. (1 kW transmitter only).
Err. PA. ALL	All Power Amplifiers switched off.
Err. Ant.rEF.	SWR greater than 5.
Err. A8 StrP	A8 strapped incorrectly.
Err. Atu.FAIL	Connected Antenna Tuner can not terminate tuning. Error message received from connected Antenna Tuner.
Err. Atu.dIS.	Antenna Tuner disconnected while mains is on.

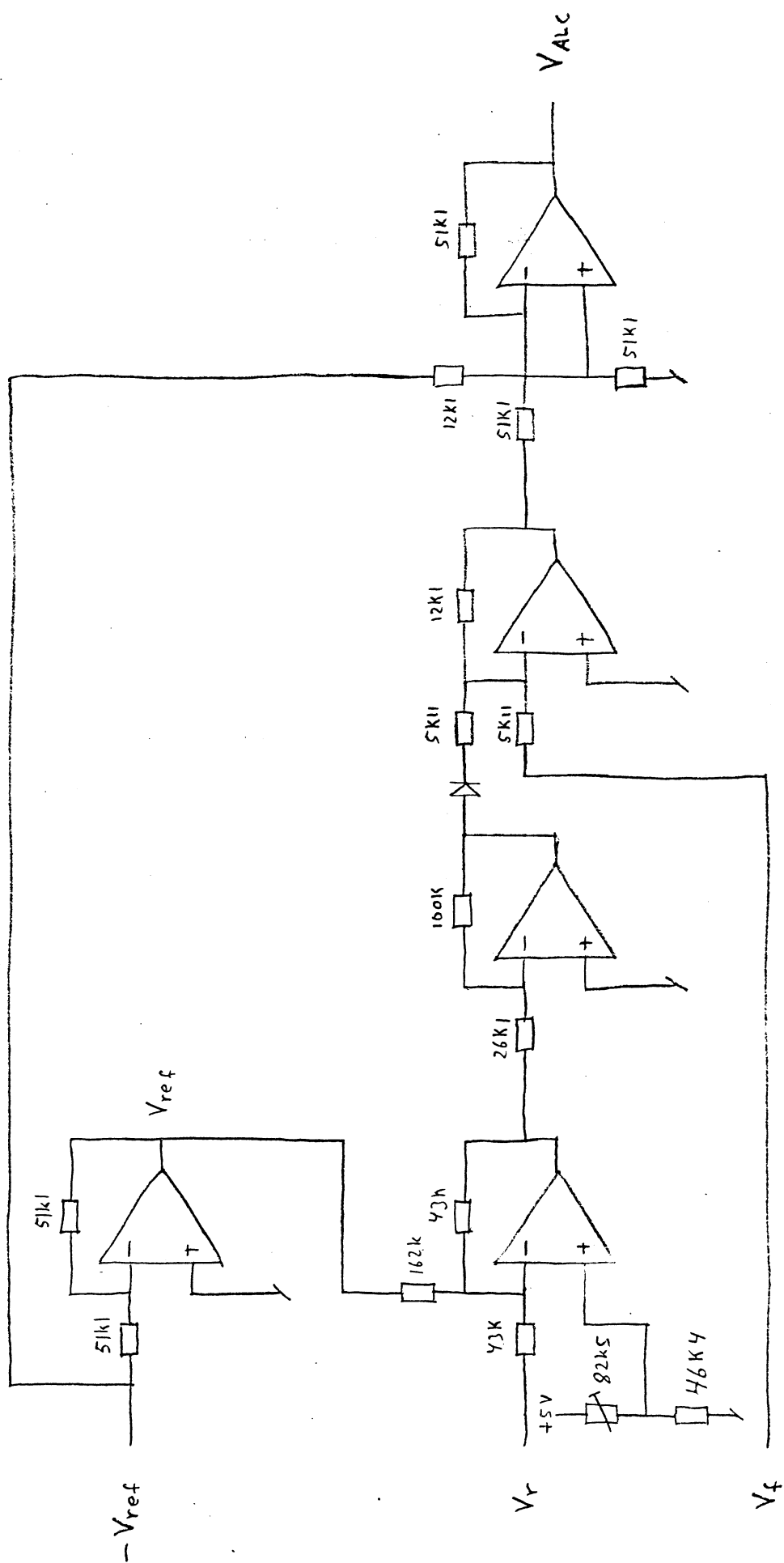
ALC LOOP

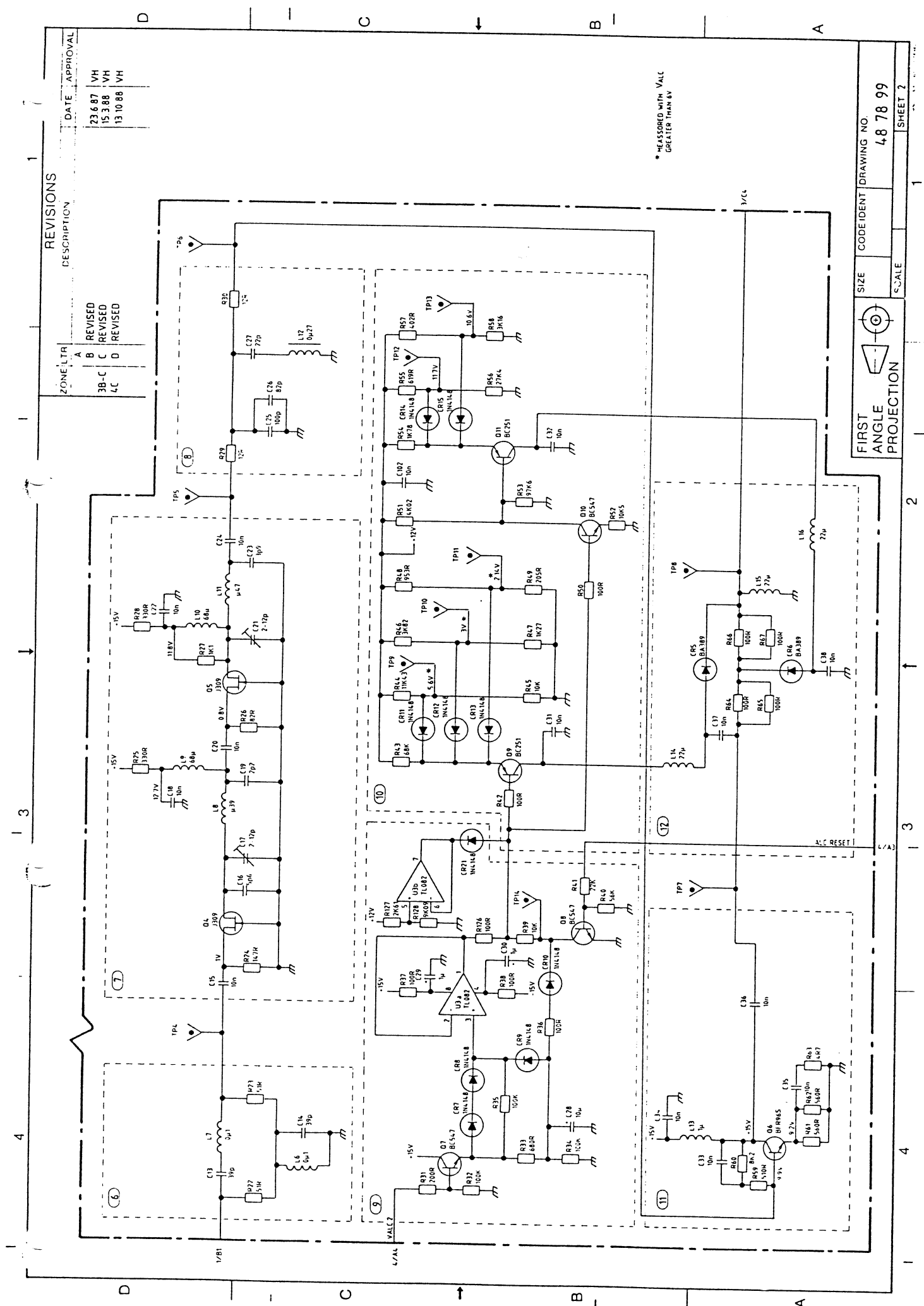


REVISIONS

ZONE LTR	DESCRIPTION	DATE	APPROVAL
A	AE05859	11/12	VH
B	AE05859	11/12	VH
D	AE07878	12/28/85	VH



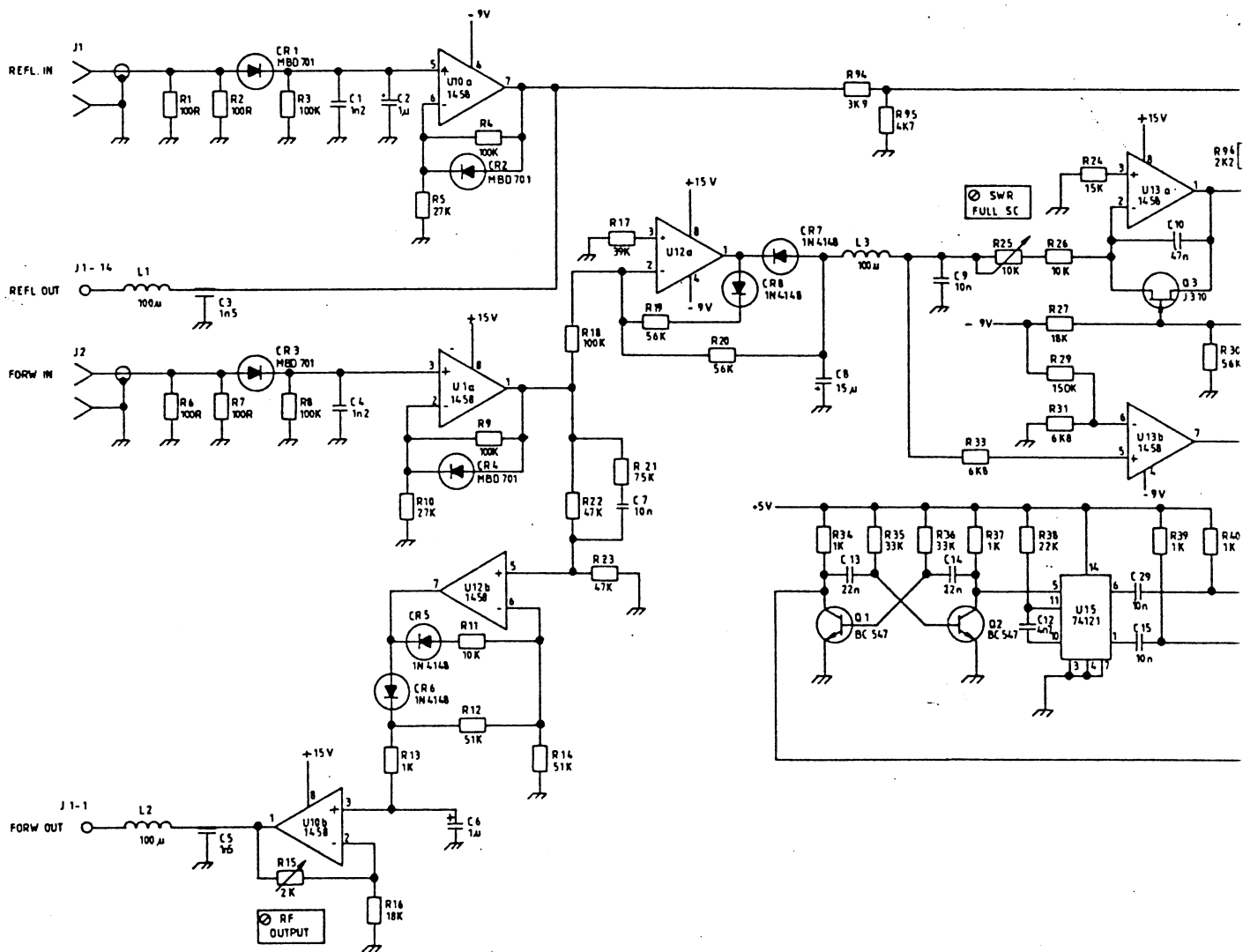




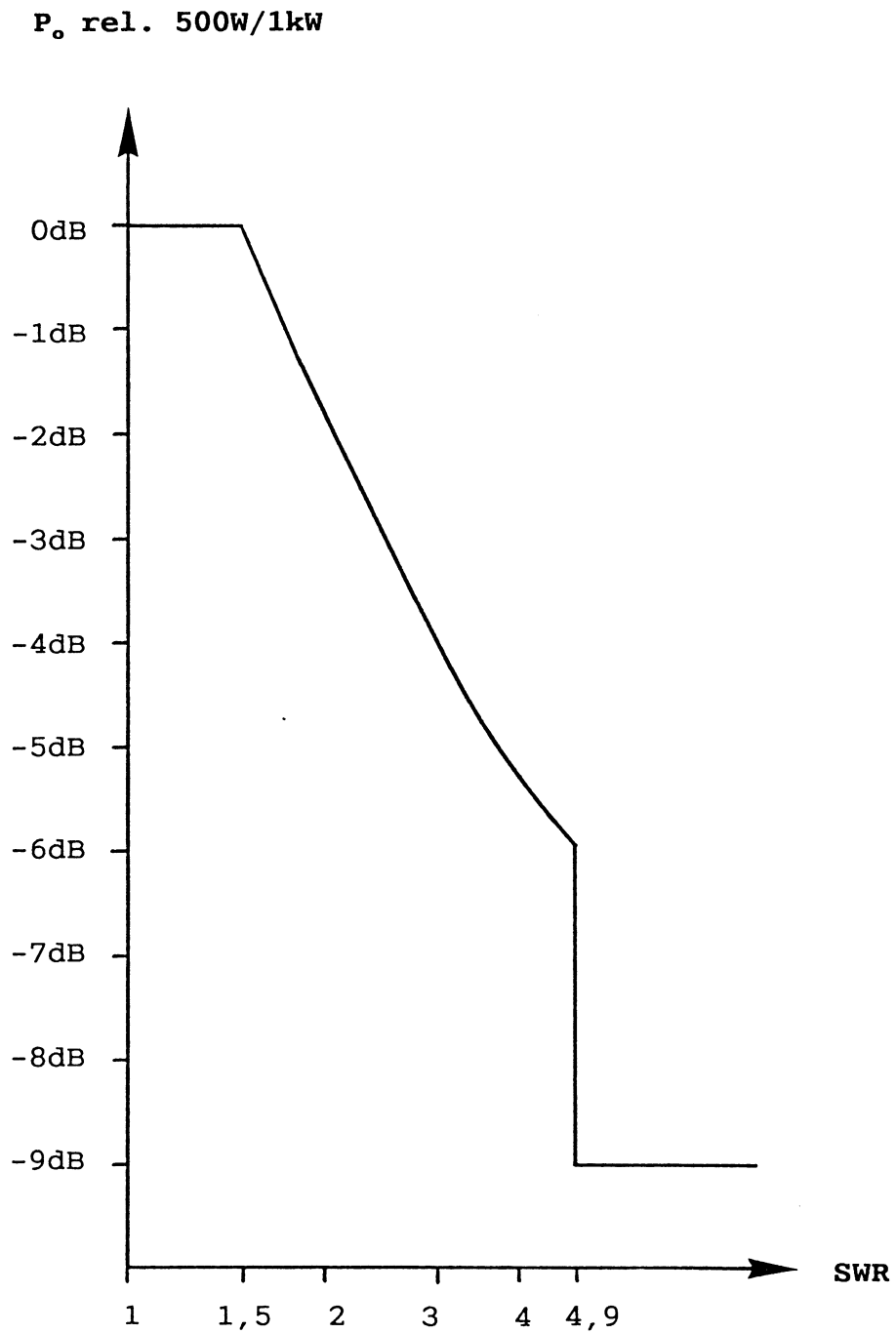
* MEASURED WITH V_{ALC}
GREATER THAN 6V

REVISIONS		DATE		APPROVAL	
DESCRIPTION					
ZONE LTR					
A	REVISED	23.6.87	VH		
B	REVISED	15.3.88	VH		
C	REVISED	13.10.88	VH		
D	REVISED				

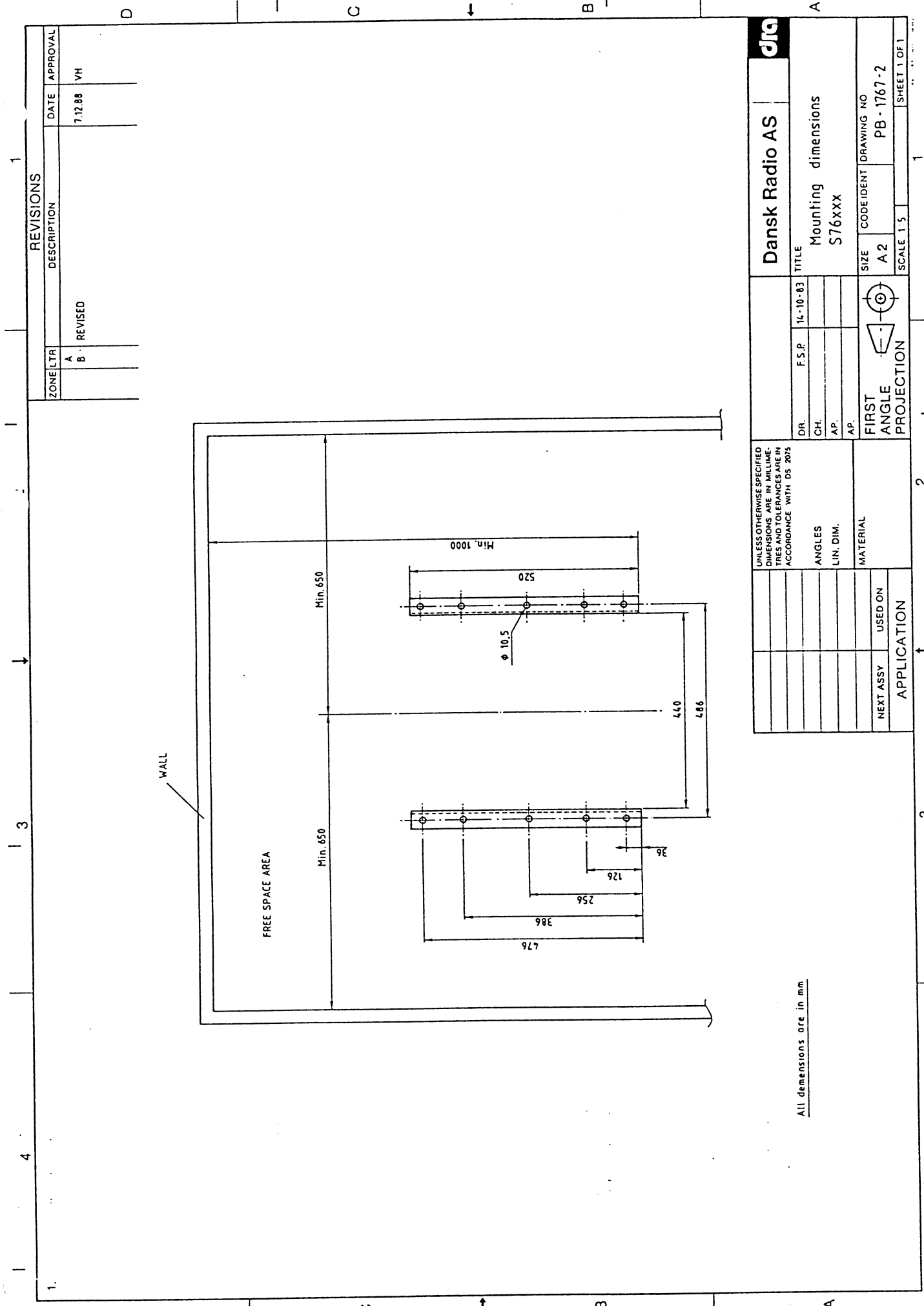
FIRST ANGLE PROJECTION		SIZE	CODE IDENT	DRAWING NO.	SHEET 2
				48 78 99	



Power Reduction vs. SWR

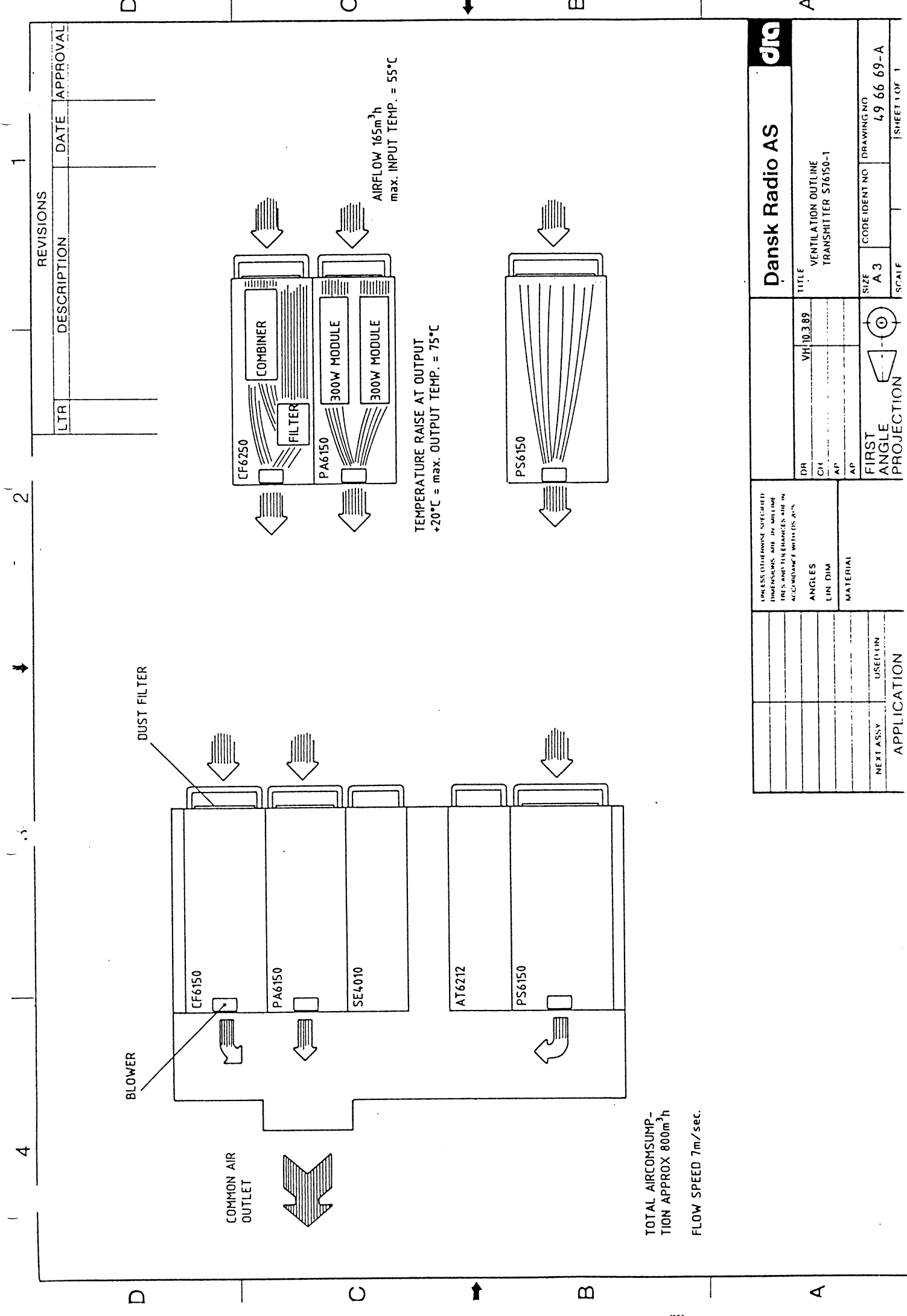


The curve is valid for transmitters with an output power of exactly 500W/1kW at SWR < 1:1,5.

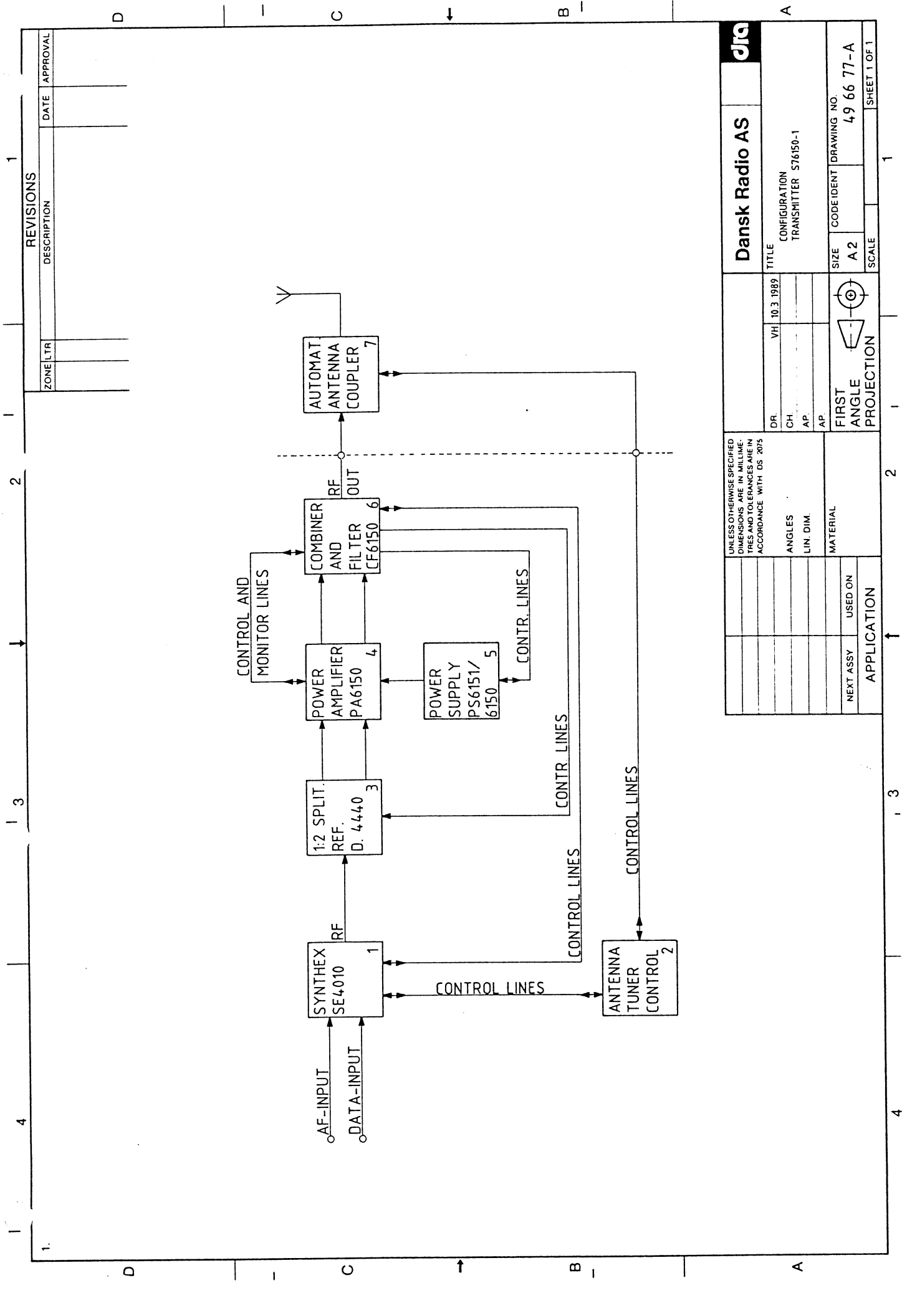


All dimensions are in mm

Dansk Radio AS		TITLE	
Mounting dimensions		S76xxx	
DR.	F.S.P.	14-10-83	
CH.			
AP.			
AP.			
FIRST ANGLE PROJECTION		SIZE	CODE IDENT
		A2	PB-1767-2
		SCALE	1:5
		SHEET 1 OF 1	

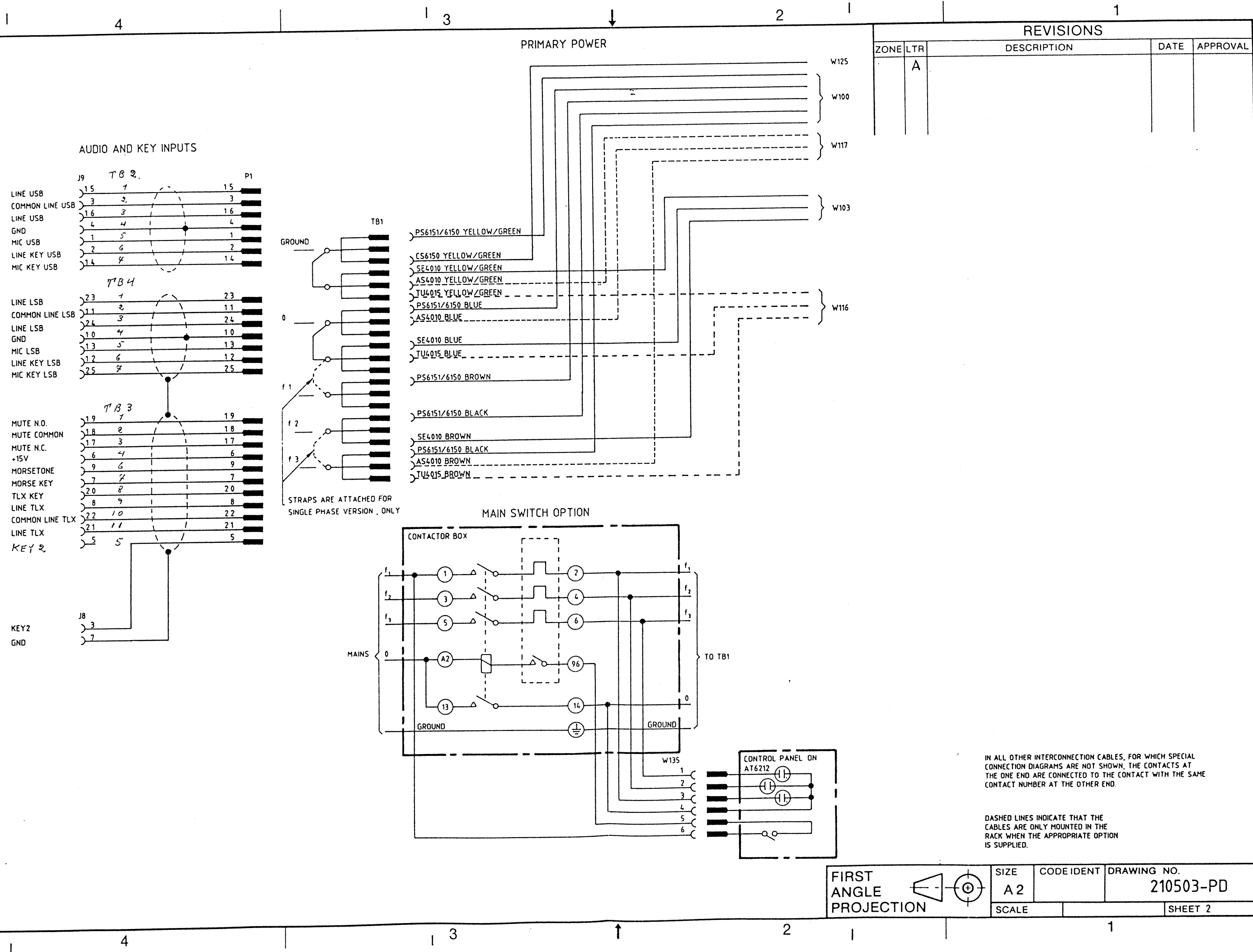


Dansk Radio AS		dra	
TITLE VENTILATION OUTLINE TRANSMITTER S76150-1		DRAWING NO 49 66 69-A	
SIZE A 3		SCALE 1	
FIRST ANGLE PROJECTION		SHEET 1 OF 1	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES ARE IN MILLIMETERS ACCORDANCE WITH EN ISO 2768		APPROVAL	
APPROVED		DATE	
DRAWN		REVISIONS	
CHECKED		DESCRIPTION	
MATERIAL		LTR	
NEXT ASSY		DATE	
USE IN		APPROVAL	
APPLICATION		DRAWING NO	

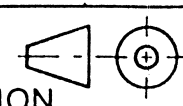


REVISIONS		
ZONE/LTR	DESCRIPTION	DATE

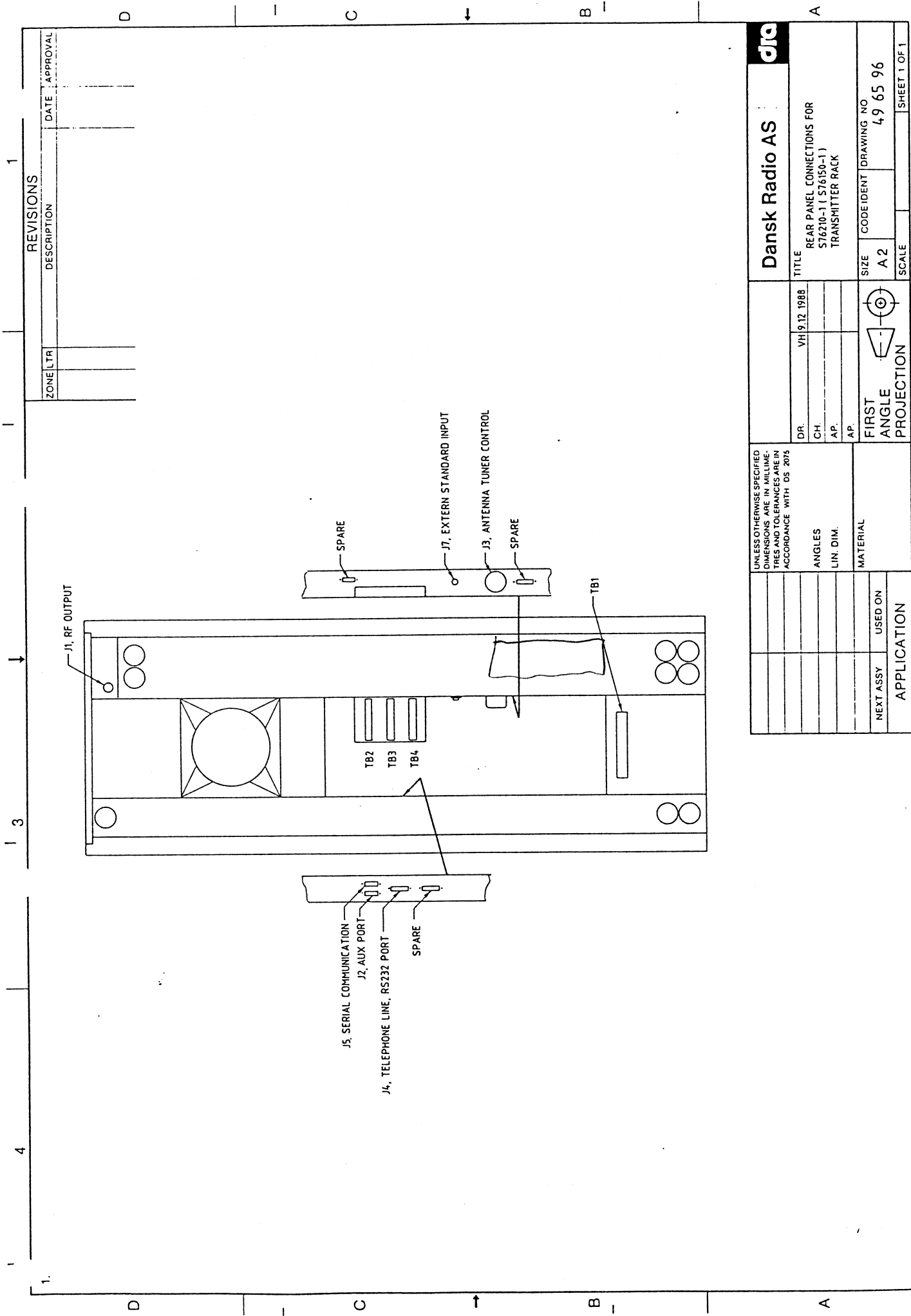
Dansk Radio AS		dra	
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE IN ACCORDANCE WITH DS 2075		TITLE	
		DR.	VH 10.3 1989
		CH.	
		AP.	
		AP.	
		FIRST ANGLE PROJECTION	
		SIZE	A2
		CODE IDENT	DRAWING NO. 49 66 77-A
		SCALE	
		SHEET 1 OF 1	



FIRST
ANGLE
PROJECTION



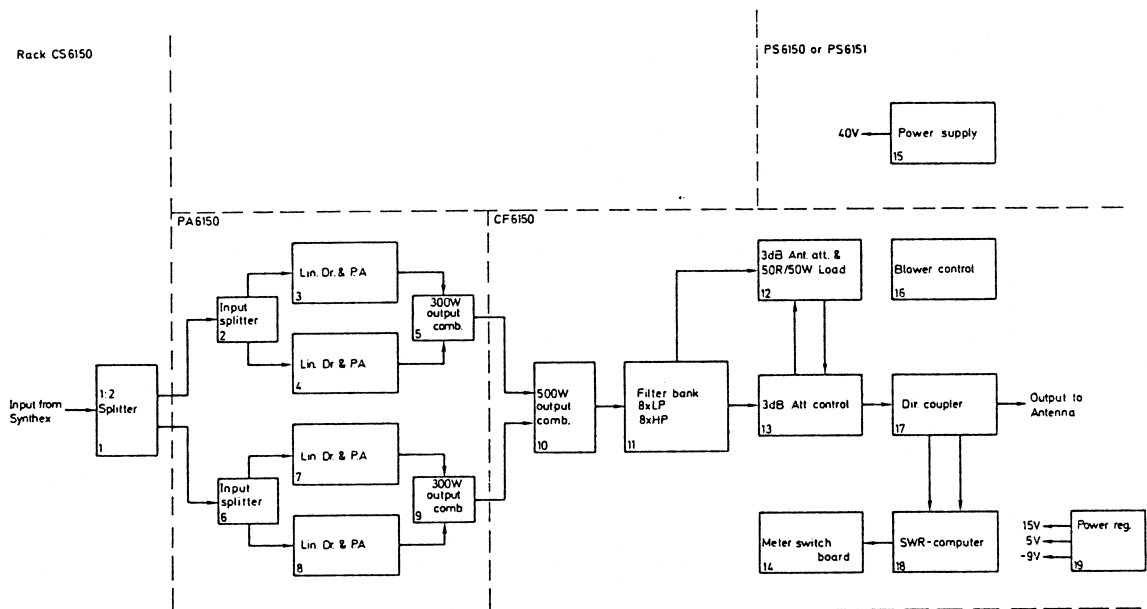
SIZE	CODE IDENT	DRAWING NO.
A 2		210503-PD
SCALE		SHEET 2



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLI- METERS AND TOLERANCES ARE IN ACCORDANCE WITH DS 2075		Dansk Radio AS		TITLE	
ANGLES LIN. DIM.		DR. VH 9.12.1988		REAR PANEL CONNECTIONS FOR S76210-1 (S76150-1) TRANSMITTER RACK	
MATERIAL		CH. AP. AP.		SIZE A2	
NEXT ASSY USED ON		FIRST ANGLE PROJECTION		CODE IDENT DRAWING NO 49 65 96	
APPLICATION		SCALE		SHEET 1 OF 1	



Block Diagram
Power Amplifier part
Ref. Designation 4471

Note 1:

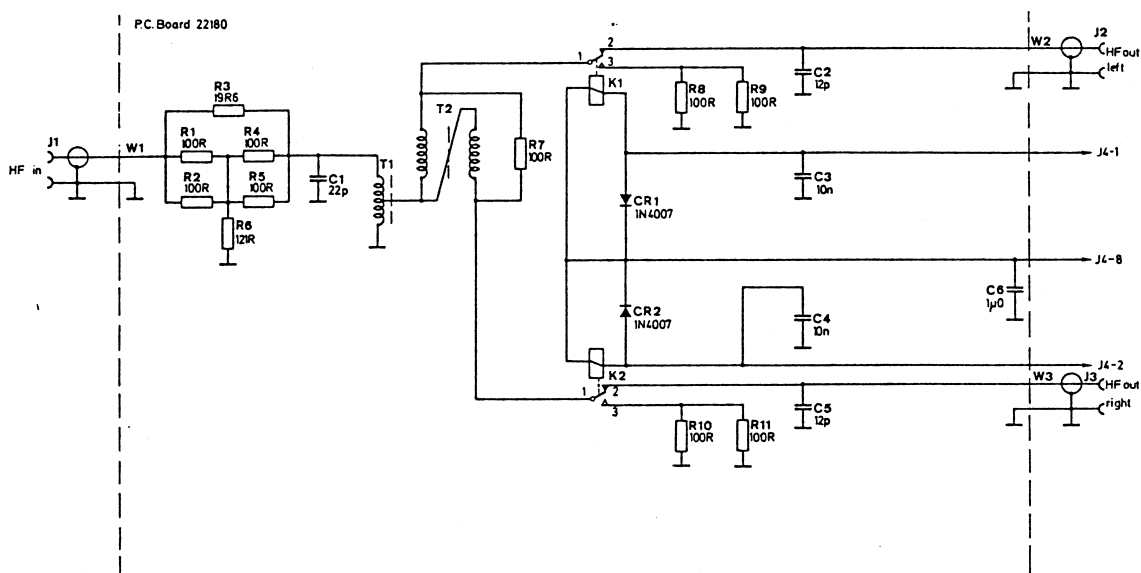
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

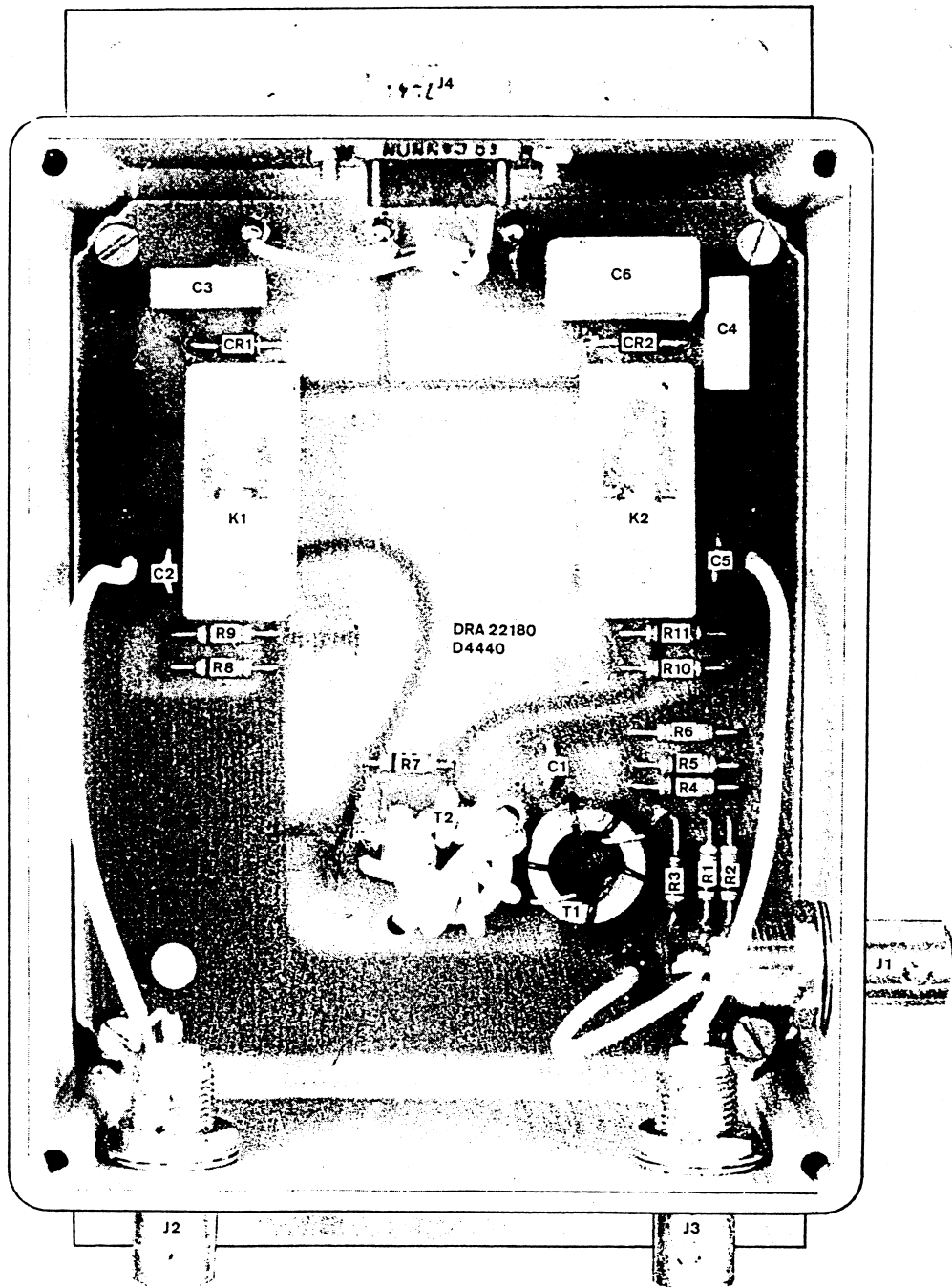
Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω , e.g. $0,47 = 0,47\Omega$, but $4R7 = 4,7\Omega$.

The capacitance units are indicated by means of the international prefixes p, n, and μ , (pF, nF, and μ F).

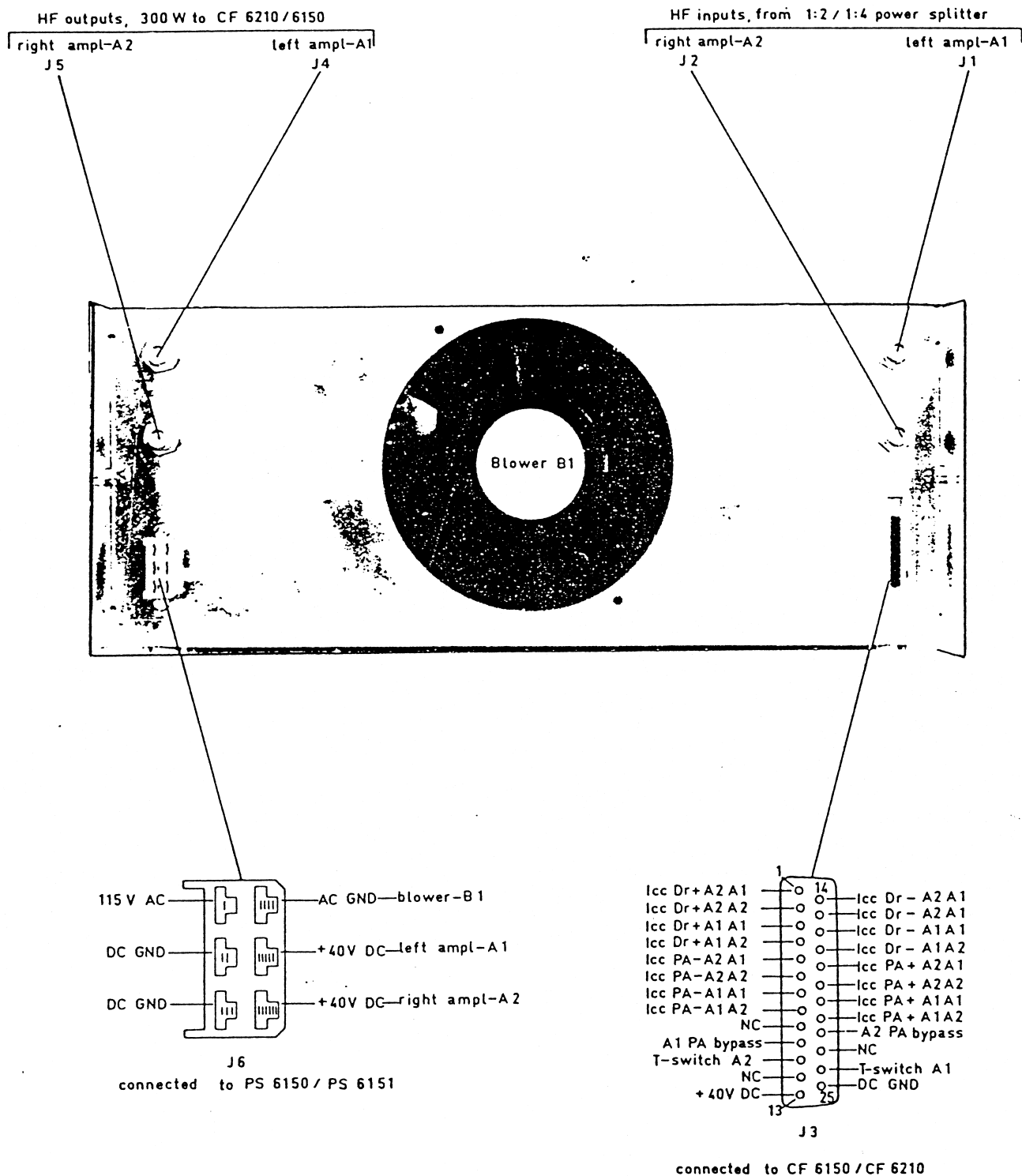
The inductance units are indicated by means of the international prefixes μ , and m, (μ H, and mH).



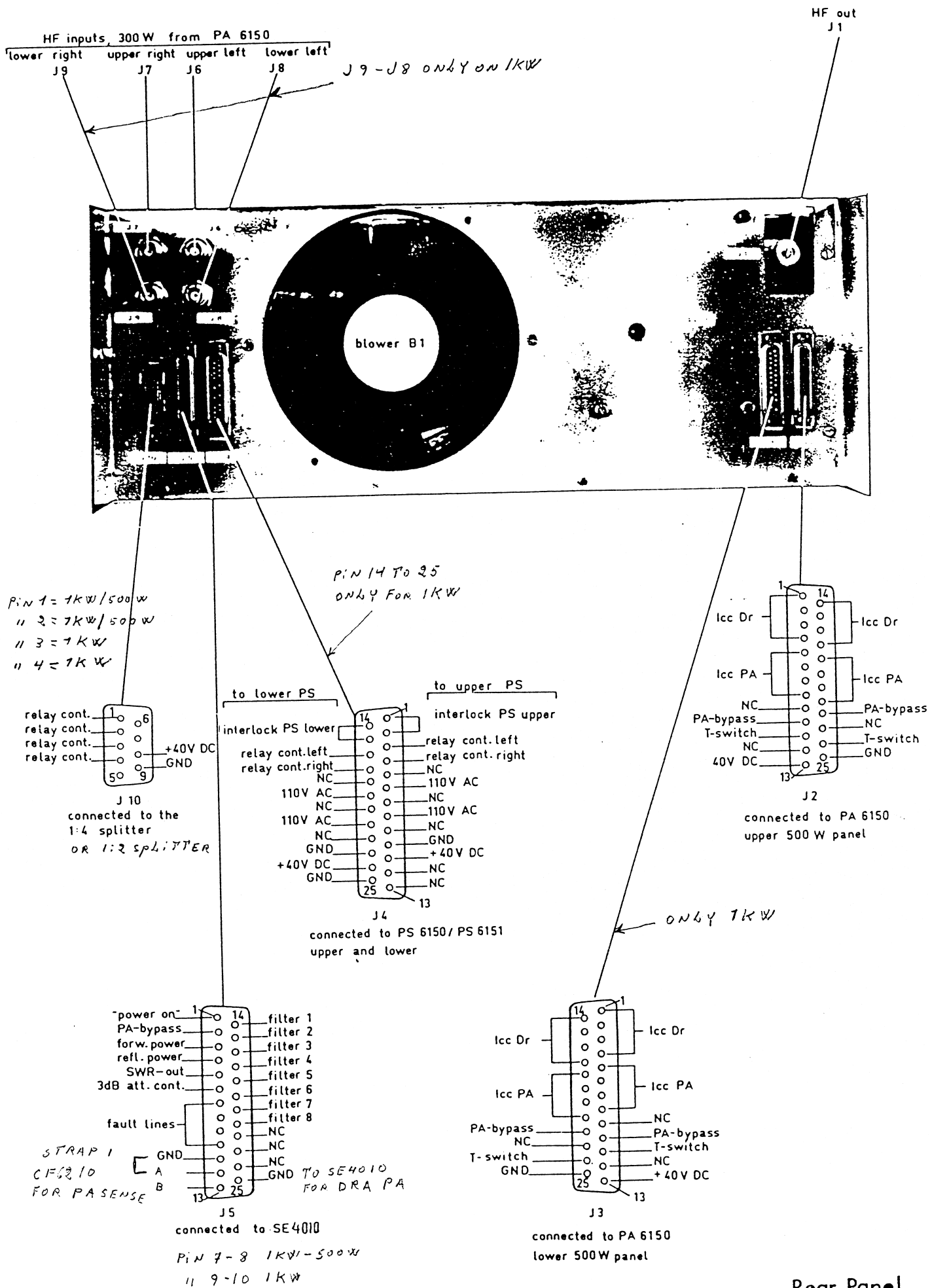


1:2 Splitter
 Ref. Desig. 4440
 Component Location

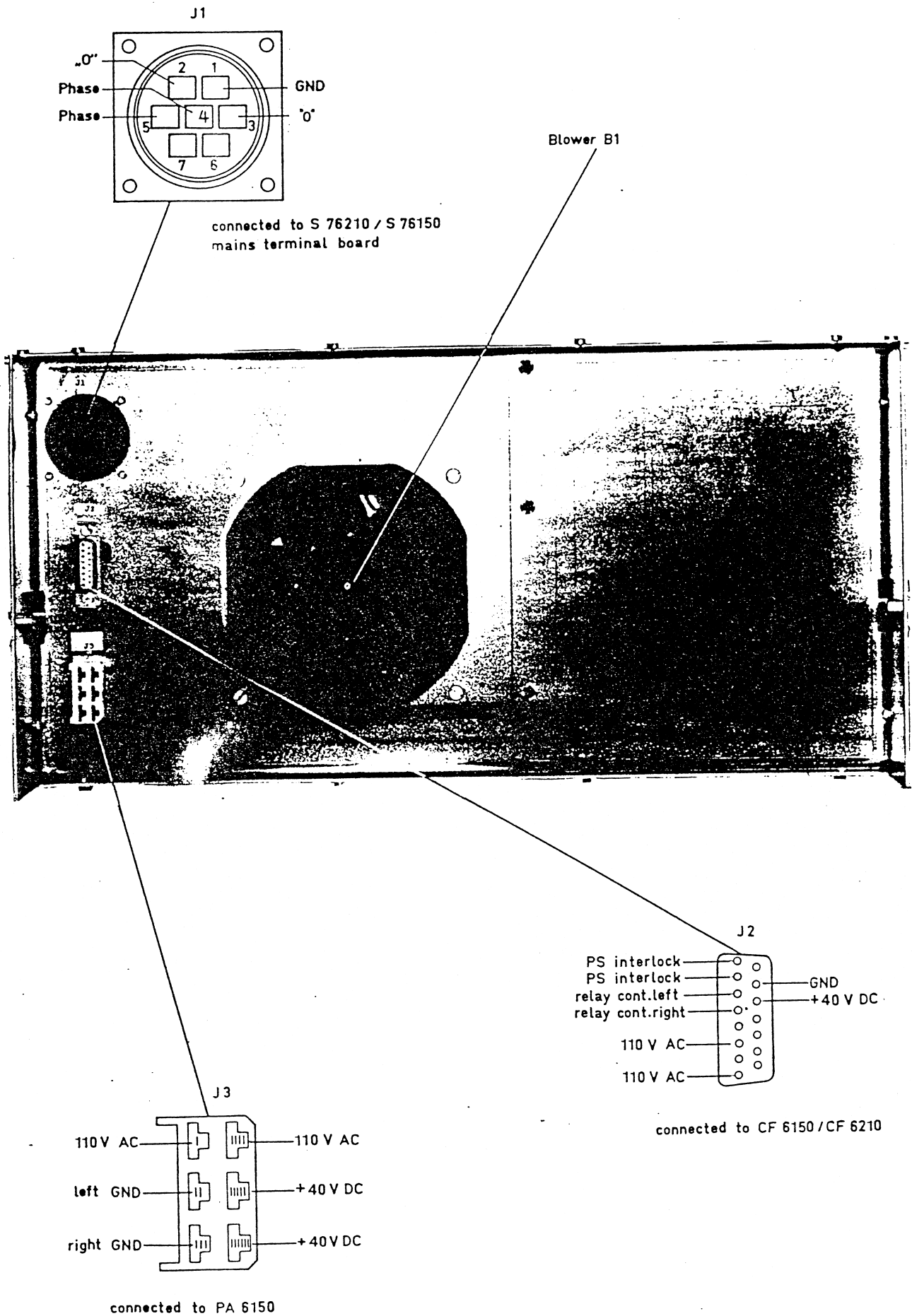
3.2. Rear Panel



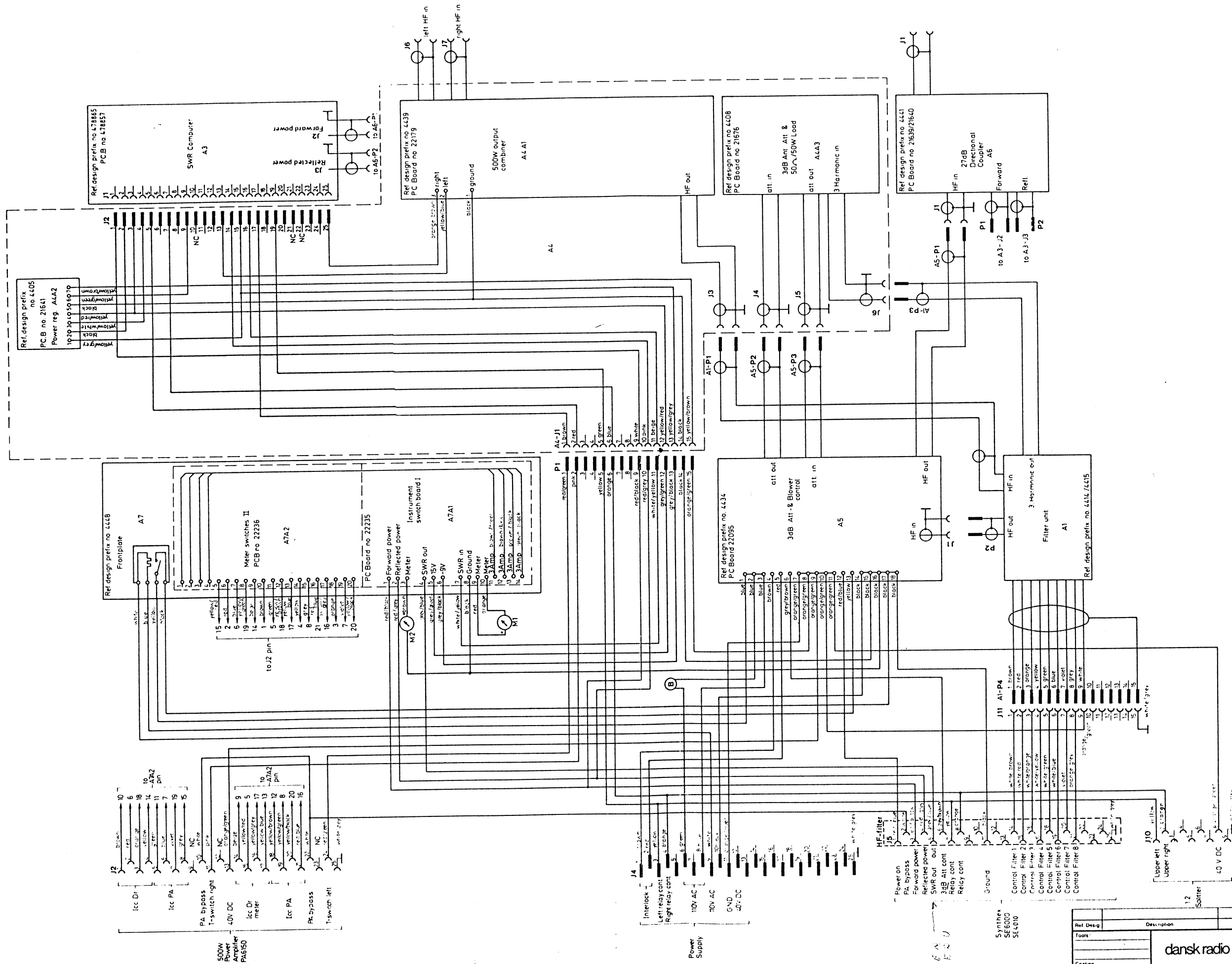
Rear view, 500-W PA Panel
Ref. Designation 4416



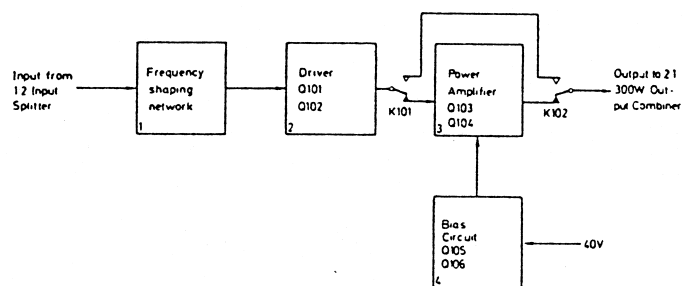
Rear Panel
 Ref. Desig. 4418



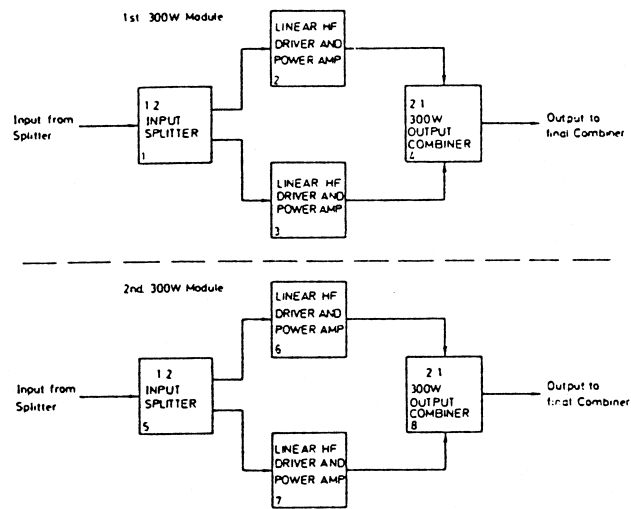
Rear Panel
Ref. Desig. 4481



Ref. Desig.	Description	Specification	Qty	Ref. M.	DNA code
SE6000	500W Combination and Filter Unit				
SE4010					
dansek radio aktieselskab					
500W Combination and Filter Unit					
CF 6150 -01					
4824					
Superseded by					



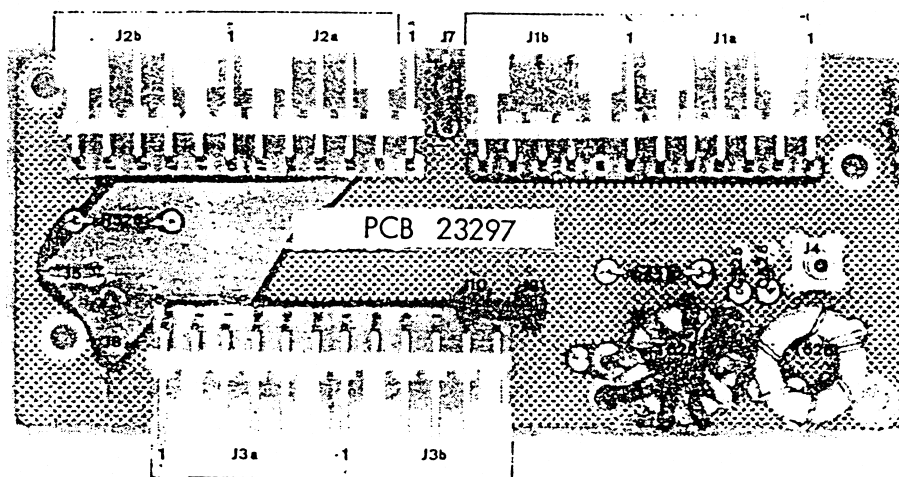
Block Diagram 150-W Power Amplifier



Block Diagram 500-W PA Panel

Ref. Designation 4445





Input Splitter

Ref. Desig. 4809

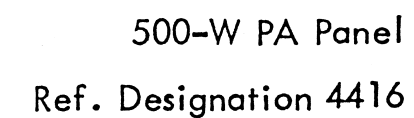
Component Location

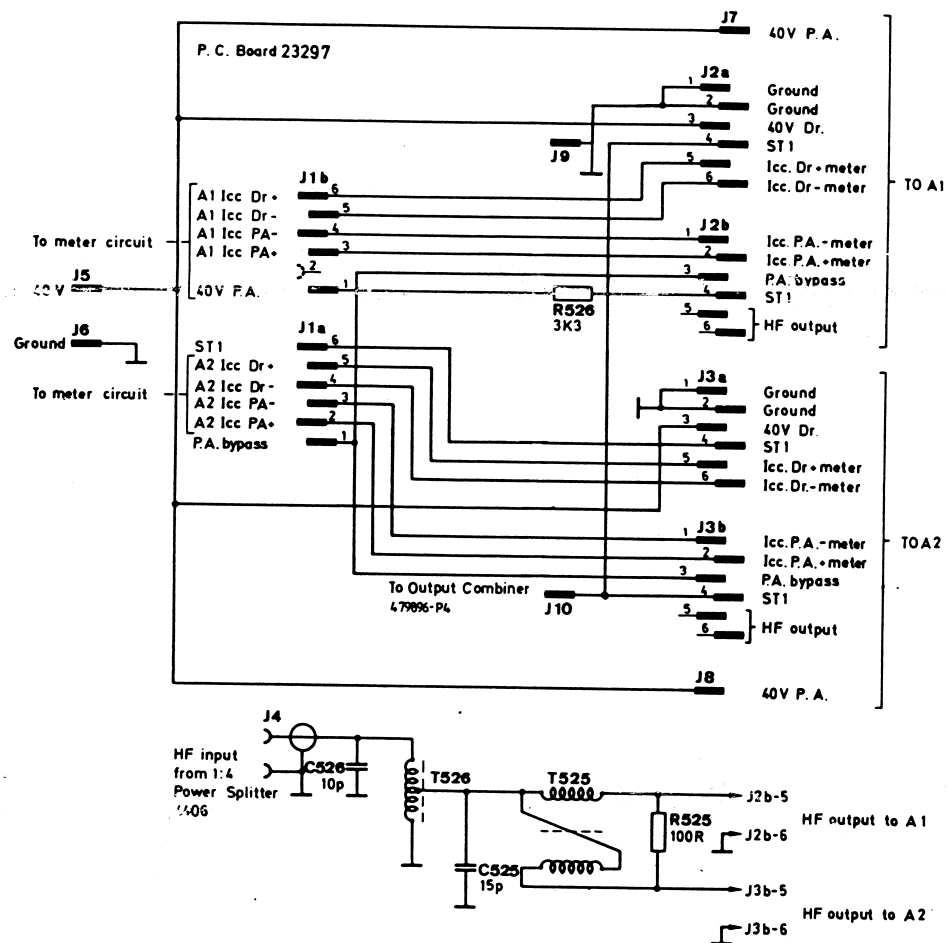
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0.47 = 0.47Ω, but 4R7 = 4.7Ω.

The capacitance units are indicated by means of the international prefixes p, n, and μ , (pF, nF, and μ F).

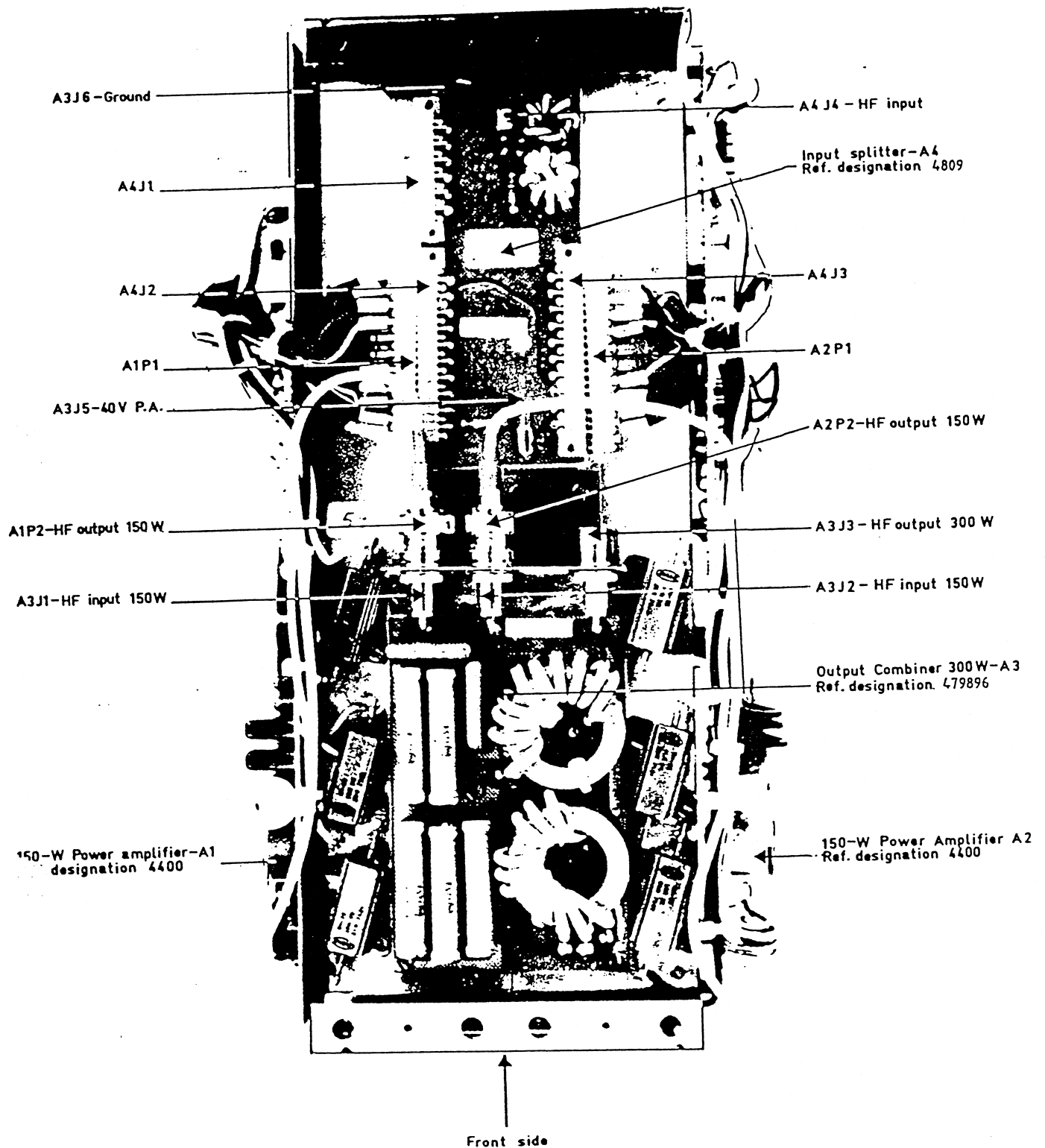
The inductance units are indicated by means of the international prefixes μ , and m , (μH , and mH).



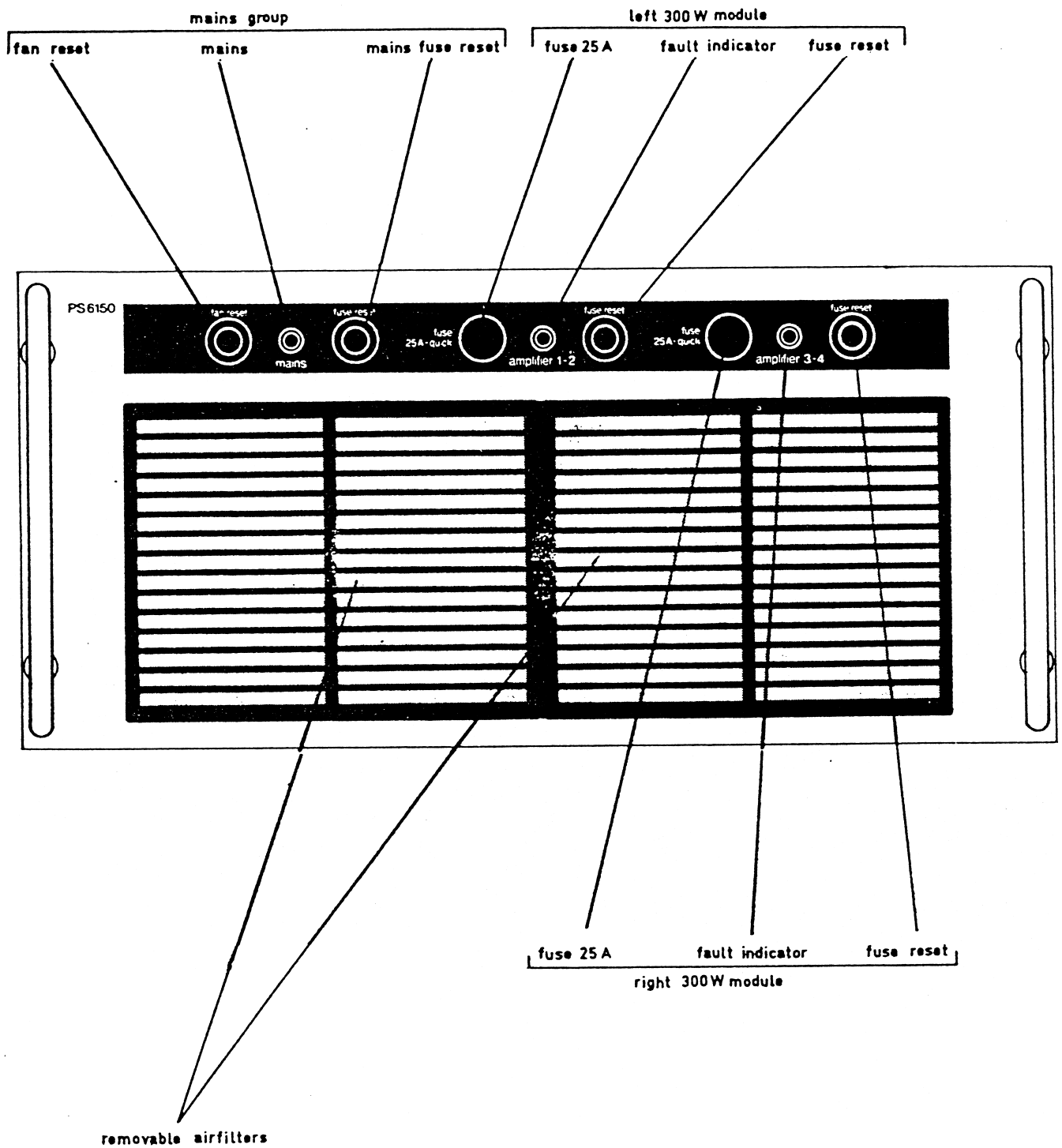


INPUT SPLITTER

(Ref. Desig. 4809)



Top View, 300-W Amplifier Unit
Ref. Designation 4478



Front Panel
Ref. Desig. 4481

Note 1:

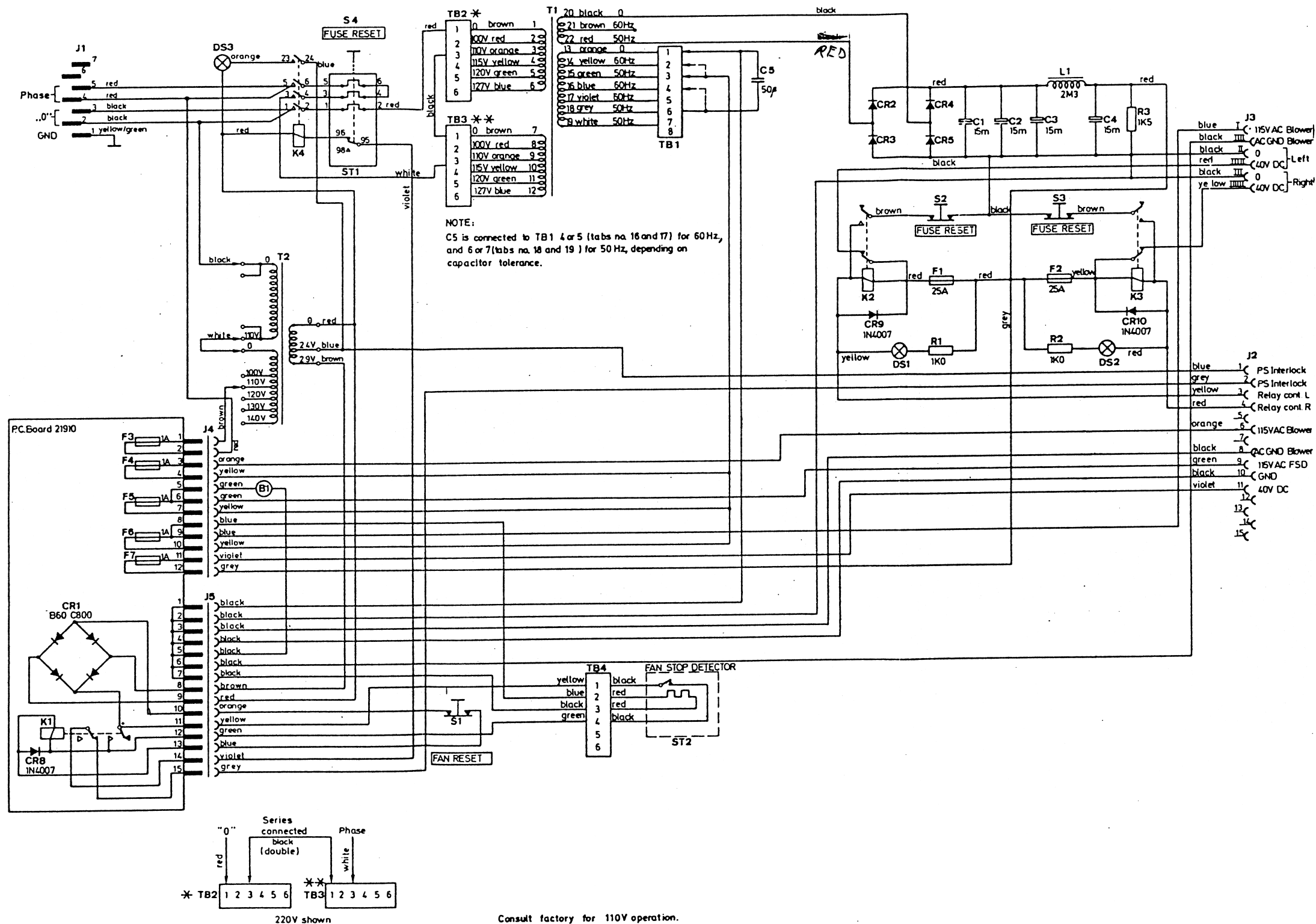
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.).

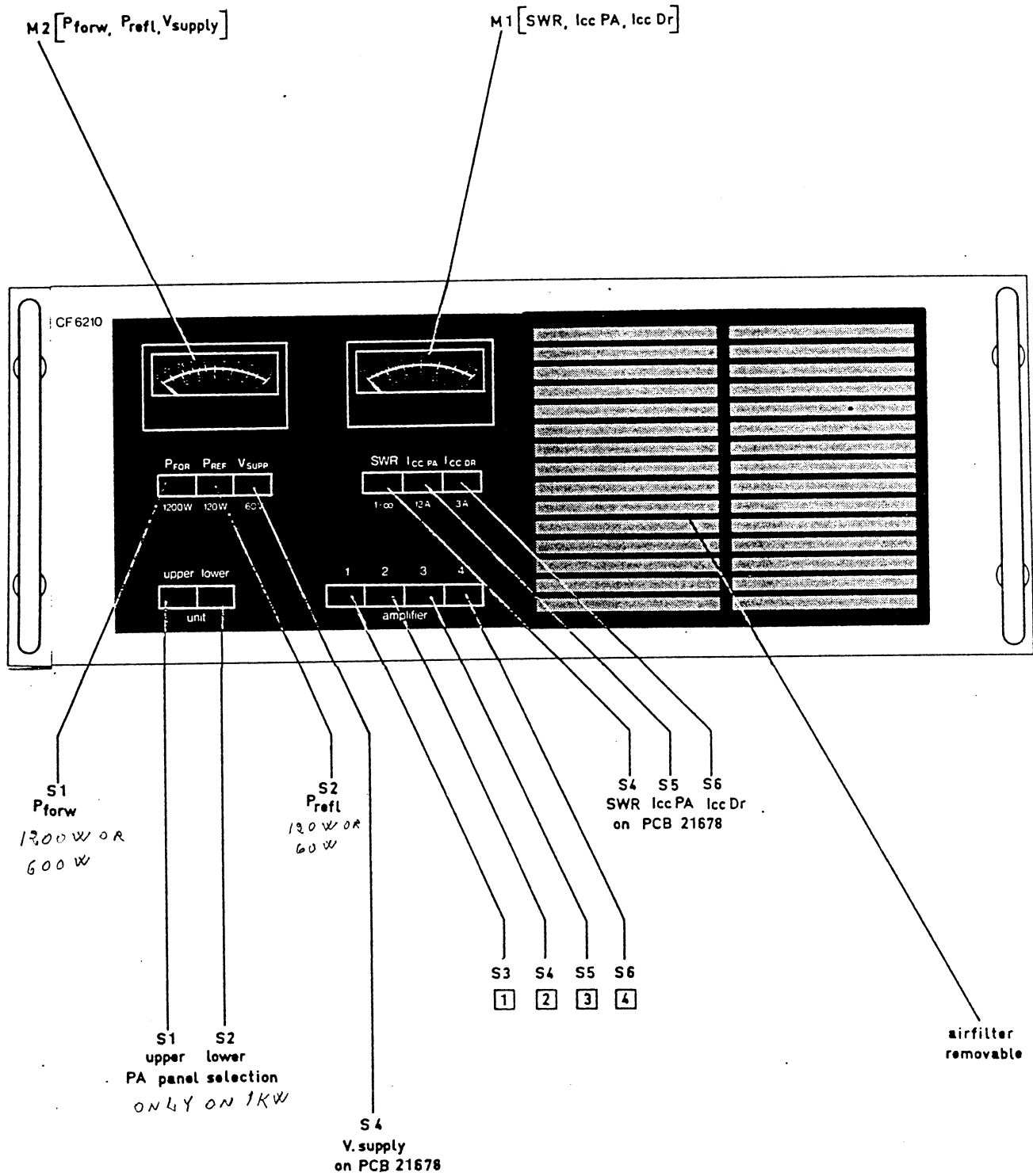
Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0.47 = 0.47Ω, but 4R7 = 4.7Ω.

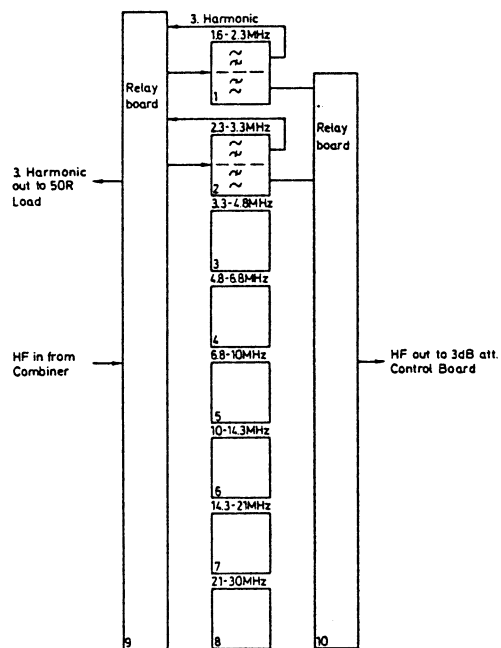
The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).



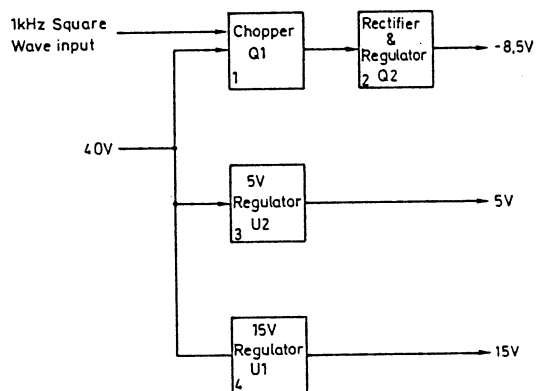


Front Panel
Ref. Desig. 4410

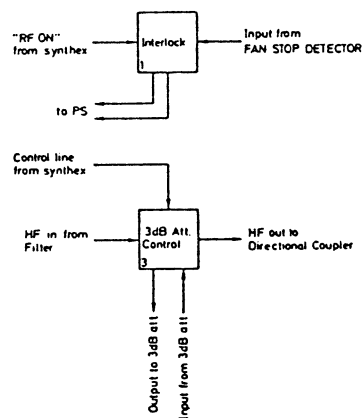


Block Diagram Filter Bank

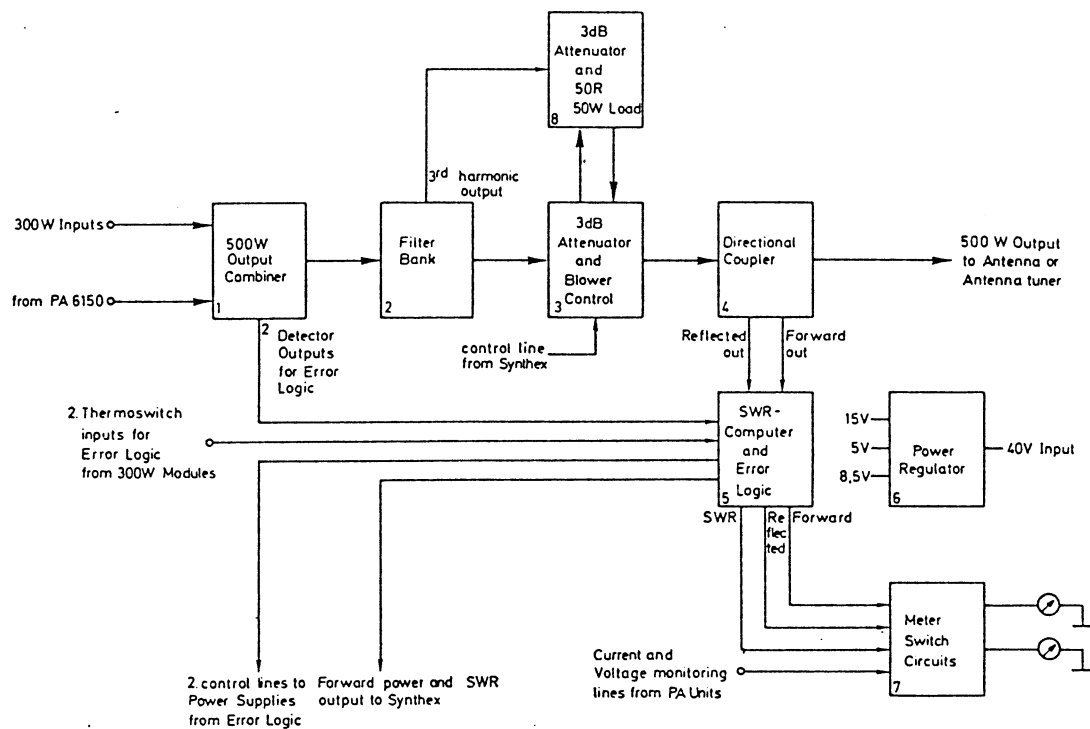
Ref. Designation 4452



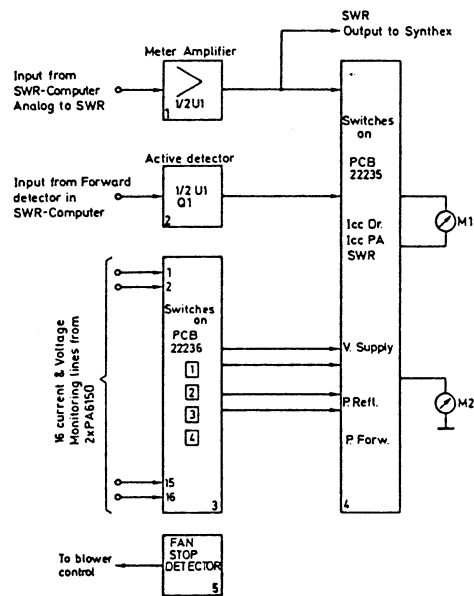
Block Diagram Power Regulator
Ref. Designation 4453



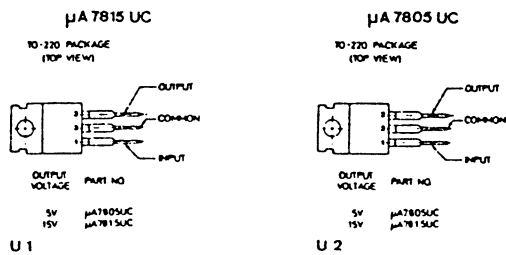
Block Diagram 3-dB Attenuator and Blower Control



Block Diagram Combination and Filter Panel



Block Diagram Front Panel
Ref. Designation 4470



Note 1:

Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

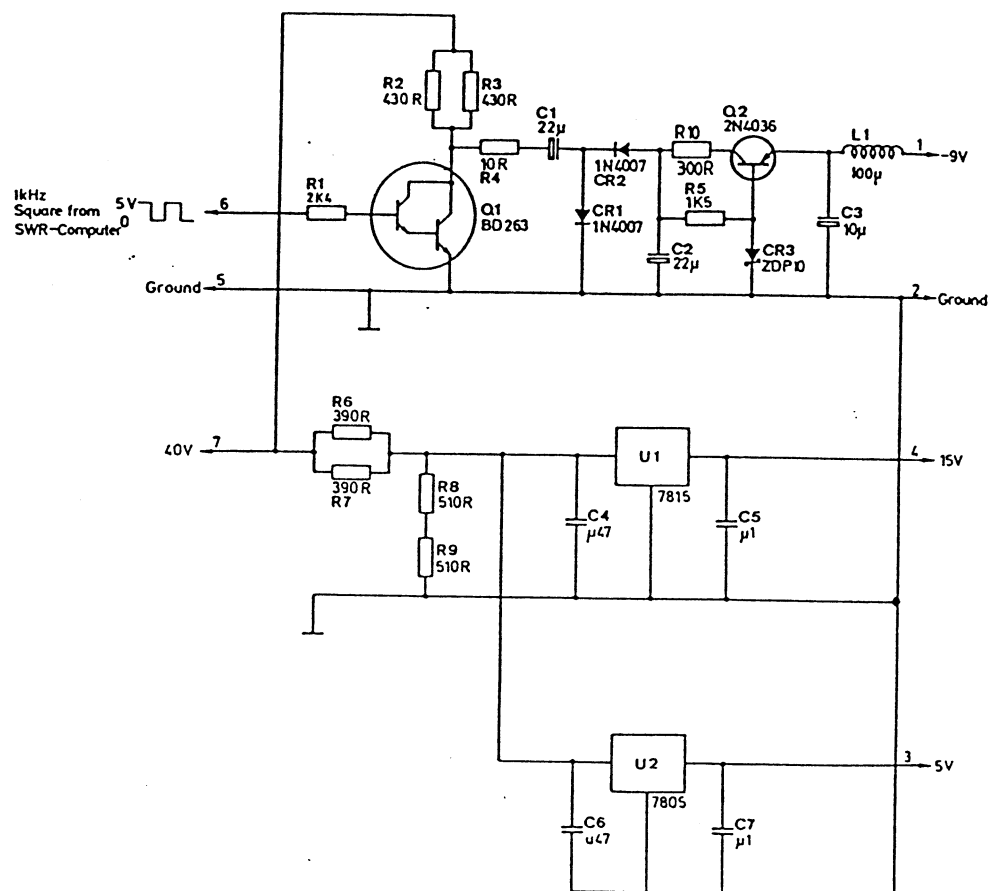
Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0.47 = 0.47Ω, but 4R7 = 4.7Ω.

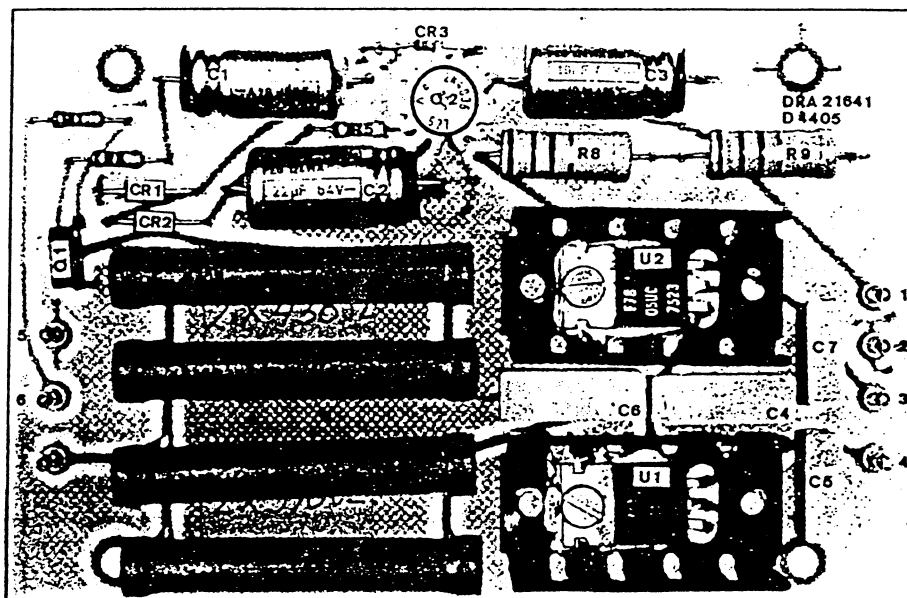
The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).

P. C. Board 21641



Power Regulator



Power Regulator
 Ref. Desig. 4405
 Component Location

Note 1:

Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

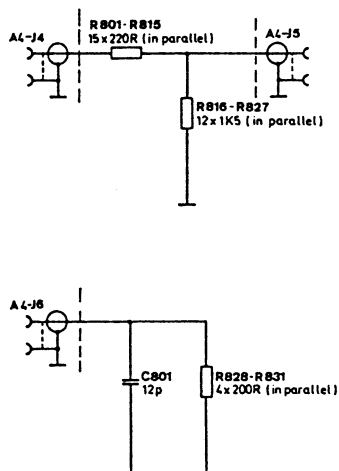
Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1 Ω , e.g. 0,47 = 0,47 Ω , but 4R7 = 4,7 Ω .

The capacitance units are indicated by means of the International prefixes p, n, and μ , (pF, nF, and μ F).

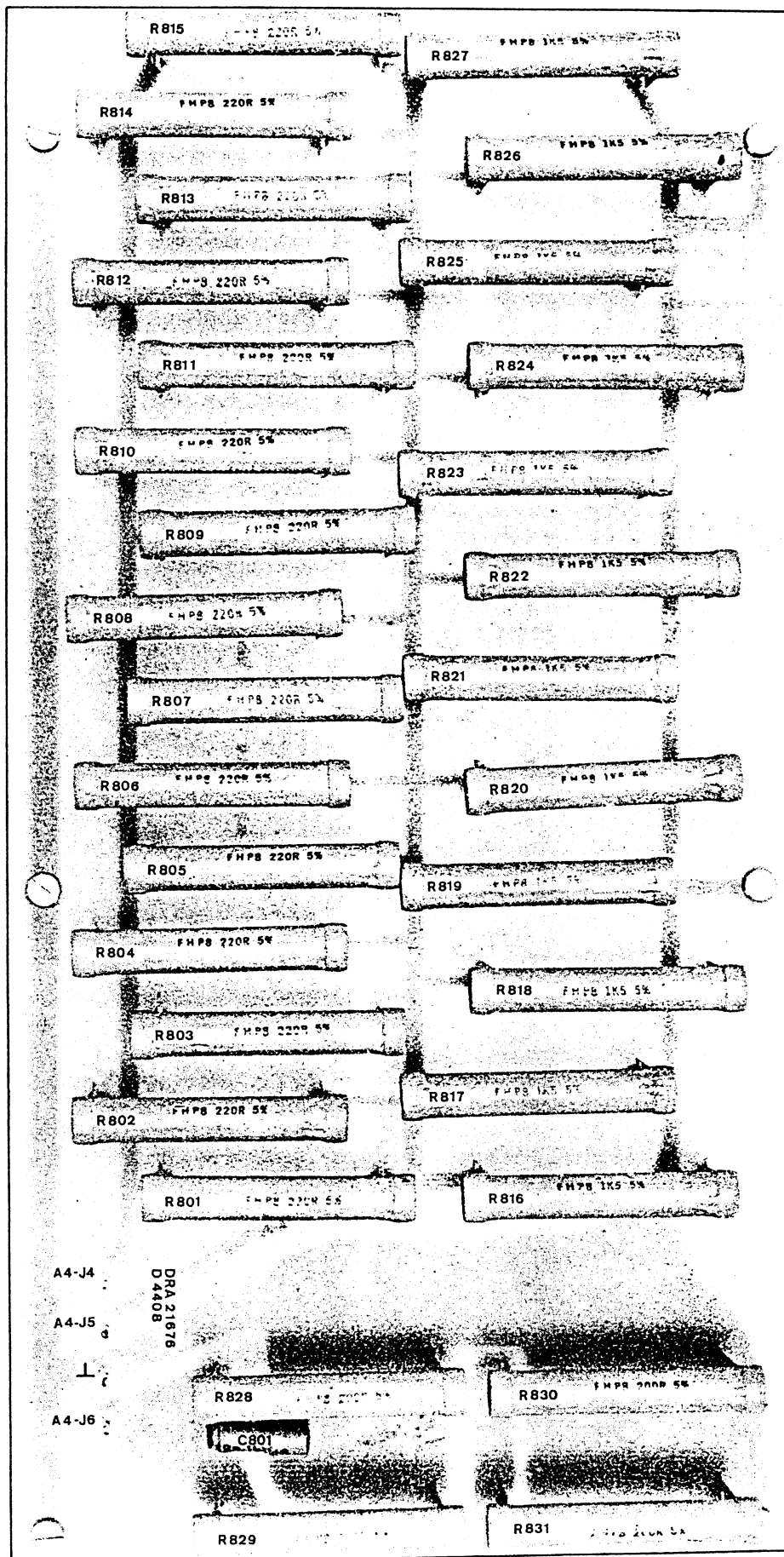
The inductance units are indicated by means of the International prefixes μ , and m, (μ H, and mH).

P. C. Board 21676



3-dB Attenuator and 50 ohm/ 50-W Load

Ref. Designation 4408



dB Attenuator and 50-Ω/50-W Load.

Ref. Desig. 4408.

Component Location.

Note 1:

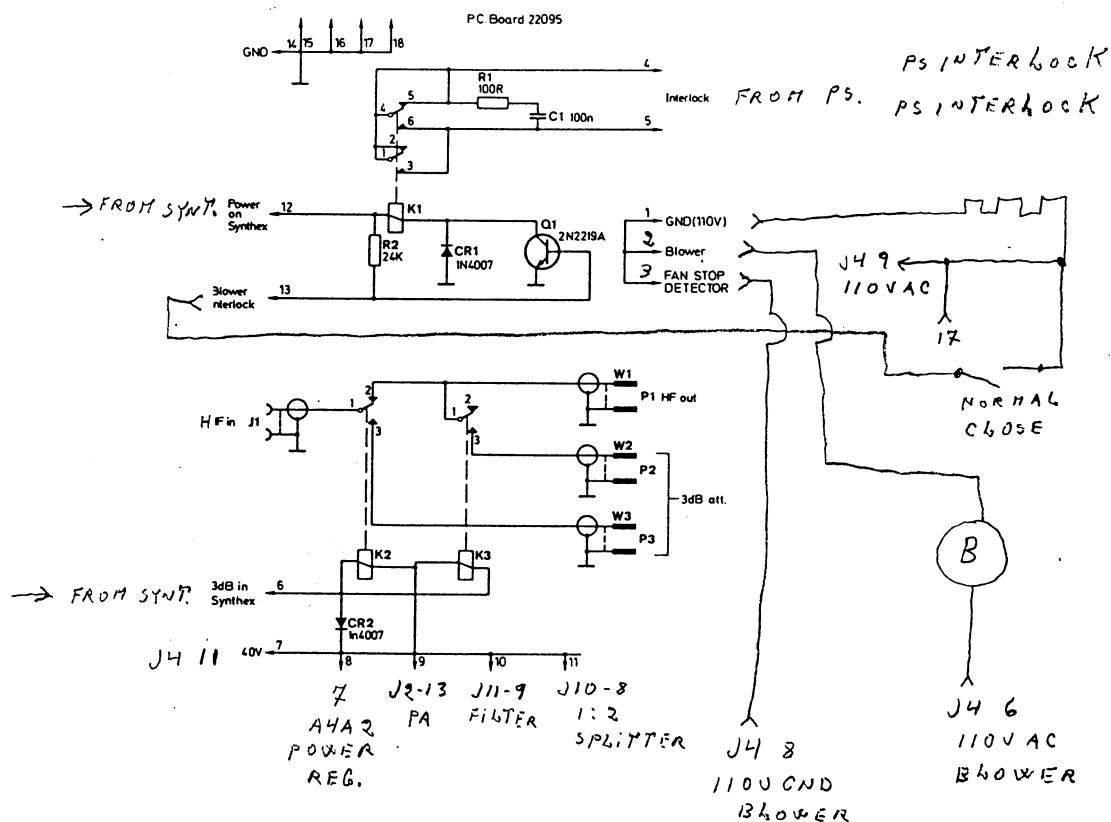
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0,47 = 0,47Ω, but 4R7 = 4,7Ω.

The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).



3-dB Attenuator and Blower Control

Note 1:

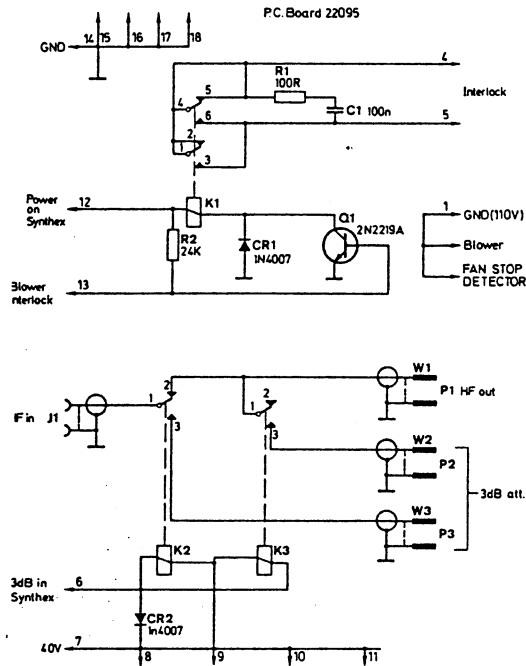
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω , e.g. $0,47 = 0,47\Omega$, but $4R7 = 4,7\Omega$.

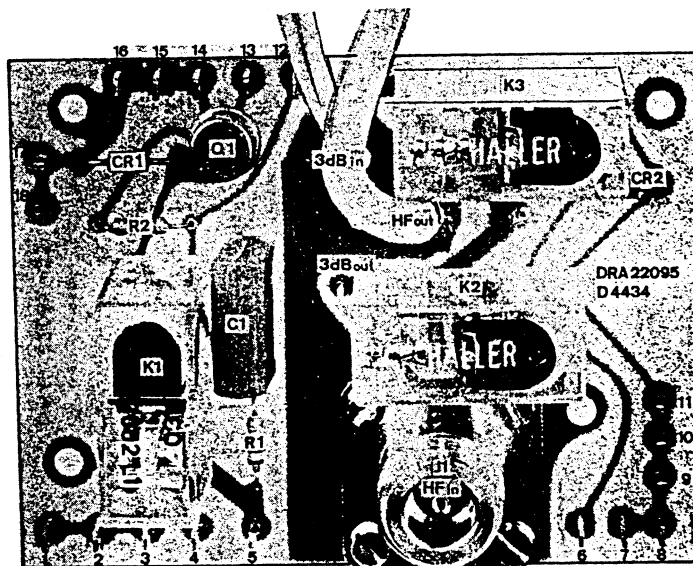
The capacitance units are indicated by means of the international prefixes p, n, and μ , (pF, nF, and μ F).

The inductance units are indicated by means of the international prefixes μ , and m, (μ H, and mH).



3-dB Attenuator and Blower Control

Ref. Designation 4434



-3-dB Attenuator
 and Blower Control
 Ref. Desig. 4434
 Component Location

Note 1:

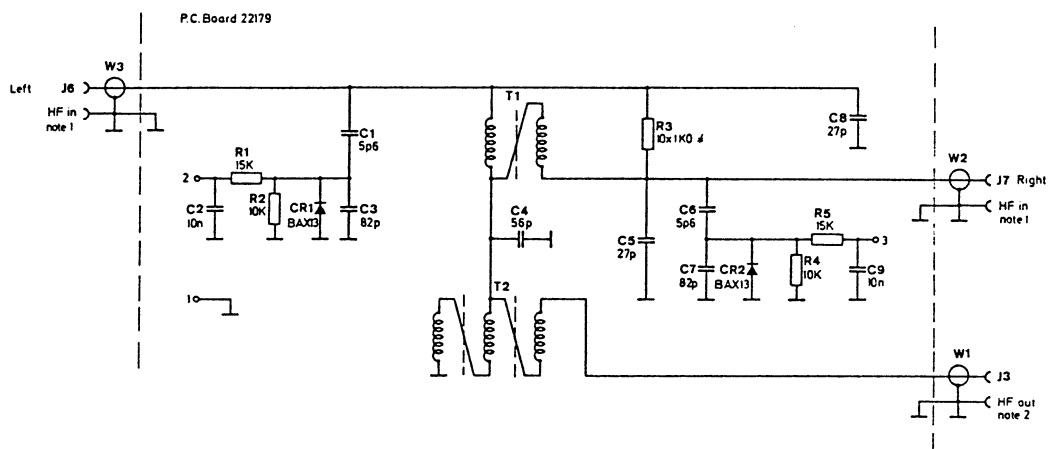
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0,47 = 0,47Ω, but 4R7 = 4,7Ω.

The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

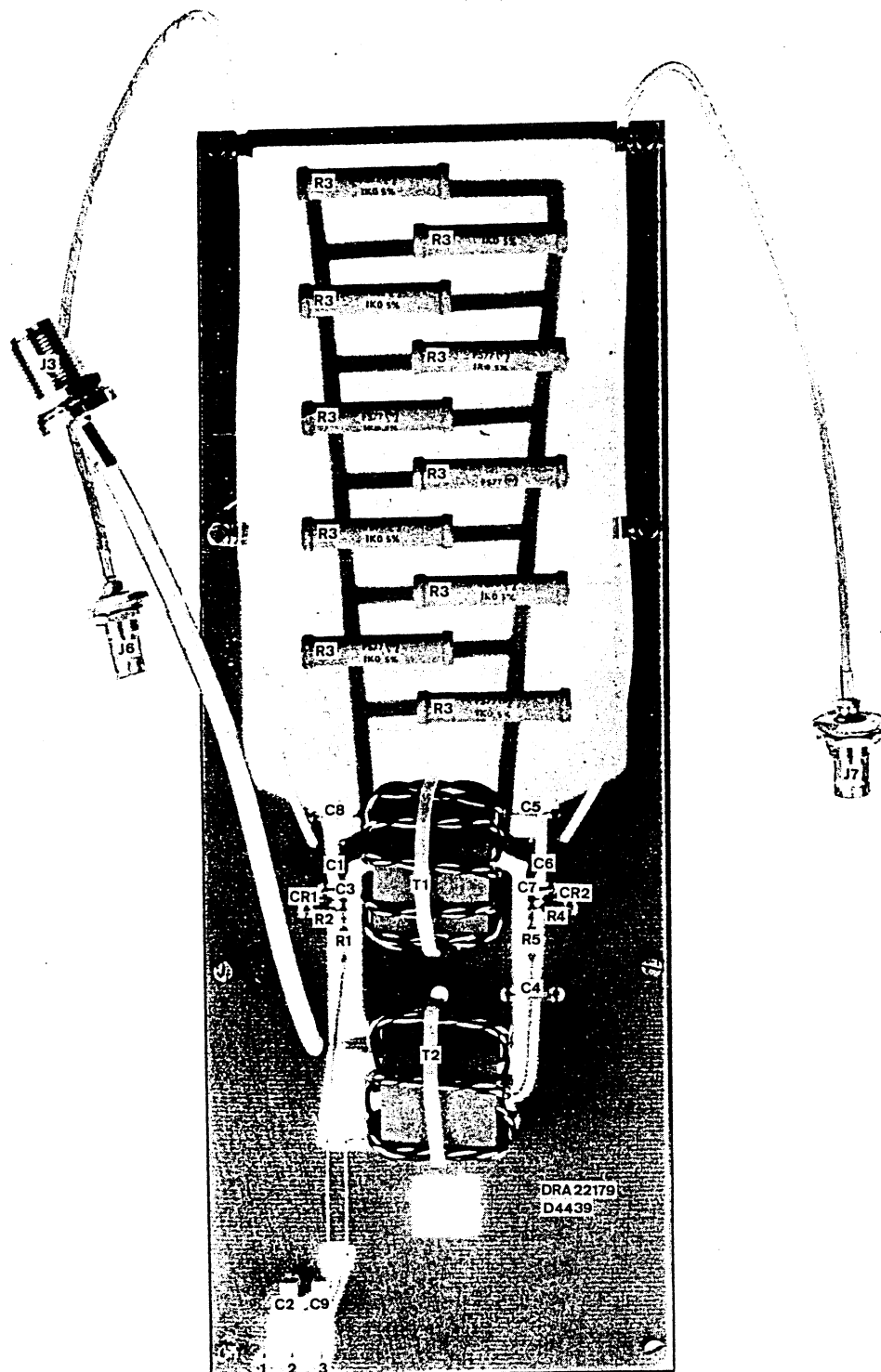
The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).



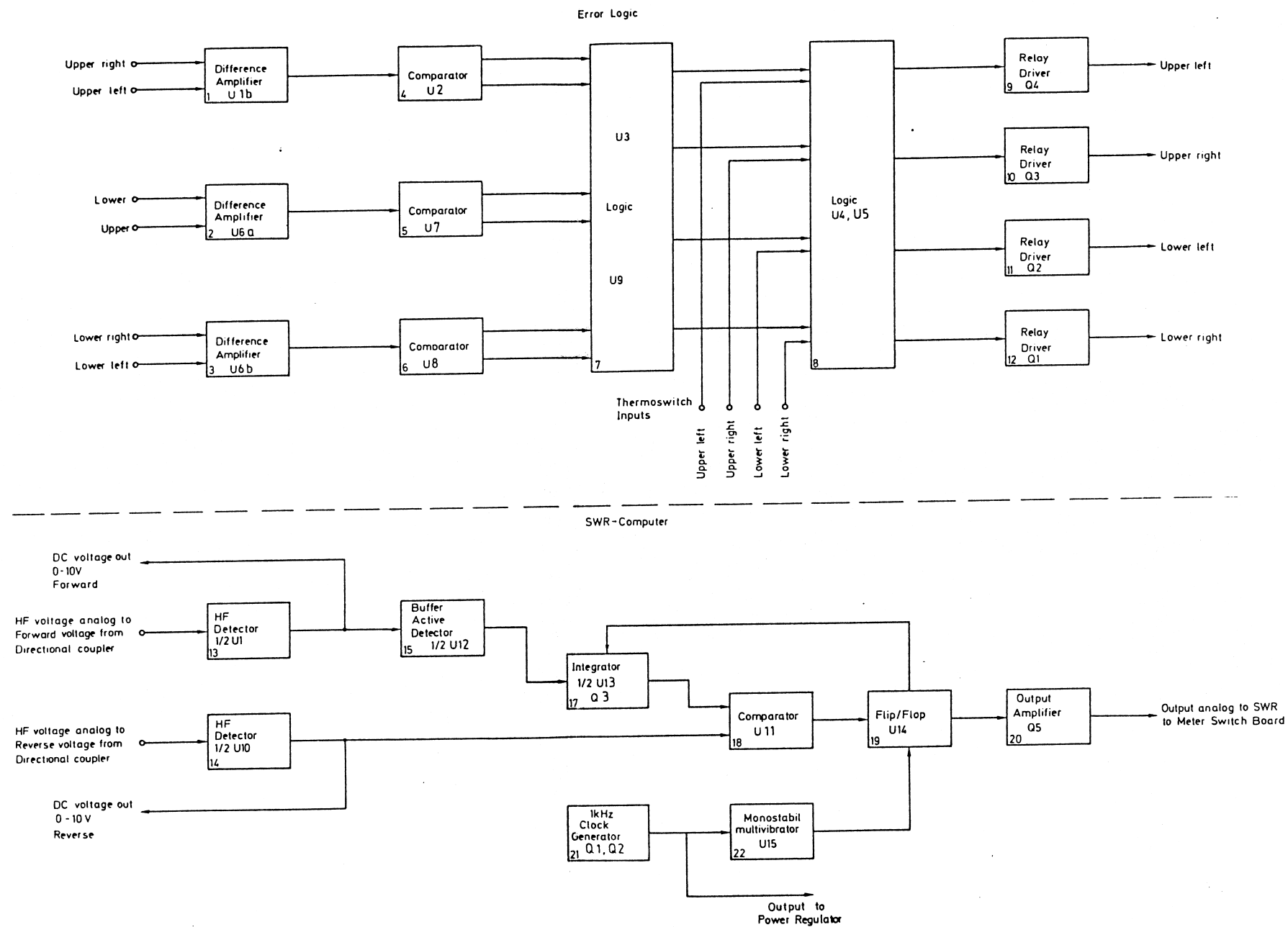
note 1 : J6, J7 are mounted on the rear of CF 6150
note 2 : J3 is mounted on the Combiner Channel

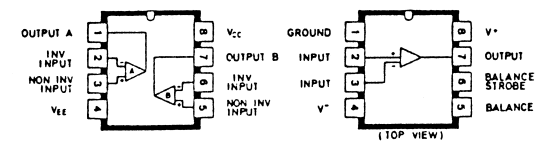
500-W Output Combiner

Ref. Designation 4439



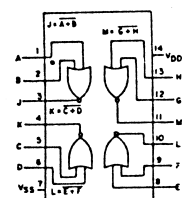
500-W Output Combiner
 Ref. Desig. 4439
 Component Location



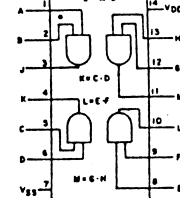


MC 1458

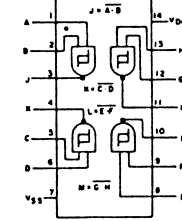
LM 311



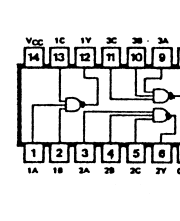
CD 4001



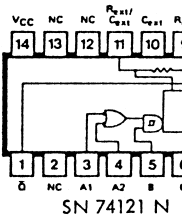
CD 4081



CD 4093



SN 7410 N



SN 74121 N

Note 1:

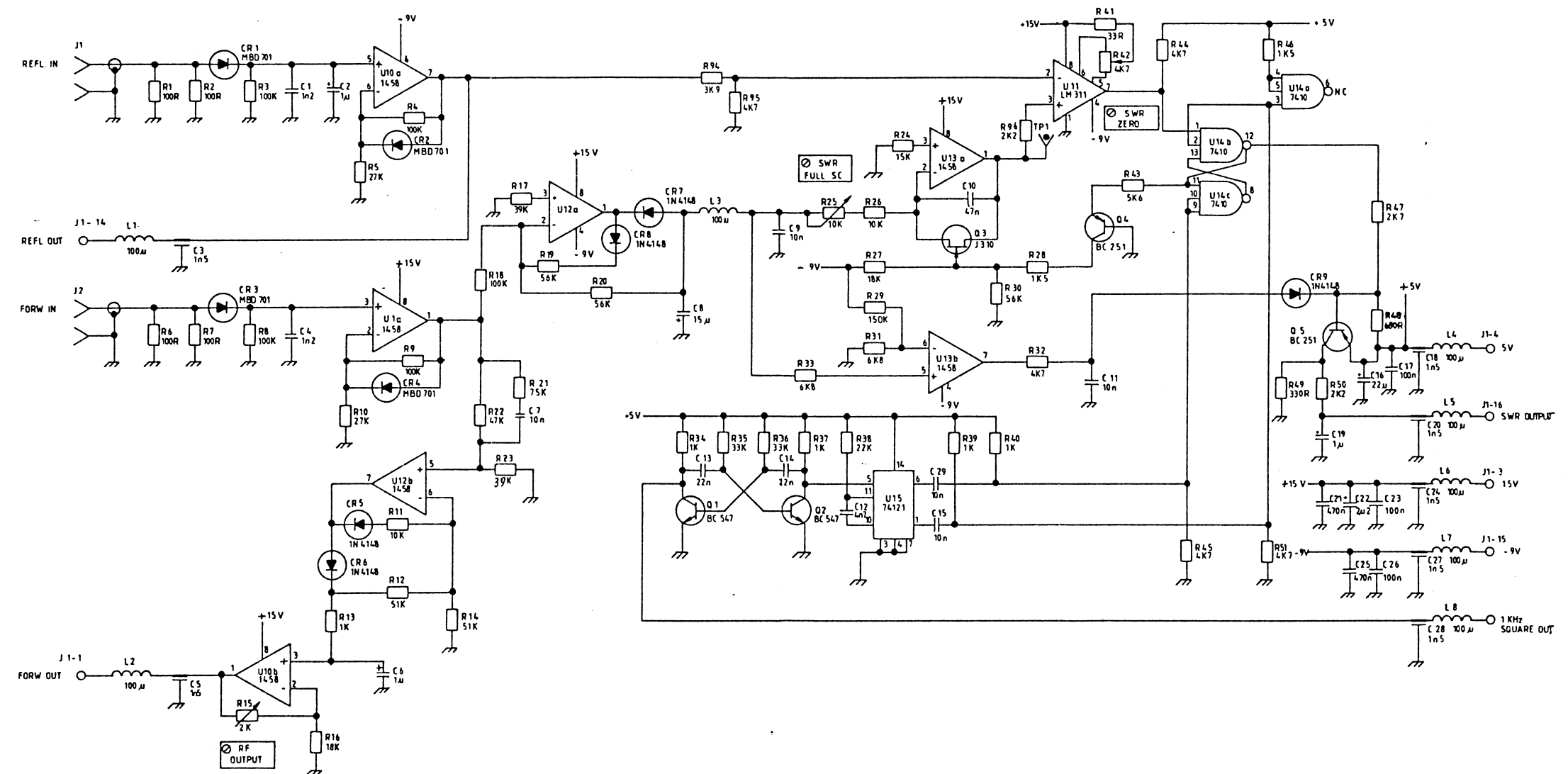
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

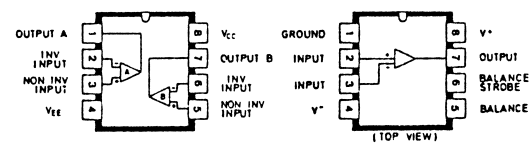
Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0,47 = 0,47Ω, but 4R7 = 4,7Ω.

The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

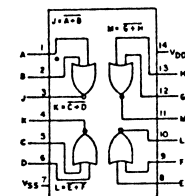
The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).



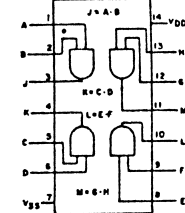


MC 1458

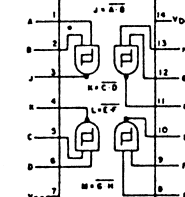
LM 311



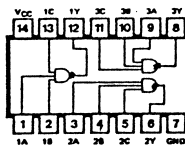
CD 4001



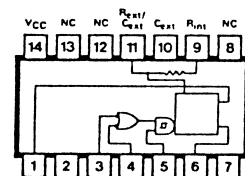
CD 4081



CD 4093



SN 7410 N



SN 74121 N

Note 1:

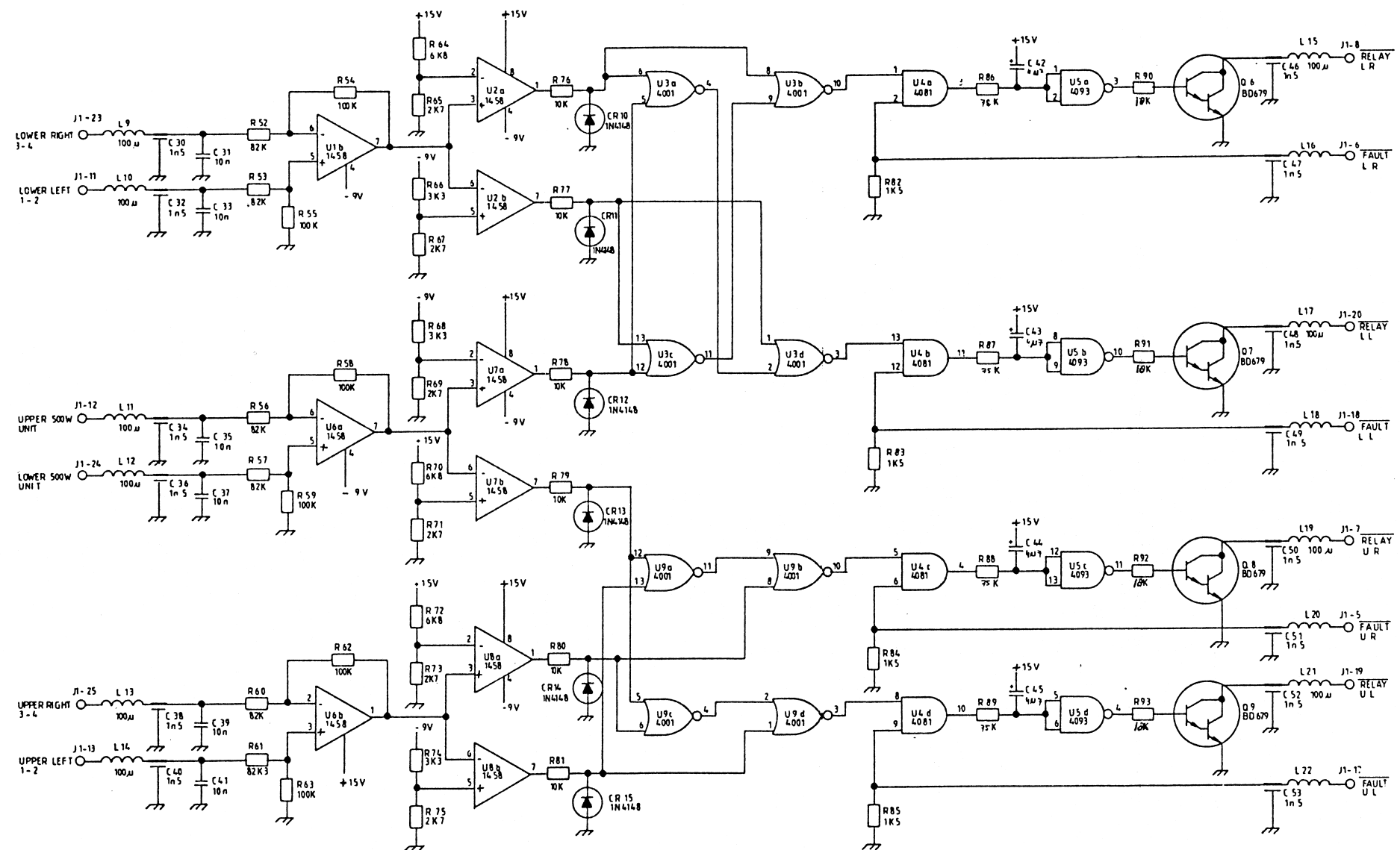
Partial Reference Designations are shown. For complete Designation prefix with Assembly and Subassembly Reference Designations (Circuit Diagram Nos.)

Note 2:

The code system used for indicating resistance values corresponds to that specified in IEC 62, with the exception that decimal fractions are used for values below 1Ω, e.g. 0.47 = 0.47Ω, but 4R7 = 4.7Ω.

The capacitance units are indicated by means of the international prefixes p, n, and μ, (pF, nF, and μF).

The inductance units are indicated by means of the international prefixes μ, and m, (μH, and mH).



- J1-1 DETECTOR UPPER RIGHT (3-4)
- J1-2 DETECTOR LOWER 500W UNIT
- J1-3 DETECTOR LOWER RIGHT (3-4)
- J1-4 NC
- J1-5 NC
- J1-6 RELAY-CONTROL LOWER LEFT
- J1-7 RELAY-CONTROL UPPER LEFT
- J1-8 THERM OR UNBAL LOWER LEFT
- J1-9 THERM OR UNBAL UPPER LEFT
- J1-10 SWR METER OUTPUT
- J1-11 -9V
- J1-12 REFLECTED OUTPUT
- J1-13 DETECTOR UPPER LEFT (1-2)
- J1-14 DETECTOR UPPER 500W UNIT
- J1-15 DETECTOR LOWER LEFT (1-2)
- J1-16 NC
- J1-17 SQUARE OUT 1KHz
- J1-18 RELAY-CONTROL LOWER RIGHT
- J1-19 RELAY-CONTROL UPPER RIGHT
- J1-20 THERM OR UNBAL LOWER RIGHT
- J1-21 THERM OR UNBAL UPPER RIGHT
- J1-22 +5V
- J1-23 +15V
- J1-24 GND
- J1-25 FORWARD OUTPUT

CONFIGURATION TU4013

The signal from the transmitter is used by the Detector Assembly A9 to measure the forward power, the reverse power, and the phase and modulus of the antenna impedance. This information is used, together with frequency information, by the Controller Assembly A8 to decide which tuning procedure and preset values to use.

The tuning elements are configured as an L-led with a lowpass characteristic.

The assemblies A1, A3, A4 and A5 form a narrowband tuner with two possible configurations, one being the capacitive element (A5) located at the transmitter input, the other being the capacitive element located at the antenna output.

The Dummy Load Assembly A2 serves as a test load during transmission and ATU selftest.

Assembly A6 and A7 are the broad band tuning elements used for compensation.

The Controller Assembly A8 performs the overall control of the antenna tuner and the data transmission between TU4013 and SE4010.

Typical tasks handled by the assembly:

- Control of the individual assemblies.
- Calculations.
- Programmable memory set-ups.
- Data communication.
- Diagnostic routines.
- Adaptive tuning control.

Communication between the Controller Assembly and the remaining assemblies is conducted over two ribbon cables. One cable contains the relay control lines, supervisory lines and supply for all assemblies except the Detector Assembly A9.

The other cable contains supply for the Controller Assembly and the Detector Assembly A9, as well as control and data lines between the the Controller and the Detector Assembly.

The Power Supply Assembly A10 supply the four voltages used by the assemblies in the tuner. The power supply can operate both on 115 and 220 Vac, single phase. Because of noise consideration the power supply is a linear type.

The Temperature Control Assembly A13 controls the blowers used for forced air circulation, activated at approximately 35°C, and the heating elements, activated at approximately +10°C, used under low temperature conditions.

DUMMY LOAD A2/TU4013

Assy 210453-001

The Dummy Load consists of three resistors in series with a combined value of 49 ohms.

When the control lines 7R, 14R and 28R are high the relay K5 is automatically energized and the series combination of the three resistors is grounded forming a dummy load with a value of 49ohms.

When the control line RS ON is activated, thereby energizing K4, the resistors are used to lower the Q of the antenna during broad band operation, by inserting the resistors in series with the tuning elements. During the broad band tuning a maximum of two resistors are available to avoid energizing the relay K5.

The Dummy Load is temperature-protected by a temperature measuring device R5. The circuit around U1 forms a comparator supervised by the Controller. The attack level of the protection is a temperature of 100°C and a decay temperature of approximately 80°C.

Assy 210453-002

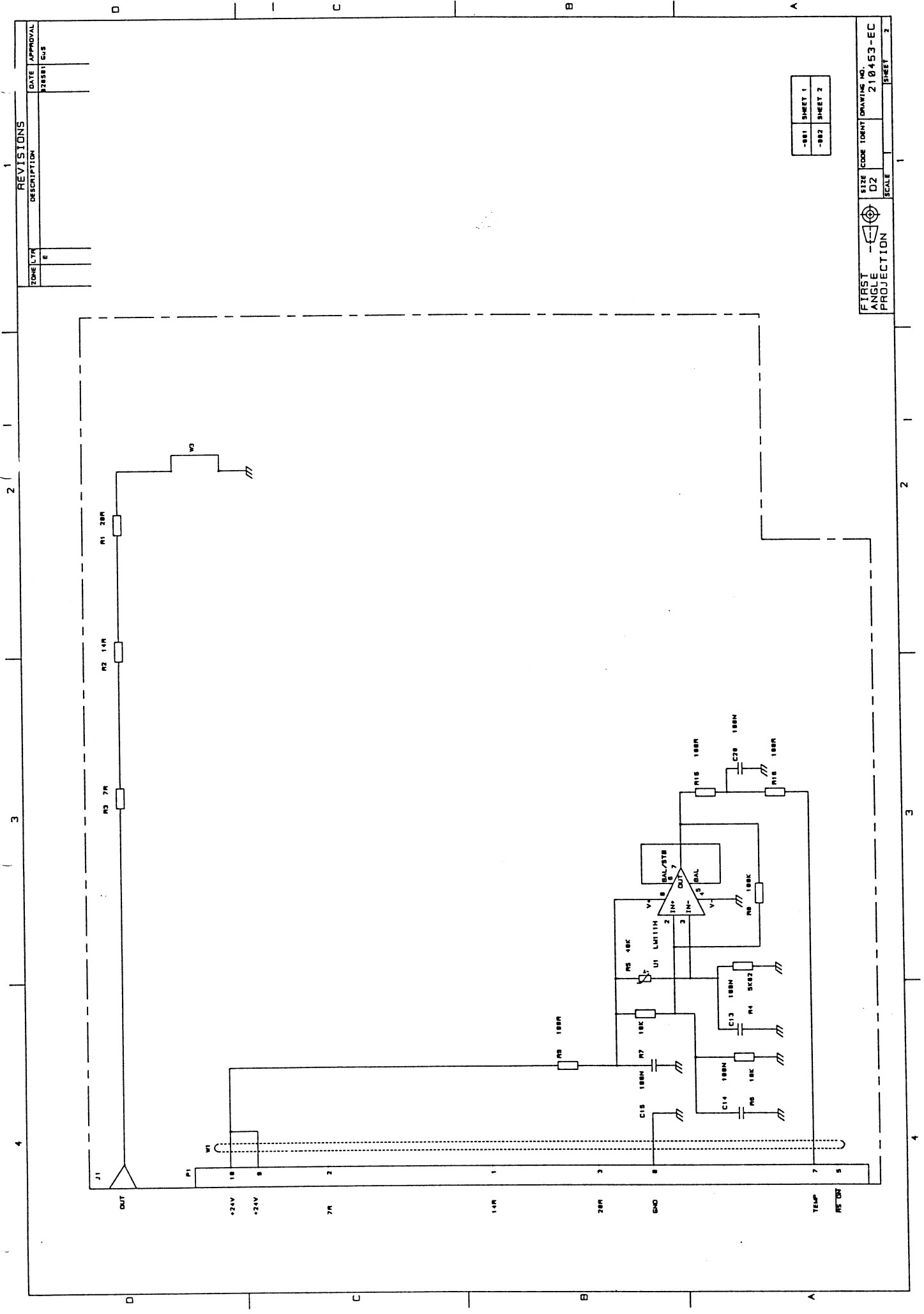
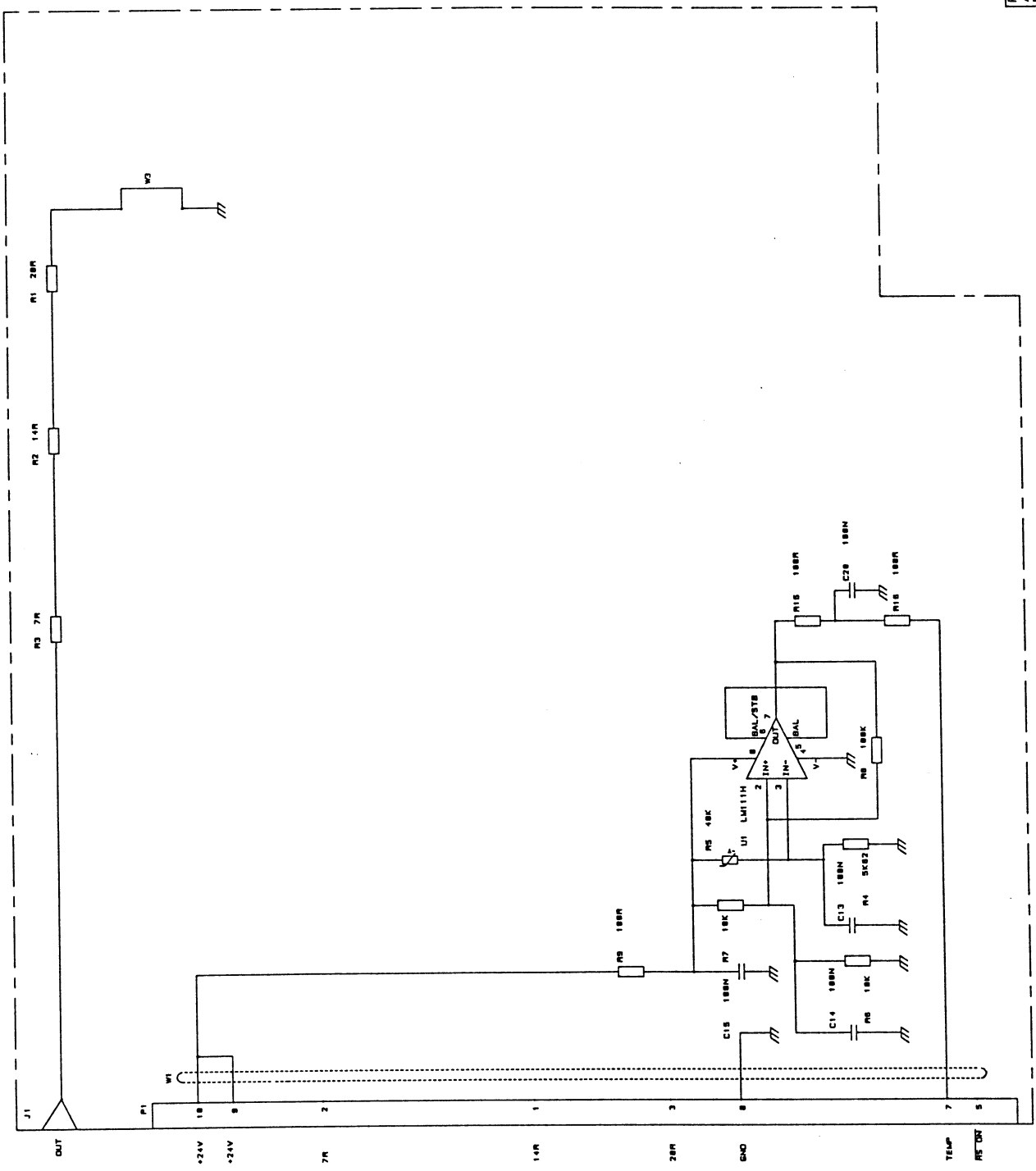
The Dummy Load consists of three resistors in series with a combined value of 49 ohms grounded by the jumper W3.

The Dummy Load is temperature-protected by a temperature measuring device R5. The circuit around U1 forms a comparator supervised by the Controller. The attack level of the protection is a temperature of 100°C and a decay temperature of approximately 80°C.

REVISIONS	
DATE	APPROVAL
3/28/81	GUS
ZONE LTR	
E	

-881	SHEET 1
-882	SHEET 2

FIRST ANGLE PROJECTION	SIZE D2	CODE 100T	DRAWING NO. 210453-EC	SHEET	
				1	2

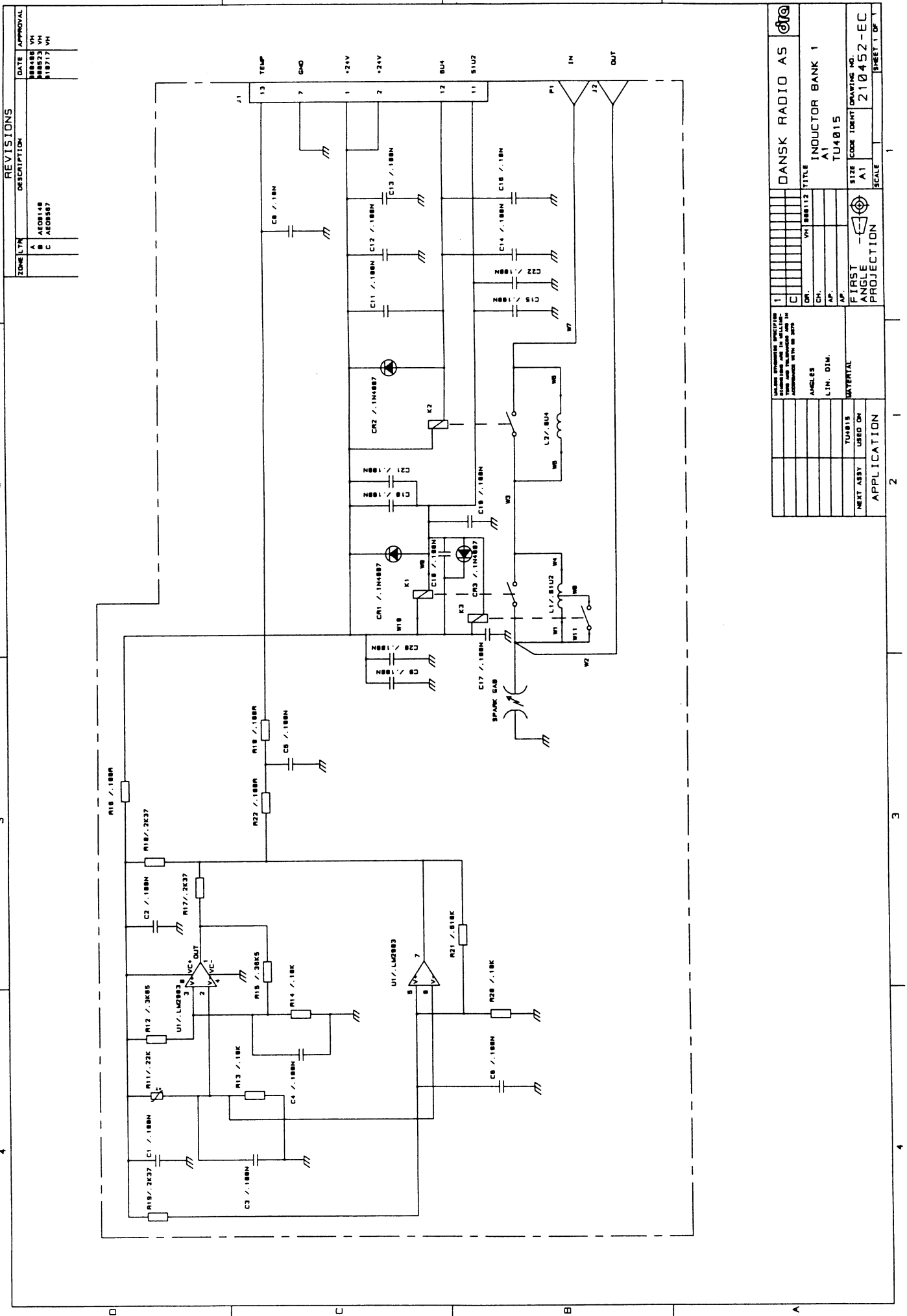


INDUCTOR BANK 1 A1/TU4013

The two inductors in Inductor Bank 1 are activated by a high level on the control input on J1.

To protect the tuner from high voltages a spark gap is located close to the antenna outlet.

A dual temperature measuring circuit, supervised by the controller, is located on the Inductor Bank 1. Both measuring devices are formed as comparators. One of the temperature measuring circuits, U1a, has an attack temperature of 70°C and hysteresis of 10°C. The output is tied together with the output from the second temperature measuring device, U1b, through a resistor R17. The second temperature measuring device has an attack level of 80°C.



REVISIONS		DATE	APPROVAL
ZONE	LTN	DESCRIPTION	
A	AE08148		VH
B	AE08253		VH
C	AE08387		VH

DANSK RADIO AS		INDUCTOR BANK 1	
DR.	VH	CH.	A1
AP.		AP.	TU4015
FIRST ANGLE PROJECTION		SIZE CODE IDENT DRAWING NO	
		A1 210452-EC	
APPLICATION		SCALE	
		SHEET 1 OF 1	

INDUCTOR BANK 2 A3/TU4013

The Inductor Bank 2 consists of two inductors and a current transformer. The inductors are controlled by K1 and K2, the inductors being active when a high level is present at the control input on J1.

The current transformer, T1, is used to measure the current in the inductors and thereby the antenna current. The current in the transformer is converted to a voltage by R5 and the rectified (by CR2) voltage is buffered by U1 giving an output voltage of +10 Vdc with a RF-current of 14 Arms.

The Inductor Bank has two outputs, one for interconnection to Inductor Bank 1 (through K3) and one for interconnection to the Dummy Load (through K4). The energizing of K3 is done with a high level on the control terminal RS ON. A low level on the control terminal energizes K4 and turns on Q1, thereby turning Q2 off, de-energizing K3.

The control signals for the Dummy Load A2 are routed through the Inductor Bank 2.

INDUCTOR BANK 3 A4/TU4013

The Inductor Bank 3 consists of seven inductors and one capacitor (formed by 3 capacitors in parallel, namely C25-26-27). The inductors are controlled by the relays K1 through K7, while the capacitor (used for compensation of residual induction) is controlled by K8.

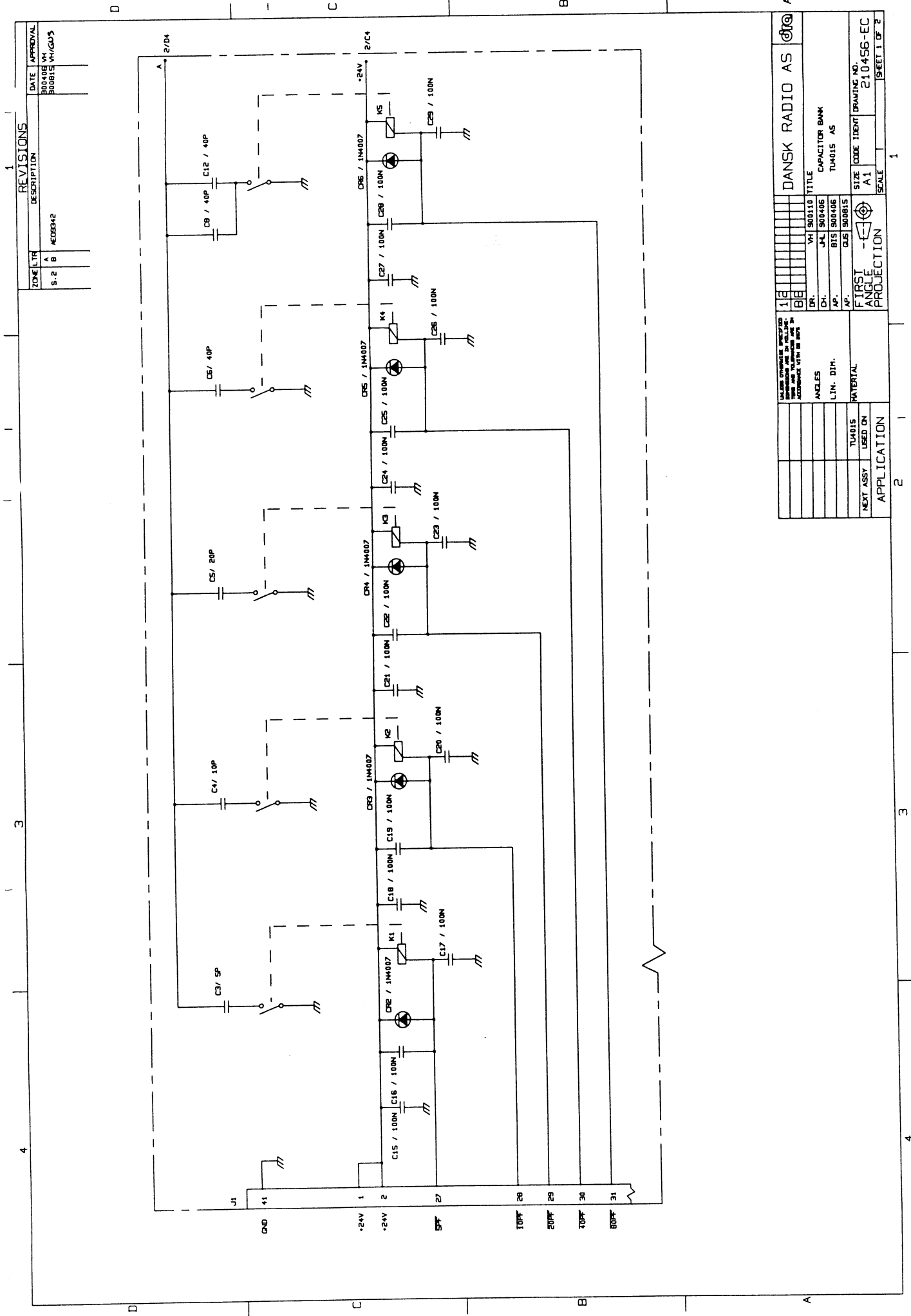
Both the inductors and the capacitor are active when a high level is present on the control pins on J1.

Parallel with the capacitors, C25-C26-C27, two resistors are located. These resistors are used as DC-pass for the static discharge of the tuner.

CAPACITOR BANK (1) A5/TU4013

The Capacitor Bank consists of 22 high power capacitors forming binary weighted sequence of 11 bits (the highest value consists of two capacitors, C13-C14, in parallel) with a minimum resolution of 5 pF.

The capacitors are controlled through the relays K1 through K12, each relay is energized by a low level on the control pin on J1.



REVISIONS	
ZONE / TR	DESCRIPTION
5.2 B	AED8342
DATE	APPROVAL
300408 VH	300815 VH/GDS

DANK RADIO AS	
1	2
DR	YH 500110
CH	J4 500408
AP	BIS 500408
AP	CUS 500815
AP	TL4015
AP	USED ON
AP	APPLICATION
AP	ANGLE
AP	PROJECTION
AP	SIZE
AP	CODE IDENT
AP	DRAWING NO.
AP	210456-EC
AP	SHEET 1 OF 2

CAPACITOR BANK (2) A5/TU4013

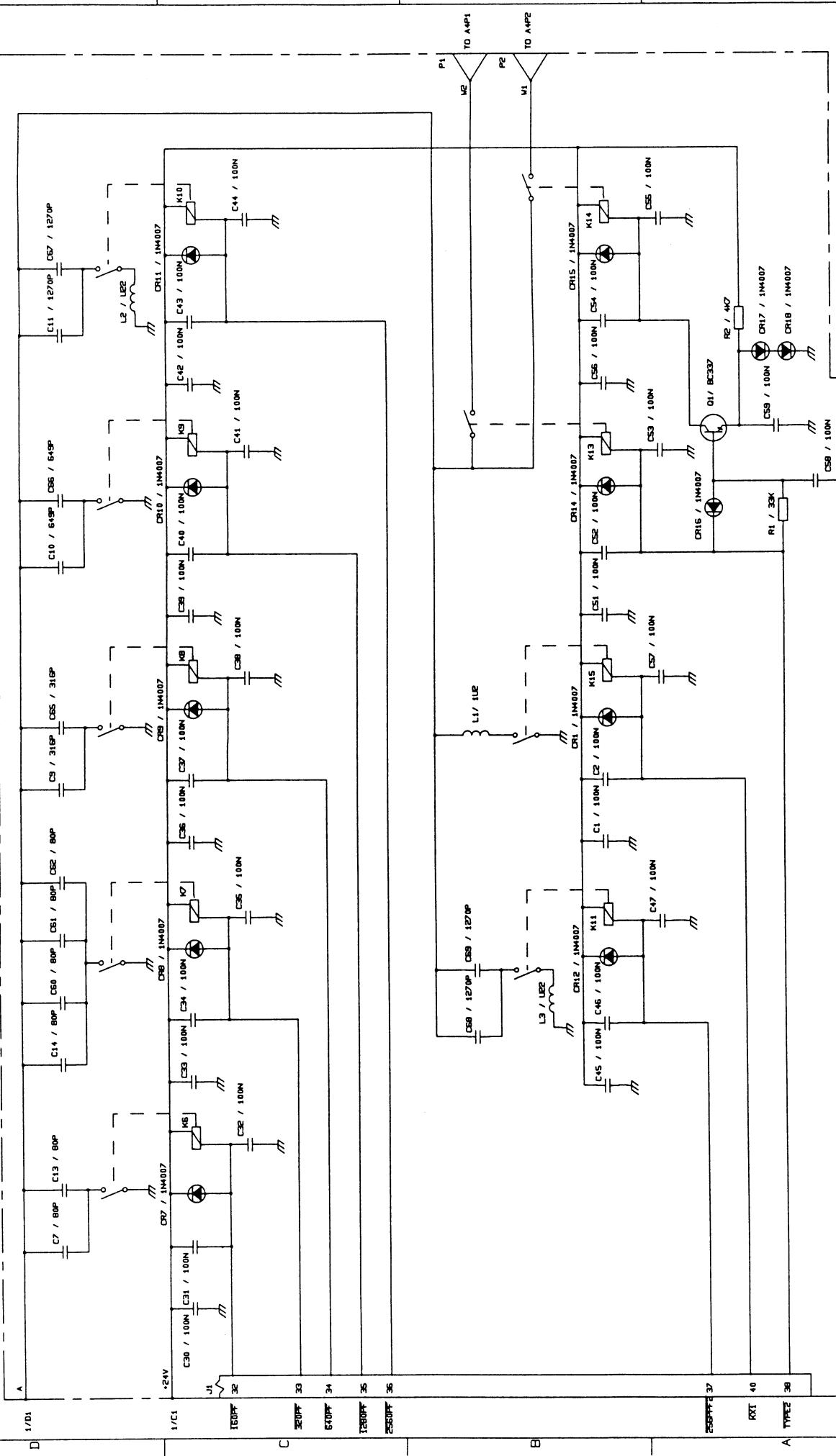
The inductor, L1, is used to compensate for the stray capacitance in the circuit.

The Capacitor Bank has two outputs, each output defining the configuration of the tuner.

When the tuner is in the Type 1 mode the output from the capacitor is P2 through K14.

When the tuner is in the Type 2 mode Q1 is cut off, thereby de-energizing K14 while the output is P1 through K13.

REVISIONS	
DATE	APPROVAL
300408	YH
300815	YH/QDS
ZOE LTR	
A	AEDE342
B	



FIRST ANGLE PROJECTION	SIZE A1	CODE 10041	DRAWING NO. 210456-EC
SCALE	1	SHEET	2

BROADBAND 1 A6/TU4013

Assy 210461-001

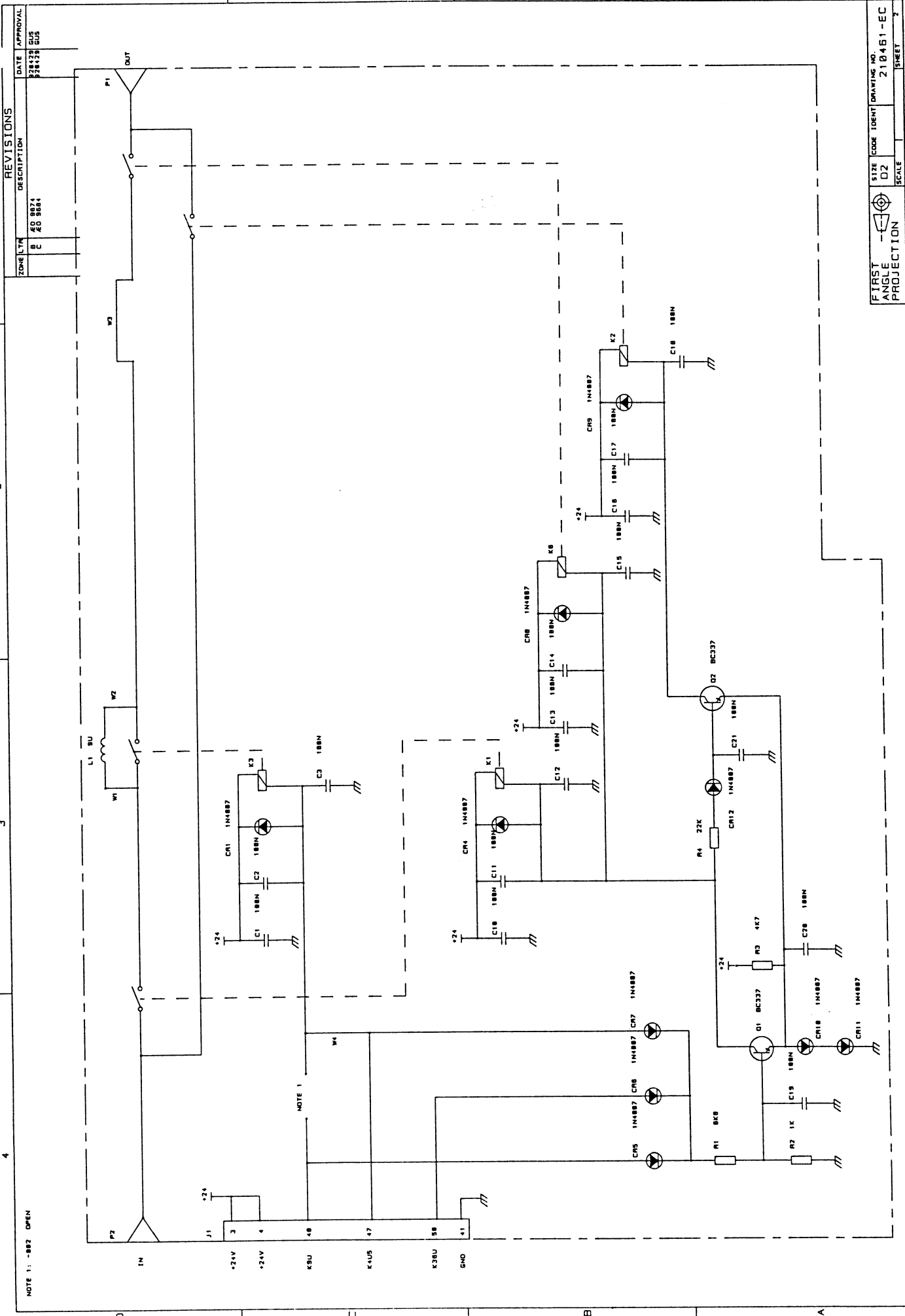
The three inductors (L1-L2-L3) are controlled through the relays K3-K4-K5. The inductors are active when a high level is present at one of the control inputs on J1.

To ensure a low residual inductance when none of the inductors are active three more relays are used, one for bypassing and two for disconnection. When no inductors are active relay K2 is active through Q2, thereby bypassing the inductors. If one or more of the inductors are activated the collector of Q1 goes low, thereby energizing K1 and K6 and turning off Q2, thereby de-energizing K2.

Assy 210461-002

The inductor, L2, is controlled through the relay K3. The inductor is active when a high level is present at the control input on J1.

To ensure a low residual inductance when none of the inductors are active three more relays are used, one for bypassing and two for disconnection. When the inductors are non-active, relay K2 is active through Q2, thereby bypassing the inductors. If the inductors are activated the collector of Q1 goes low, thereby energizing K1 and K6 and turning off Q2 and thereby de-energizing K2.



BROADBAND 2 A7/TU4013

Assy 210462-001

The inductor (L1) and the capacitors (C22 through C27) are controlled by the relays K1 through K6.

K7 is used to bypass the capacitors.

The inductor is active when a high level is present at the control pin while the rest of the functions are active when a low level is present.

All capacitors with a value of 10 nF are used to decouple the control lines before entering the Controller.

The two resistors, R1-R2, function as static discharge for the tuner.

Assy 210462-002

The capacitors (C22 through C27) are controlled by the relays K2 through K6.

K7 is used to bypass the capacitors.

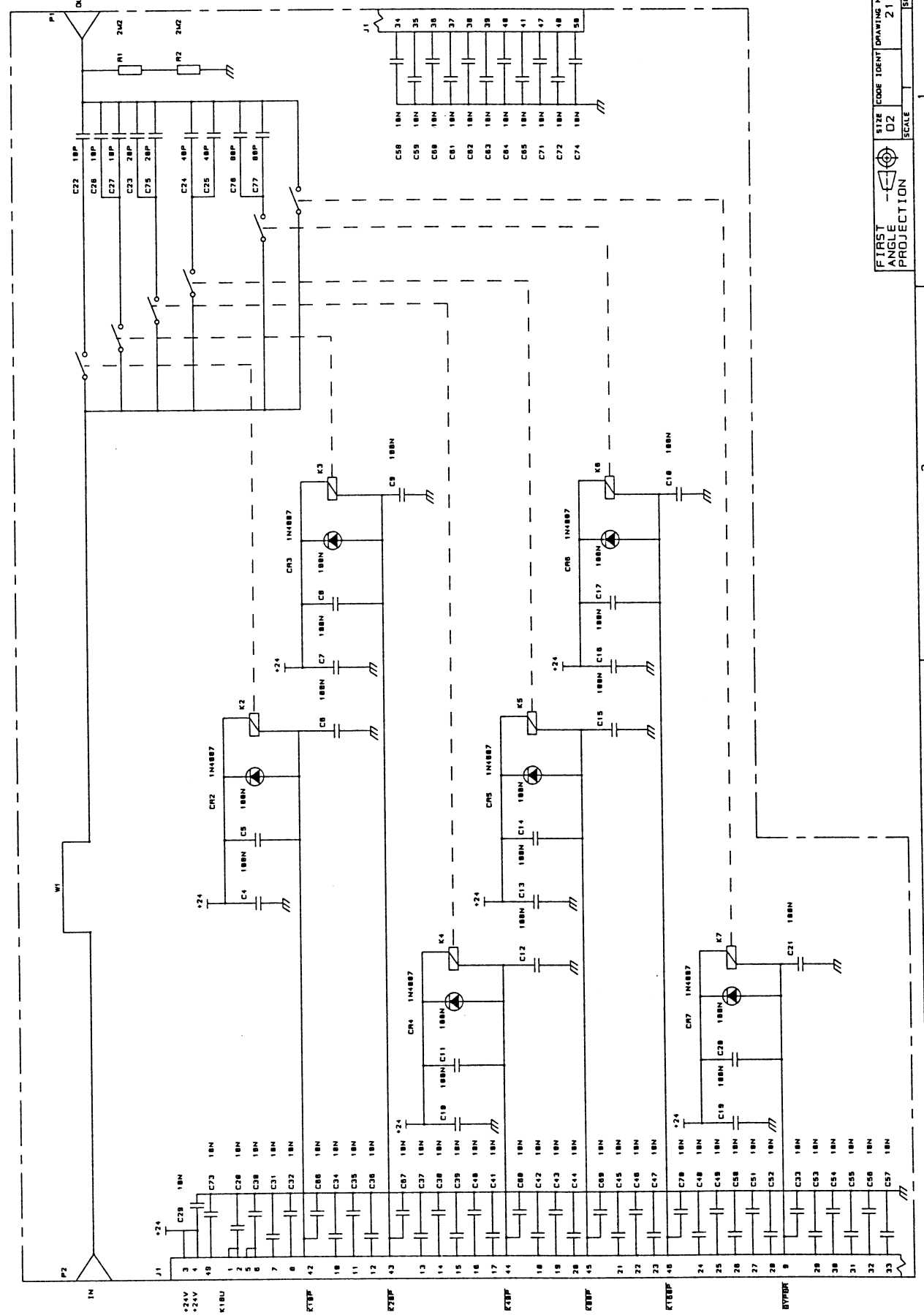
All capacitors with a value of 10 nF are used to decouple the control lines before entering the Controller.

The two resistors, R1-R2, function as static discharge for the tuner.

1 2 3 4

REVISIONS

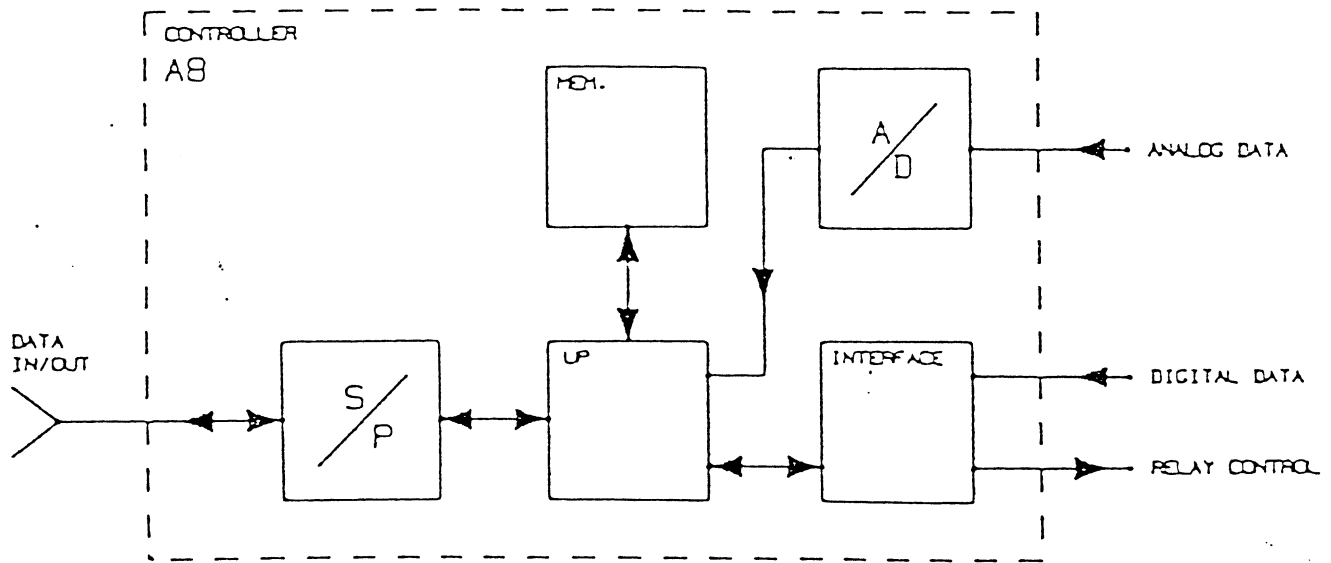
ZONE	DATE	APPROVAL
8	EO 8874	28428 GUS

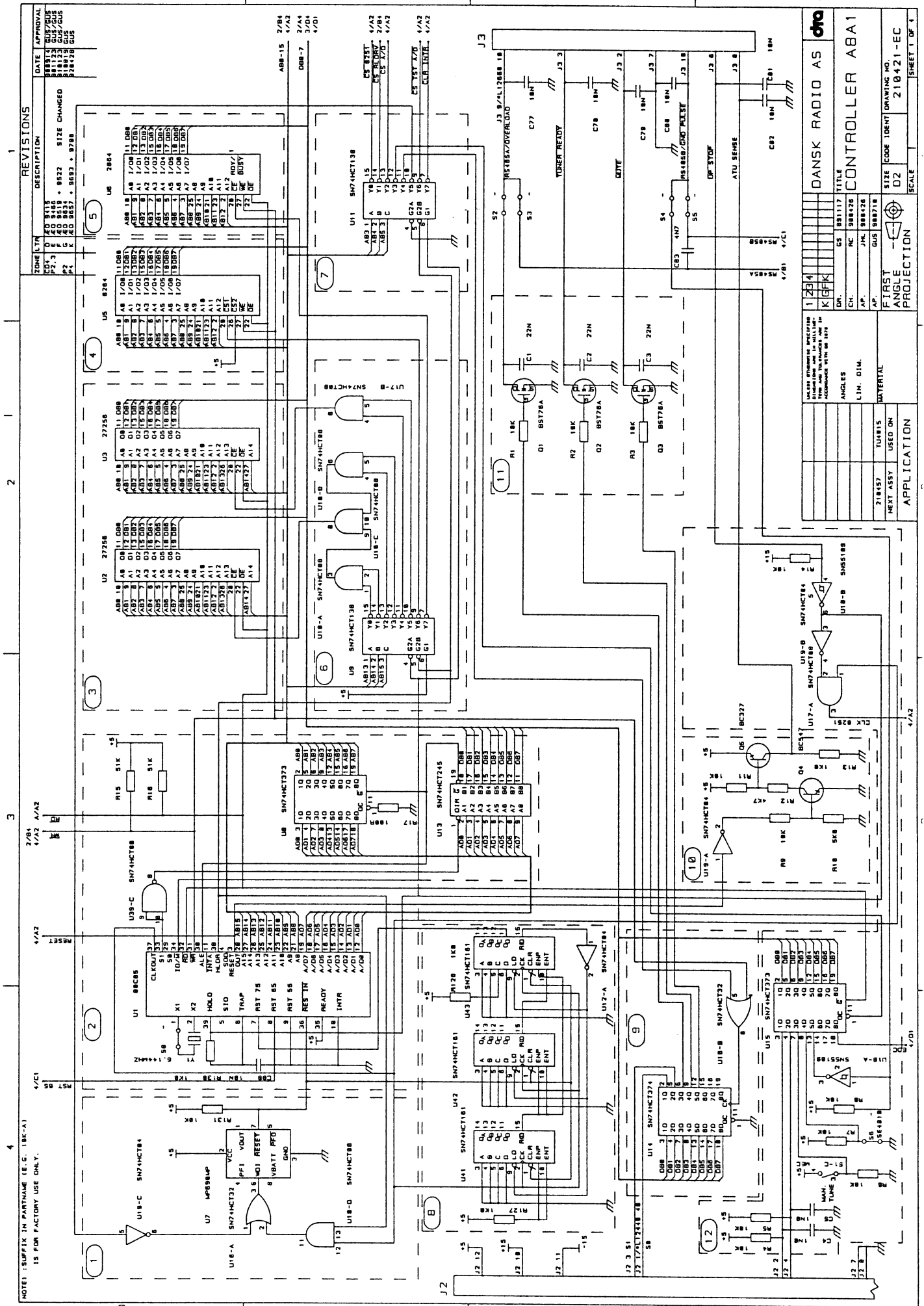


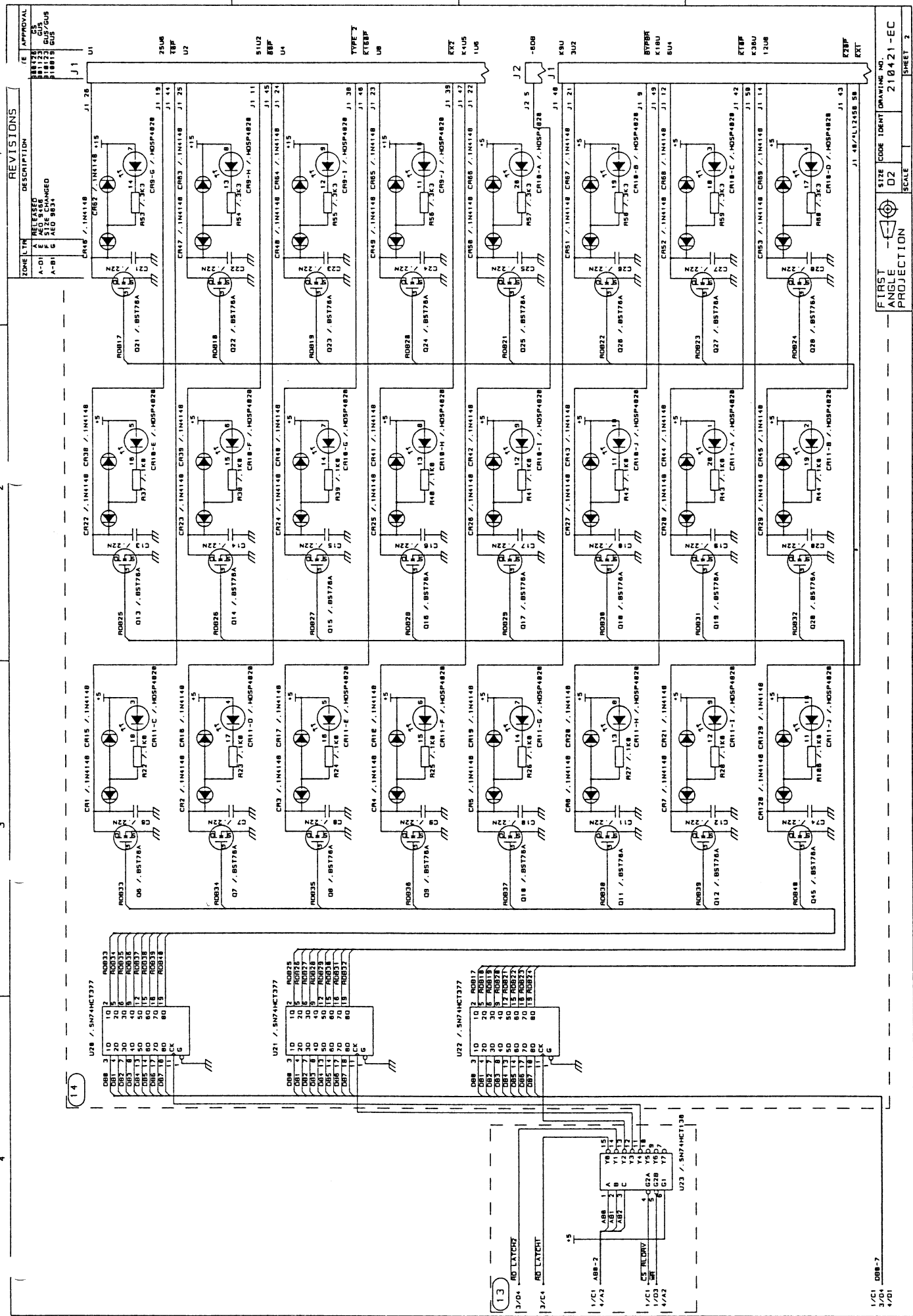
FIRST ANGLE PROJECTION	SIZE D2	CODE IDENT 210462-EC	SHEET 2
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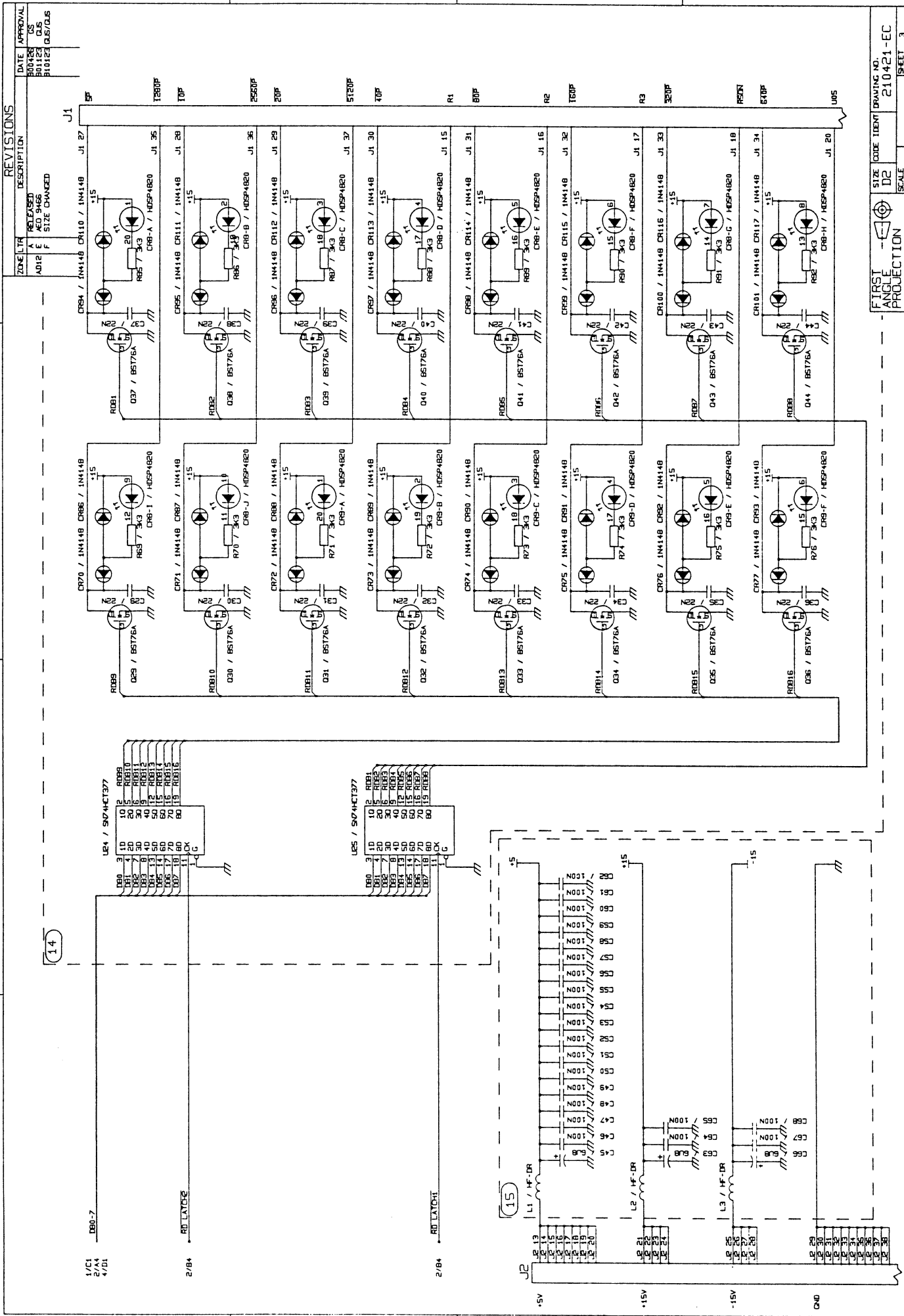
MICROPROCESSOR MODULE A8/TU4013

The functional block diagram is shown below:









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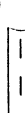
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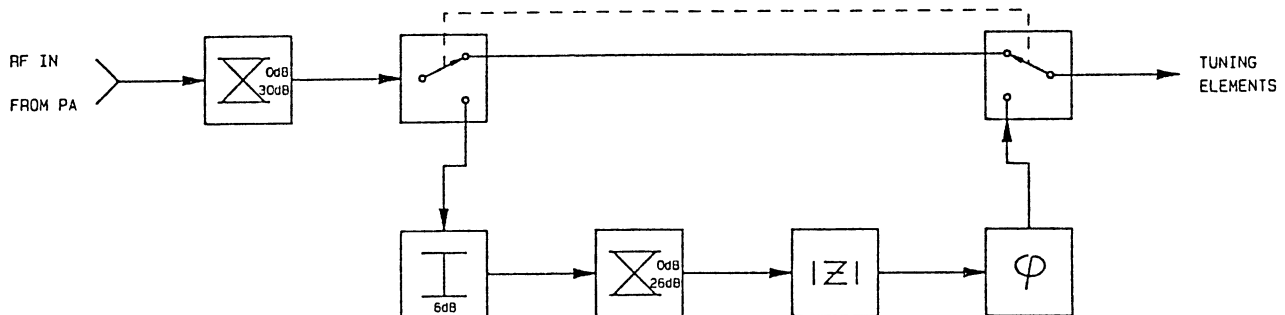
REVISIONS



CS	/C1
CS	/C1
AC	/O3
AF	Z/84
CS	/C1
AE	/O3
AE	/C1
CS	A3
CS	/C1

E	CODE IDENT	OR
E		

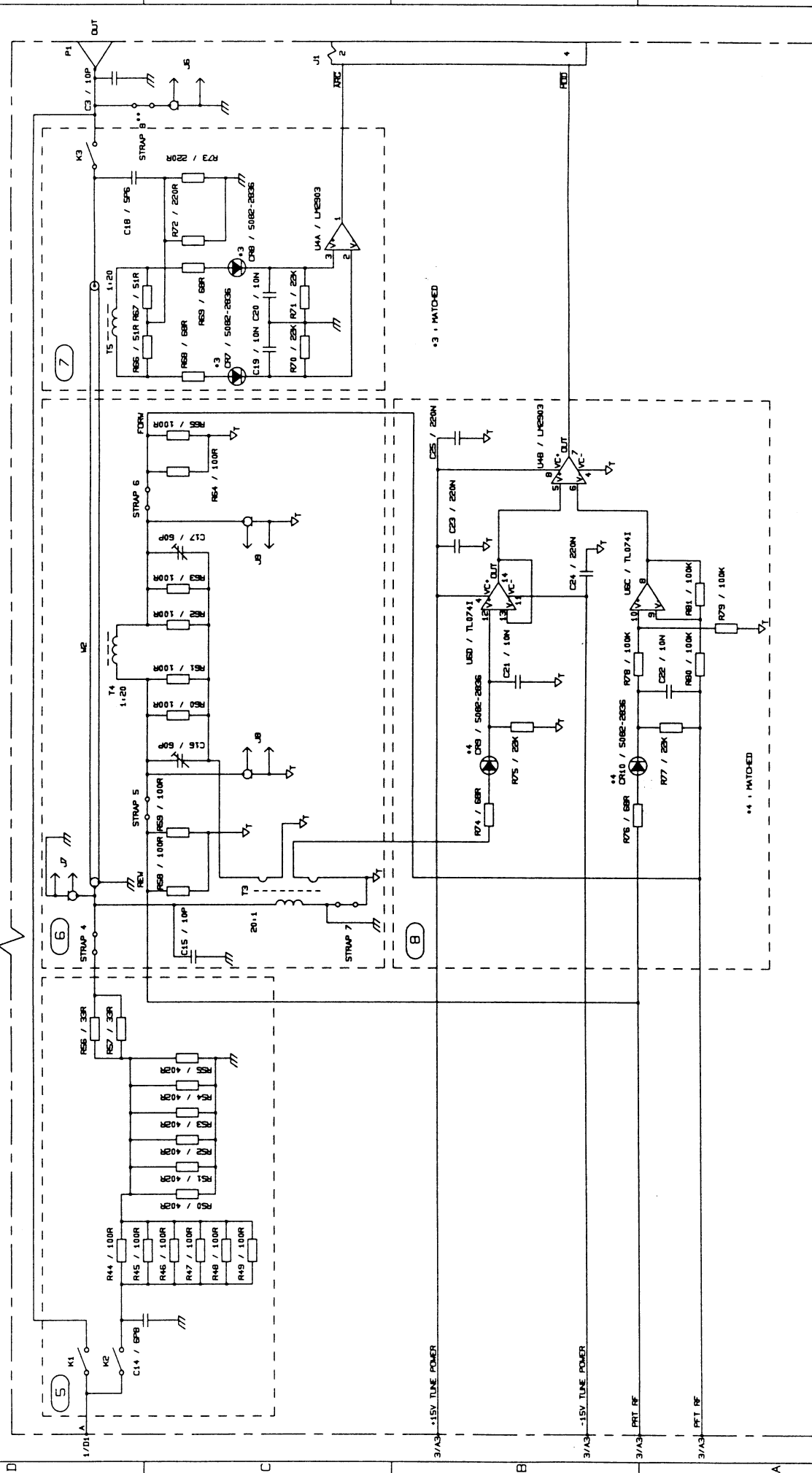
DETECTOR MODULE A9/TU4013



The signal from the transmitter is used by the Detector Assembly A9 to measure the forward power, the reverse power, and the phase and modulus of the antenna impedance. This information is used, together with frequency information, by the Controller Assembly A8 to decide which tuning procedure and preset values to use.

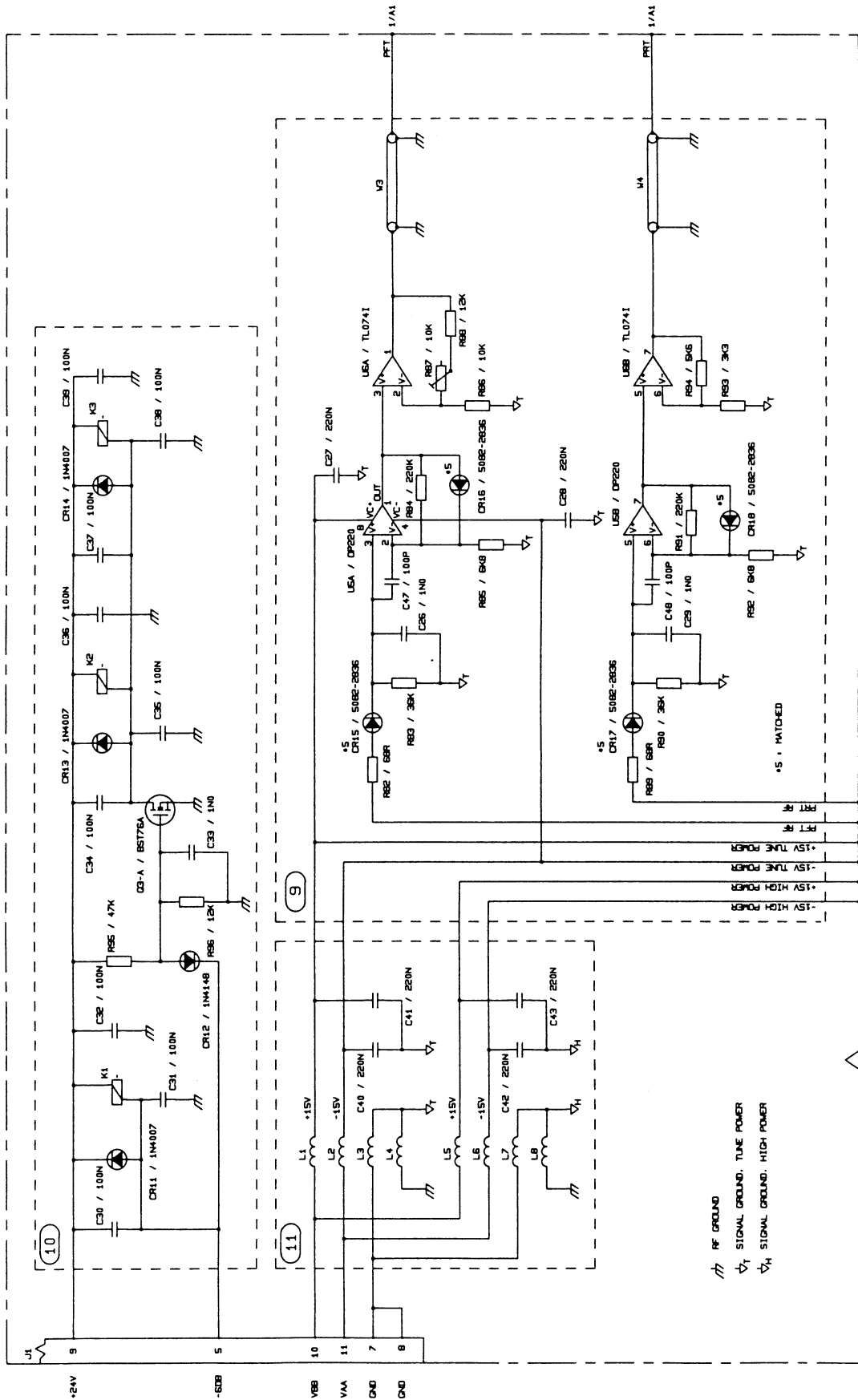
•1 : MATCHED
•2 : MATCHED

ZONE	LT#	DESCRIPTION	DATE	APPROVAL
A	8	REVISION	8/04/03	VH
B	9	REVISION	8/04/03	VH
C	10	REVISION	8/04/03	VH
D	11	REVISION	8/04/03	VH



FIRST	ANGLE	PROJECTION	SIZE	IDENT	DRAWING NO.	SHEET
1	1	1	A1	210458-EC	2	2

REVISIONS		DATE	APPROVAL
ZONE LTR	DESCRIPTION		
A		300405	VH



RF GROUND
 SIGNAL GROUND, TUNE POWER
 SIGNAL GROUND, HIGH POWER

FIRST ANGLE PROJECTION	SIZE CODE IDENT	DRAWING NO.
	A1	210458-EC
SCALE		SHEET 3

POWER SUPPLY A10/TU4013

1 +5 V, 600 mA Regulator

U3 is a common used +5 V regulator, 7805, with extended temperature range. Thyristor Q8 is normally on. If CR15 is pulled to GND, through Q11, the basis current is removed from Q7 and thereby the gate current for Q8, turning the +5 V supply off.

2 +15 V, 160 mA Regulator

The circuit functions in the same manner as 1, except that U2 pin3 is lifted to +10 V with Q6, R7-8 to give an output voltage of +15 V.

3 -15 V, 130 mA Regulator

The circuit functions in the same manner as 1, except that U1 pin3 is lifted to +10 V with Q3, R3-4 to give an output voltage of +15 V.

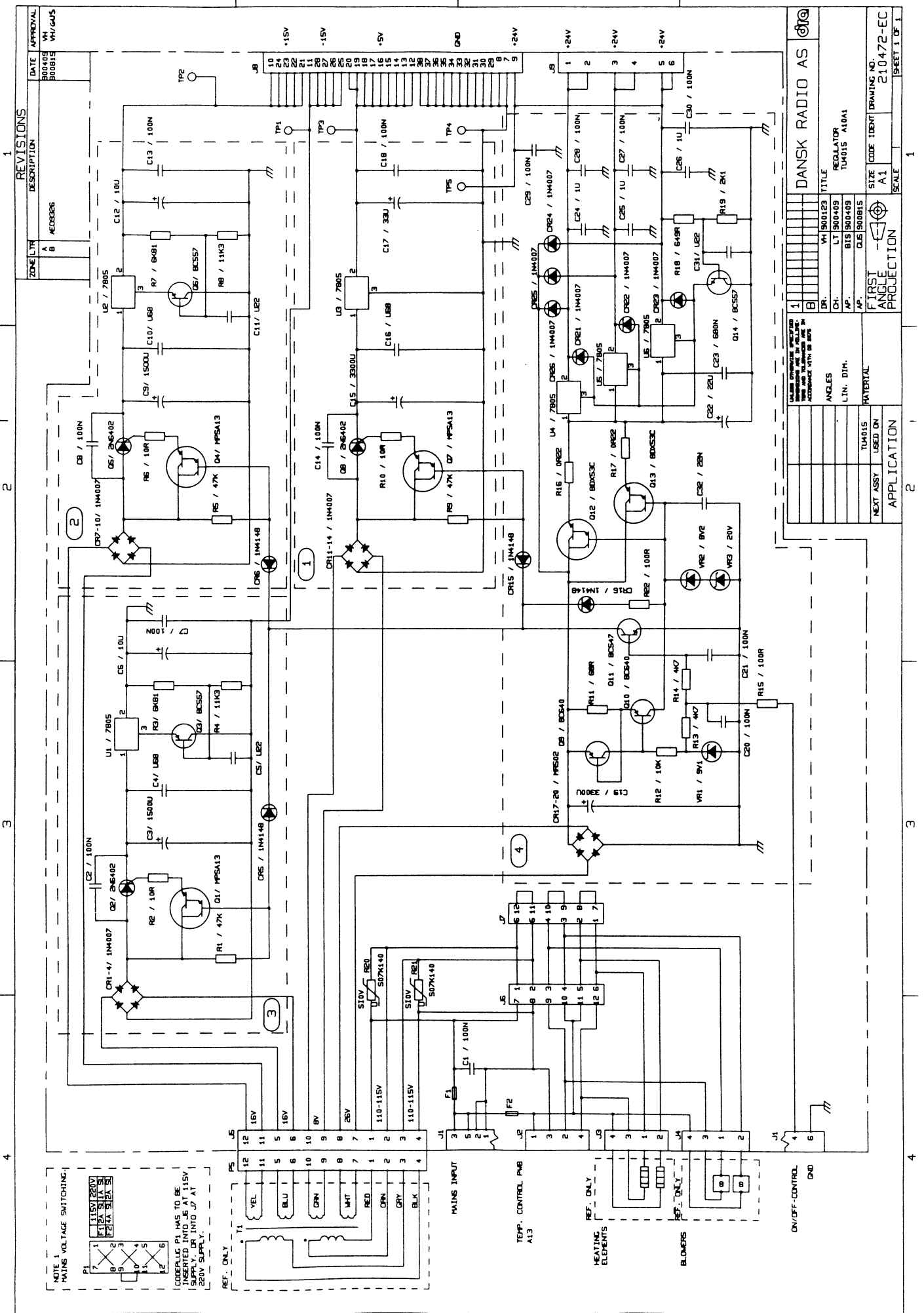
The output from the regulator is grounded and the output is taken from the negative input, thereby giving an output of -15 V.

4 +24 V, 3*600 mA Regulator

U4-5-6 are lifted to +19 V with Q14, R18-19 to give an output voltage of +15 V.

Q12-13 act as pre-regulators, with Q9-10 used as current regulators for VR2-3 to give a constant input voltage of +27 V to U4-5-6. CR16 cuts off the +24 V supply through Q11.

A logical 0 at J1 pin4 forces Q11 to go off, thereby turning the four supply voltages on.



PRINCIPLES OF TUNING TU4013

Introduction to Tuning

The TU4013 can be tuned by different procedures. The procedures are accessible on two levels.

The first level is the automatic narrow band tune procedure which is initiated every time the [tune] key is pressed.

The second level is only accessible through the program mode where manual tuning and manual/ silent tuning is performed.

The Tuning Strategy

The TU4013 is configured as an L-matching circuit with a lowpass characteristic. The capacitor in the circuit can be located at two places as shown in figure 1.

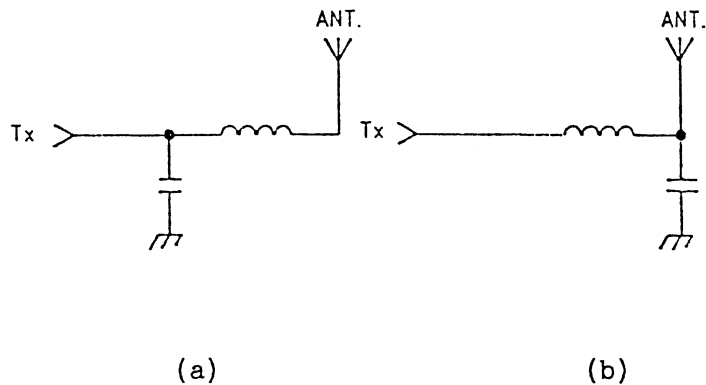


Figure 1

Figure 1a is identified as Type 1 and 1b as Type 2. The choice of type to use during tuning is made automatically by the program in automatic tuning and by the operator in manual tuning.

PRINCIPLES OF TUNING TU4013

The tuning strategy operates in a Polar Impedance chart, shown in figure 2.

The Polar Impedance chart is divided into four quadrants, numbered 1 through 4. This information allows the operator to detect in which quadrant the antenna impedance is located.

With the aid of the quadrant and SWR information the operator can manually set the elements of the tuner to obtain a low SWR.

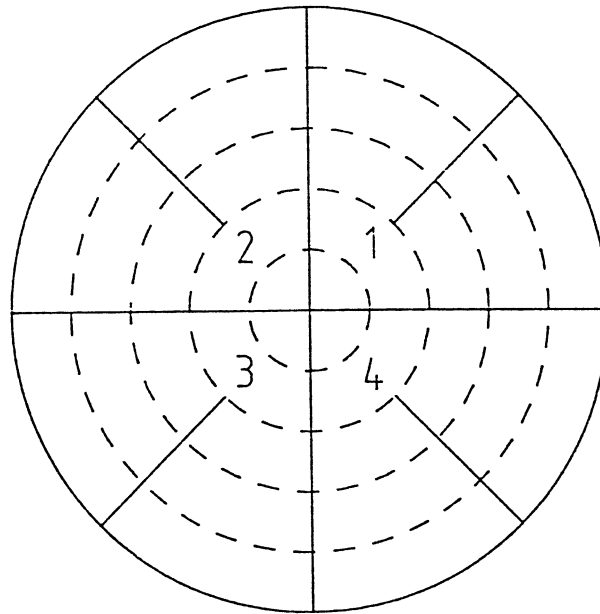


Figure 2

PRINCIPLES OF TUNING TU4013

Elements Available

The elements in the tuner are configured in a binary sequence.

The inductor elements are presented to the operator as numbers between 0 and 2047.

The numbers for the inductors correspond to a factor of 0.05 uH/bit.

When operating with a Type 1 configuration the greatest number for the inductors available is 2047, while in a Type 2 configuration the greatest number available is 255.

The capacitor elements are presented to the operator as a number between 0 and 1535 in the frequency range 1.5-26.112 MHz and as a number between 0 and 511 in the frequency range 26.112-29.999 MHz.

The numbers for the capacitors correspond to a factor of 5pF/bit.

PRINCIPLES OF TUNING TU4013

Example of Manual Tuning with a Type 1 Configuration

Figure 3 shows a Polar Impedance chart with a typical impedance point for a 12 meter whip antenna at a low frequency.

Tuning is carried out by increasing the value of the inductor, whereby the impedance of the antenna is shifted around the Polar impedance chart along the line marked L in figure 3, until a shift from quadrant 2 to 1 is obtained.

The next step is to increase the value of the capacitors, whereby a shift from quadrant 1 to 4 is obtained. The value of the capacitor is decreased so a shift from quadrant 4 to 1 is obtained. Next the value of L is decreased until quadrant 2 is obtained. The value of the inductor is then increased so a shift from quadrant 2 to 1 is obtained.

Next the value of C is increased until quadrant 1 is obtained and so on.

Through these shifts between quadrant 1, 2 and 4 with the L and C elements the SWR of the tuner will decrease, as indicated on the bargraph meter, to an acceptable level.

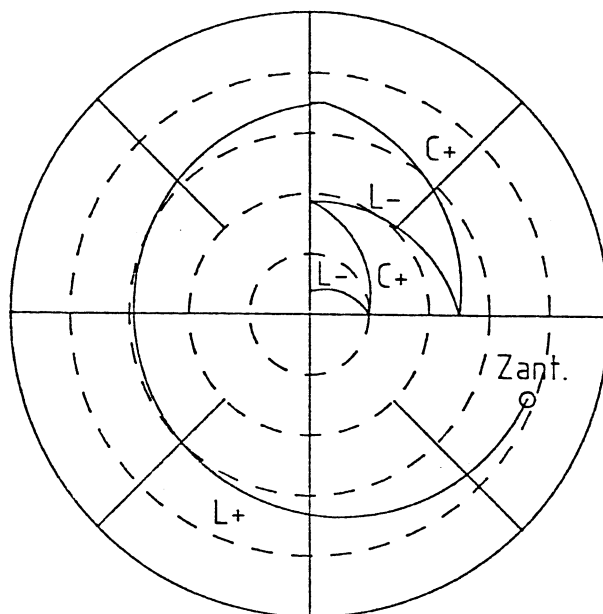


Figure 3

PRINCIPLES OF TUNING TU4013

Example of Manual Tuning with a Type 2 Configuration

Figure 4 shows a Polar Impedance chart with a typical impedance point for a 12 meter whip antenna at a high frequency.

Tuning is carried out by increasing the value of the capacitor, whereby the impedance of the antenna is shifted around the Polar impedance chart along the line marked C in figure 4, until a shift from quadrant 3 to 2 is obtained.

The operator may experience that a shift from quadrant 3 to 2 is not possible. In this case increase the value of L to obtain the shift.

The next step is to increase the value of the inductors, whereby a shift from quadrant 2 to 1 is obtained. The value of the inductor is then decreased so a shift from quadrant 1 to 2 is obtained.

Next the value of C is decreased until quadrant 3 is obtained. The value of the capacitor is then increased so a shift from quadrant 3 to 2 is obtained.

Through these shifts between quadrant 1, 2 and 3 with the L and C elements the SWR of the tuner will decrease, as indicated on the bargraph meter, to an acceptable level.

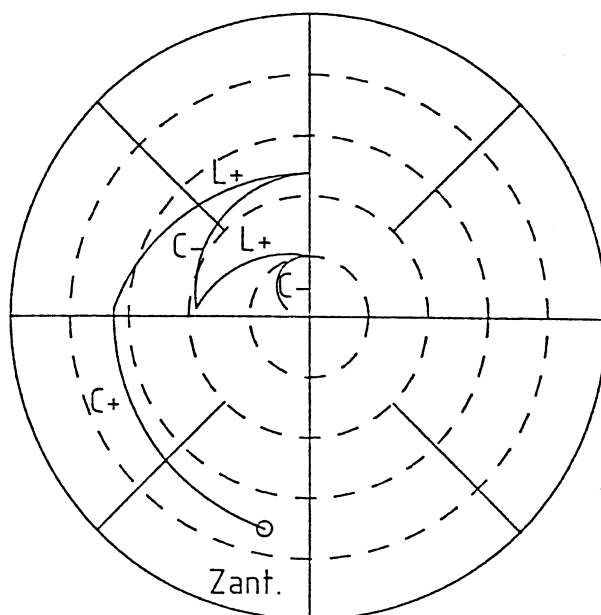


Figure 4

SELF TEST AND PROGRAM FACILITIES TU4013

The Program Function

The program function is selected by pressing the [PROGR] key followed by the program number. The program number is accepted by pressing the [enter] key.

The operation of the programs can be illustrated in this way:

- 1) Select the program.
- 2) The main menu will be displayed.

main menu

- 3) The menus are scrolled by [←] and [→] keys.

main menu

←→

sub menu 1

←→

sub menu 2

←→

- 4) The first message is displayed when a menu is selected by pressing [enter] while the menu is shown.

message 1

- 5) Sub messages may be scrolled by using [←] and [→] keys.

message 1

←→

sub mess.1.1

←→

sub mess.1.2

←→

- 6) Messages are scrolled by using the down arrow and the up arrow keys.

message 1

←→

sub mess.1.1

←→

sub mess 1.2

←→

*
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*
*

message N

←→

sub mess.N.1

←→

sub mess.N.2

←→

- 7) Pressing the down arrow keys after the last message returns the SE4010 to the former setting.

SELF TEST AND PROGRAM FACILITIES TU4013

TU4013 Programs

Program 50: Self Test

Program 51: Antenna tuner memory programming

Program 52: Antenna tuner memory clearing

Program 54: Dummy load ON/OFF

Program 55: Supervision of tuner power condition

Program 56: Battle ON/OFF

Program 57: Manual tuning

Program 58: Manual, Silent Tuning

Self Test

Program 50

The Self Test program is used to test the function of the tuner.

Antenna Tuner Memory Programming

Program 51

The programmable channels 1 through 99 are synchronized with the memory channels of the exciter, SE4010.

Antenna Tuner Memory Clearing

Program 52

After installation or service inspection of the antenna tuner or the antenna, the stored indication of tuner setting in the synthex memory must be cleared using program 52.

Dummy Load ON/OFF

Program 54

For transmitter testing a 500 W dummy load is available in the tuner.

Supervision of Tuner Power Condition

Program 55

When the tuner is operating it is possible to display the reflection coefficient (r.), the forward power (P.f.), the reflected power (P.r.) and the antenna current (i.A.) in the tuner.

SELF TEST AND PROGRAM FACILITIES TU4013

Battle ON/OFF

Program 56

The program function Battle ON/OFF allows the operator to bypass all the protection systems in the tuner.

Manual Tuning

Program 57

In manual tuning it is possible to tune the transmitter to a low VSWR operating the inductors and capacitors in the tuner.

Manual, Silent Tuning

Program 58

Program 58 has two menus, the main menu is displaying of tuner settings and the sub-menu manual setting of the tuner elements.

SELF TEST AND PROGRAM FACILITIES TU4013

Operational Status Information

During operation the following messages may occur:

AtuoFF.Line

AtuFAIL

err.Cur. o.L.

err.Atu. tPr.

SELF TEST AND PROGRAM FACILITIES TU4013

Fatal Self Test Error Messages

Error code	Module	Possible faulty component(s)
Err Ad.con.	A8	The A/D converter failed
Err SYSt.1		The transmitter muting is not functioning. If not see paragraph for the A9 module.
	A9	The High power Detector.
Err PF.L1		The tune power is too low. If not see the paragraph for the A9 module.
	A9	K1, K2, K3, R44 through R57, or low power detector.
Err Pr.L1		The tune power is too low. If not see the paragraph for the A9 module.
	A9	K1, K2, K3, R44 through R57, or low power detector.
Err r.L	A9	Low power detector.
Err PF.L2		The Tx muting is not functioning, else see the paragraph for the A9 module
	A9	Low power detector.
Err Pr.L2		The Tx muting is not functioning, else see the paragraph for the A9 module.
	A9	Low power detector.
Err SYSt.3		The Tx muting is too slow.

SELF TEST AND PROGRAM FACILITIES TU4013

Self Test Error Messages

Error code	Module	Possible faulty component(s)
Err PF.H		The tune power is low.
Err Pr.H		The input SWR for the Tx is too high or the tune power too high
	A9	K1, K2, K3, R ⁴⁴ through R57
Err r.H		The input SWR for the Tx is too high
	A9	K1, K2, K3, R ⁴⁴ through R57
Err PF.H2		The Tx muting is low
Err Pr.H2		The Tx muting is low
Err SYSt.2		The SWR for the internal dummy load is too high.
	A2	R1, R2, R3,
	A3	K1, K2, K3, K ⁴
	A4	L3, K3, C25, C26, C27, C28, R1, R2, K8
	A5	C3, C ⁴ , C5, C68, C69, C11, C67, L2, L3, K10, K11, K1, K2, K3, K13, K1 ⁴
	A6	K1, K2, K6
	A7	K7, C22, C26, C27, K2, K3
Err L 1	A4	L1, K1
Err L 2	A4	L2, K2
Err L 3	A4	L3, K3
Err L 4	A4	L ⁴ , K ⁴
Err L 5	A4	L5, K5
Err L 6	A4	L6, K6
Err L 7	A4	L7, K7

SELF TEST AND PROGRAM FACILITIES TU4013

Self Test Error Messages, continued

Error code	Module	Possible faulty component(s)
Err L 9	A3	L2, K2
Err L 10	A3	L1, K1
Err C 2	A5	C4, K2
Err C 3	A5	C5, K3
Err C 4	A5	C6, K4
Err C 5	A5	C8, C12, K5
Err C 6	A5	C7, C13, K6
Err C 7	A5	C14, C60, C61, C62, K7
Err C 8	A5	C9, C65, K8
Err C 9	A5	C10, C66, K9
Err C 10	A5	C11, C67, K10
Err C 11	A5	C68, C69, K11
Err Lb 2	A6	L2, K1, K2, K3, K6
Err Cb 1	A7	C22, K2
Err Cb 2	A7	C26, C27, K3
Err Cb 3	A7	C23, C75, K4
Err Cb 4	A7	C24, C25, K5
Err Cb 5	A7	C76, C77, K6
Err BB	A7	K7
Err cP 1	A5	L1, K15
Err cP 2	A4	C25, C26, C27, C28, R1, R2, K8
Err tP	A5	K13, K14, Q1

REMOTE OPERATION

1. PROTOCOL IN GENERAL

Transmission of data is done by a Intel 8251 programmable communication interface.

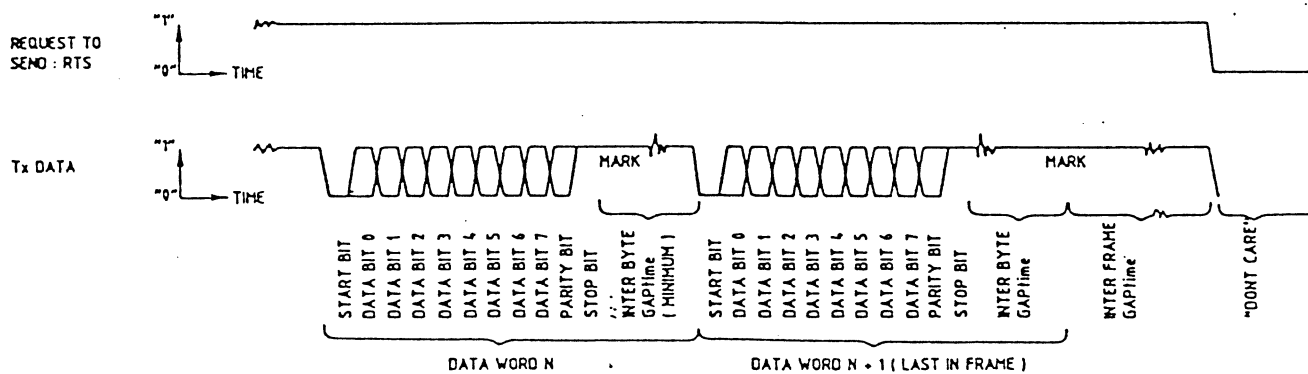
The transmission is: Asynchronous
1 start bit
8 data bits (a data byte)
1 odd parity bit
1 stop bit
INTER BYTE GAPtime (Only 9600 Baud).

After each 11 bit transmitted (start,data,parity,stop:bits) there must be a INTER BYTE GAPtime delay before the next 11 bits are transmitted (9600 Baud). This delay is necessary because the receiving software fetch received data only once per msec.

The hardware strapping on the A9 module of the unit must match the decided baudrate. The decided baudrate must also be stored in the memory of the line MASTER or MASTER CONTROLLER units, using program No. 20 on the units.

The transmission of a data package consists of transmission of a number of 8 bit data word. The total transmission of such a number of data will be referred to as a "data frame" or simply a "frame". A frame has a variable length.

INTER FRAME GAPtime / INTER BYTE GAPtime

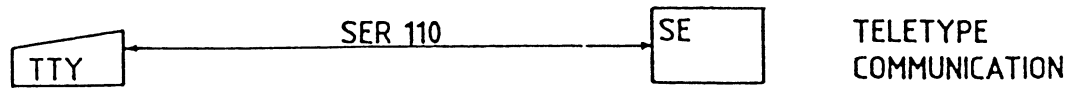
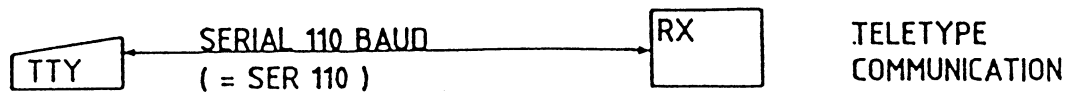


USING THE 1200 BAUD A9 MODULE RTS "LOW" WITHIN THE INTER FRAME GAPtime TELLS THE RECEIVING UNIT THAT THE TOTAL FRAME IS FINISHED. IF RTS DON'T BECOMES LOW THE TOTAL FRAME IS ACCEPTED AFTER THE INTER FRAME GAPtime.

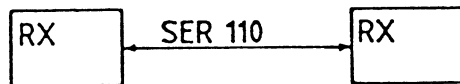
USING THE 9600 BAUD A9 MODULE RTS MUST BE "HIGH" WITHIN THE INTER FRAME GAPtime.

BAUD RATE	INTER FRAME GAPtime	INTER BYTE GAPtime
75	255 msec	0.0 msec
150	147 msec	0.0 msec
300	74 msec	0.0 msec
600	37 msec	0.0 msec
1200	19 msec	0.0 msec
2400	9 msec	0.0 msec
4800	6 msec	0.0 msec
9600	6 msec	0.9 msec

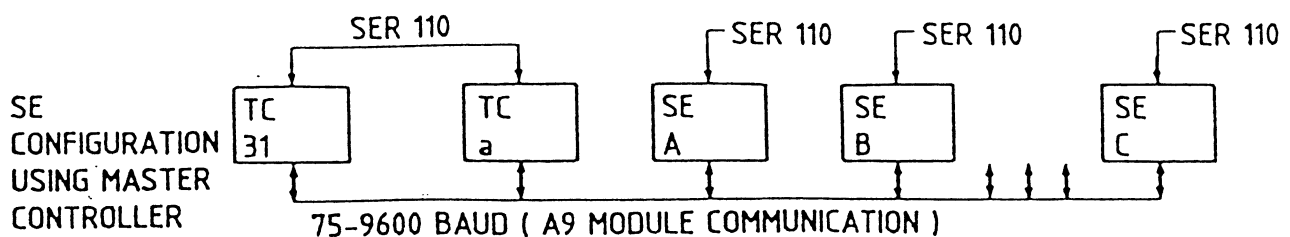
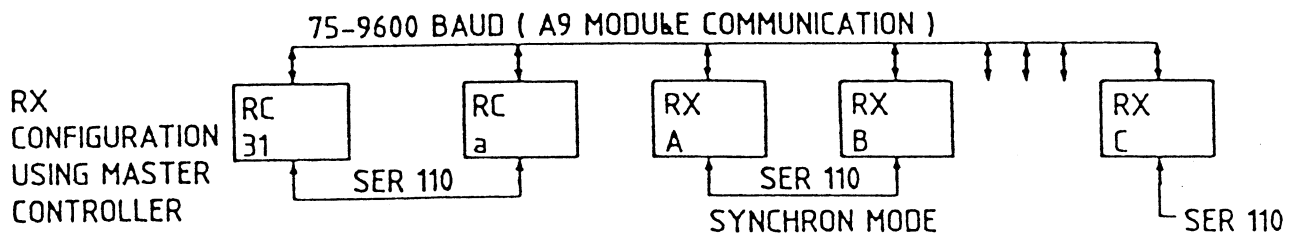
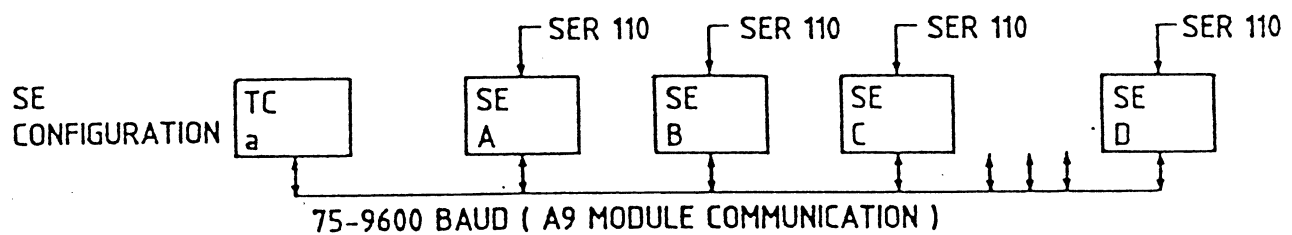
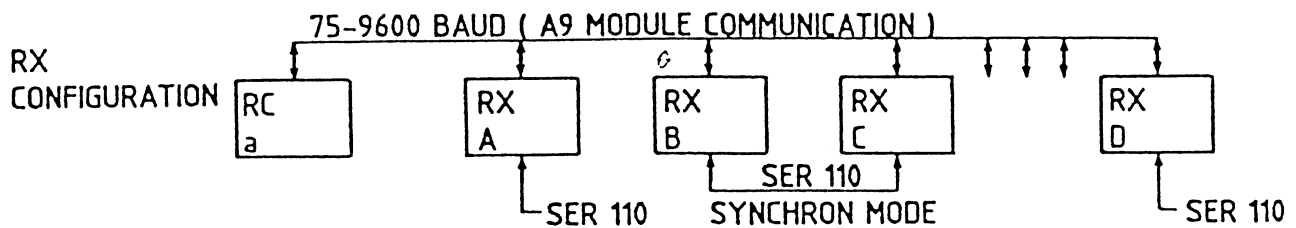
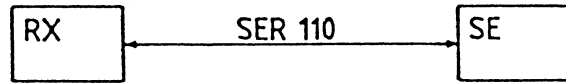
CONNECTION EXAMPLES



SYNCHRON MODE



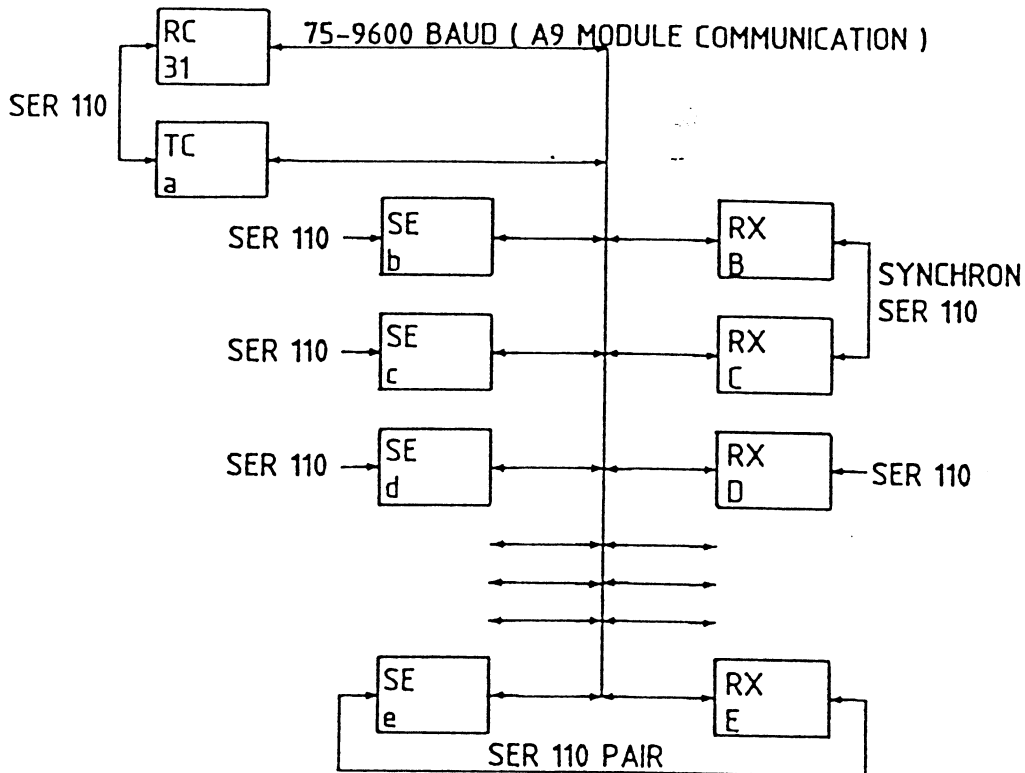
PAIR MODE



CONNECTION EXAMPLES continued

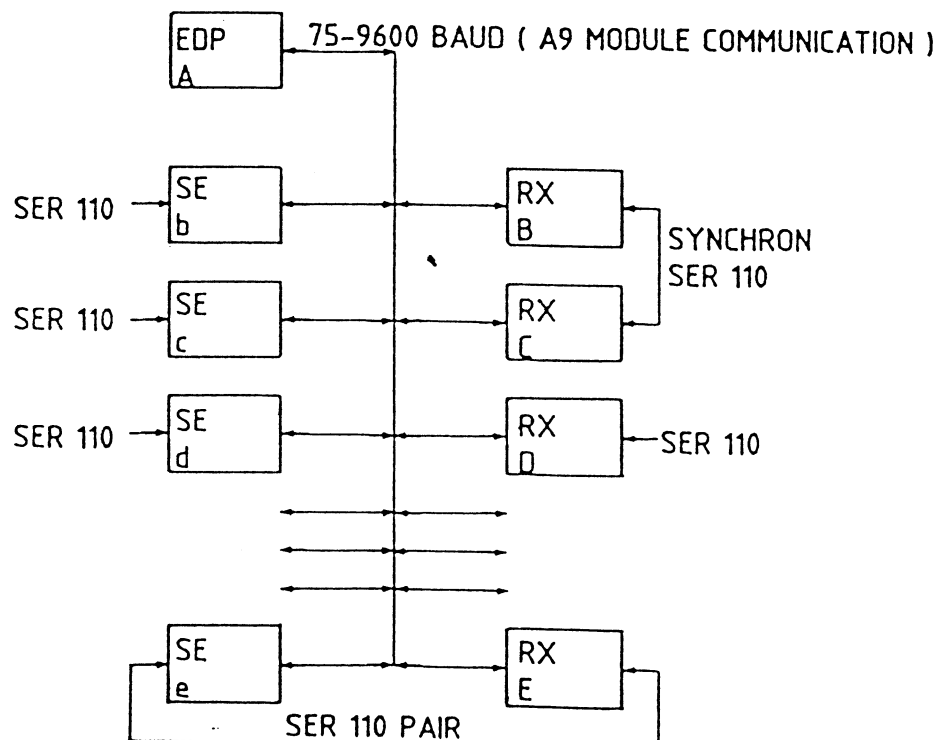
RX - SE CONFIGURATION

USING RC MASTER CONTROLLER



RX - SE CONFIGURATION

USING EDP CONTROLLER



1.1 COMMUNICATION TOOLS

Errors in network are often very difficult to locate.

To simplify the work of investigating causes of errors, there are built-in communication counters in the TC,RC,SE and RX software.

Both the normal communication via the A9 module, and the special communication via the serial 110 bps line are examined during communication.

The number of received frames and bytes are counted, as well as all errors recognized during receiving frames.

All information about the communication is stored in the AUTOMATIC REMOTE TRANSMISSION ERROR LOG (ARTEL)

1.2 ARTEL: AUTOMATIC REMOTE TRANSMISSION ERROR LOG

The counters in the ARTEL are all set to 0 when mains are switched on. Counters are incremented to a max. limit of 65535. When a counter reaches this limit, it starts counting from 0 again.

The counters for: received frames and bytes are only incremented when 256 frames (and bytes) are received.
The counter "to.S" is dedicated to the serial 110 bps communication. All the other counters are dedicated to the normal network communication.

To investigate the actual status of the counters, use program No. 41 on the TC,RC,SE and RX units.

EXPLANATION TO COUNTERS IN PROGRAM No. 41:

"r.Fr" :Number of received frames (MOD 256)

"r.bt" :Number of received bytes (MOD 256)

"Syn" :Number of synchronizing retransmissions.
Incremented every time a retransmission takes place.
REASON FOR RETRANSMISSION FROM A MASTER:
The master (TC or RC) does not receive an answering frame from a slave, within 1 sec.
REASON FOR RETRANSMISSION - ALL UNITS:
- The unit receives a wrong ACK (acknowledge)
- The unit receives a NACK (not acknowledge)

"Hd.E" :Number of header errors.
Incremented when.:
- A frame with more than 32 bytes has been received.
- The number of data in a frame does not fit together with the frame type.
- The received frame type does not exist.

"to.E" :Number of timeout errors.
Incremented when the unit has been waiting for an answering frame for more than 1 sec.

"Fr.E" :Number of framing errors.
Incremented when no stopbit has been detected after a data byte has been received. (*1)

"or.E" :Number of overrun errors.
Incremented when a new byte has arrived before the last has been read. (*1)

"Pt.E" :Number of parity errors.
Incremented when a parity error has occurred. (*1)

"to.S" :Number of timeouts/errors on the serial 110 bps line.
Incremented on wrong echo, retransmit command and if the echo has not been received within 1 sec.

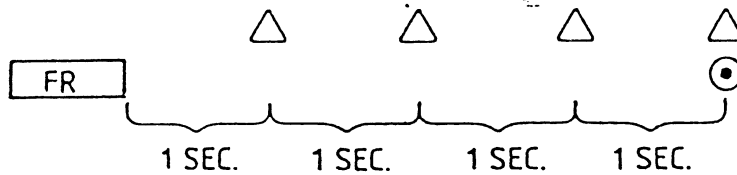
(*1) :According to Intel 8251 specifications.

TIMEOUT ACTIONS ON UNITS

SLAVES:

If a slave reaches a timeout state, it remains listening up to 4 sec.. After the 4th sec. the slave displays "Err. OFFLINE" and must be addressed to be selected again.

SCHEMATIC DRAWING



FR = LAST TRANSMITTED FRAME

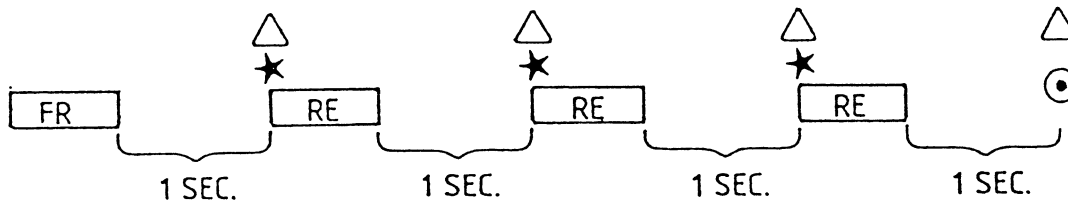
△ = TIME OUT ERROR COUNTER INCREMENTED ("to.E")

⊙ = UNIT NOT SELECTED. DISPLAYS " Err. OFFLINE "

MASTER AND MASTER CONTROLLERS:

If a master reaches a timeout state, it retransmits the last frame every 1 sec. (maximum 3 retransmissions). If there is no answer within 1 sec. after the last retransmission, the display shows "Err. OFFLINE" and automatic addressing of the last addressed unit starts.

SCHEMATIC DRAWING



FR = LAST TRANSMITTED FRAME

RE = RETRANSMISSION OF FRAME

△ = TIME OUT COUNTER INCREMENTED ("to.E")

★ = RETRANSMISSION COUNTER INCREMENTED ("syn")

⊙ = UNIT DISPLAYS " Err. OFFLINE " AND STARTS AUTOMATIC ADDRESSING

5.1 LOGIC STATE DIAGRAM OF SE AND RX UNITS.

